January 1982

analog switch & IC product data book

Siliconix
incorporated



Siliconix
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Siliconix Analog Switch & IC Product Data Book

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Siliconix incorporated reserves the right to make changes in the circuitry or specifications at any time without notice and assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

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About This Edition of the Siliconix Integrated Circuit Catalog

This Data Manual combines three previous publications: The Analog Switch, LSI and Telecommunications Data Books.

For Integrated Circuit Cross Referencing and Substitution, see the current issues of the Siliconix Short Form or OEM Pricing Guides.

NEW PRODUCT DATA SHEETS APPEARING FOR THE FIRST TIME

D169	Dual Level Shifter Driver
DF328	Loop Disconnect Dialer, Push Button Activated
DG200A	PLUS-40 CMOS Dual SPST Analog Switch
DG201A	PLUS-40 CMOS Quad SPST Analog Switch
DG202	PLUS-40 CMOS Quad SPST Analog Switch
DG212	PLUS-40 CMOS Quad SPST Analog Switch
DG243	PLUS-40 CMOS Dual SPDT Analog Switch
DG300A-DG307A	PLUS-40 CMOS Family of Analog Switches
DG381A-DG390A	PLUS-40 CMOS Family of Analog Switches
DG309	PLUS-40 CMOS Quad SPST Analog Switch
DG5040-DG5045	PLUS-40 CMOS Family of Analog Switches
DG506A/DG507A	PLUS-40 CMOS 16-Channel Analog Multiplexer
DG508A/DG509A	PLUS-40 CMOS 8-Channel Analog Multiplexer
DG528/DG529	PLUS-40 CMOS 8-Channel Latchable Analog Multiplexer
Si1525/27B, Si2525/27B, Si3525/27B	Regulating Pulse Width Modulators

DATA SHEETS NO LONGER INCLUDED

DGM111	Dual PMOS SPST Switch — Note 1
DGM122	Dual PMOS DPST Switch — Note 1
DF331A/DF332A/DF334A	μ-Law Companding CODEC — Note 1
DF341/DF342	A-Law Companding CODEC — Note 1
LD111/LD114	3½-Digit Serial Output A/D Converter Set — Note 2
LD130	3-Digit Integrating A/D Converter — Note 2
SM310	SMOKE Detector Battery Operated, Piezo Horn Drive — Note 1

Notes: 1. Contact factory on availability.
2. Obsolete product.

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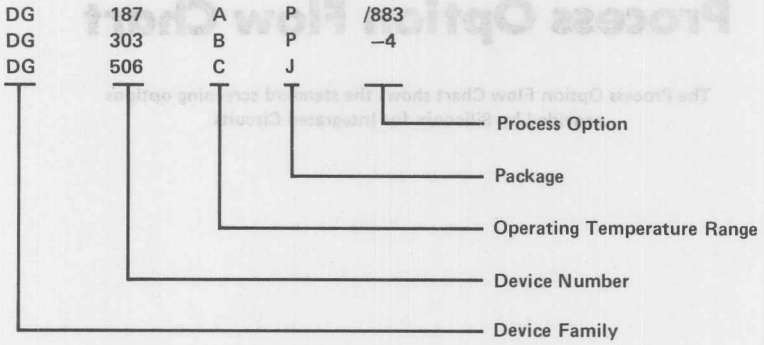
D160	Dual Level Shifter Driver
DF230	Loop Disconnect Dialer, Push Button Activated
DG200A	PLUS-40 CMOS Dual SPST Analog Switch
DG201A	PLUS-40 CMOS Quad SPST Analog Switch
DG202	PLUS-40 CMOS Quad SPST Analog Switch
DG212	PLUS-40 CMOS Quad SPST Analog Switch
DG243	PLUS-40 CMOS Dual SPDT Analog Switch
DG300A-DG301A	PLUS-40 CMOS Family of Analog Switches
DG302A-DG390A	PLUS-40 CMOS Family of Analog Switches
DG309	PLUS-40 CMOS Quad SPST Analog Switch
DG500-DG506	PLUS-40 CMOS Family of Analog Switches
DG506A/DG507A	PLUS-40 CMOS 16-Channel Analog Multiplexer
DG508A/DG509A	PLUS-40 CMOS 8-Channel Analog Multiplexer
DG528/DG529	PLUS-40 CMOS 8-Channel Latchable Analog Multiplexer
SH525/27B, SH325/27B, SH525/27B	Regulating Pulse Width Modulators

DATA SHEETS NO LONGER INCLUDED

DGM111	Dual PMOS SPST Switch—Note 1
DGM122	Dual PMOS DPST Switch—Note 1
DF231A/DF232A/DF234A	μ-Law Companding CODEC—Note 1
DF311/DF342	A-Law Companding CODEC—Note 1
LD111/LD114	3½-Digit Serial Output A/D Converter Set—Note 2
LD130	3-Digit Integrating A/D Converter—Note 2
SM510	SMOKE Detector Battery Operated, Piezo Horn Drive — Note 1

Notes: 1. Contact factory on availability
2. Obsolete product.

Device Ordering Information



DEVICE FAMILY
(1, 2 or 3 Letters)

D — Drivers for FET Switches
DF — Digital Function
DG — Analog Switches
DGM — Analog Switches
G — Multi-Channel FETs
L — Linear
LD — Linear Digital Combinations
Si — Siliconix Second Source Part
SJM — QPL Listed Part

DEVICE NUMBER
(3 or 4 Digit Numbers)

OPERATING TEMPERATURE RANGE
(1 Letter)

A — –55 to 125°C
B — –20 to 85°C
C — 0 to 70°C
D — –40 to 85°C (Applies to Telecom Products only)

B temperature range parts receive industrial processing unless a process option dash number is added to the part number.

C and D temperature range parts are given commercial processing.

All possible combinations of device types, temperature ranges, package types and MIL-883 process options are not necessarily available. Consult individual data book pages for complete information, or sales office.

PACKAGE
(1 Letter)

A — Metal Can
J — Dual In-Line Package—Plastic
K — Dual In-Line Package—CERDIP
L — Flat Package
P — Dual In-Line Package—Side Braze
R — Dual In-Line Package—Side Braze

PROCESS OPTION

/883 MIL-STD-883, Class B
–4 160 Hour Burn-In
BS9000 Series

Process Option Flow Chart

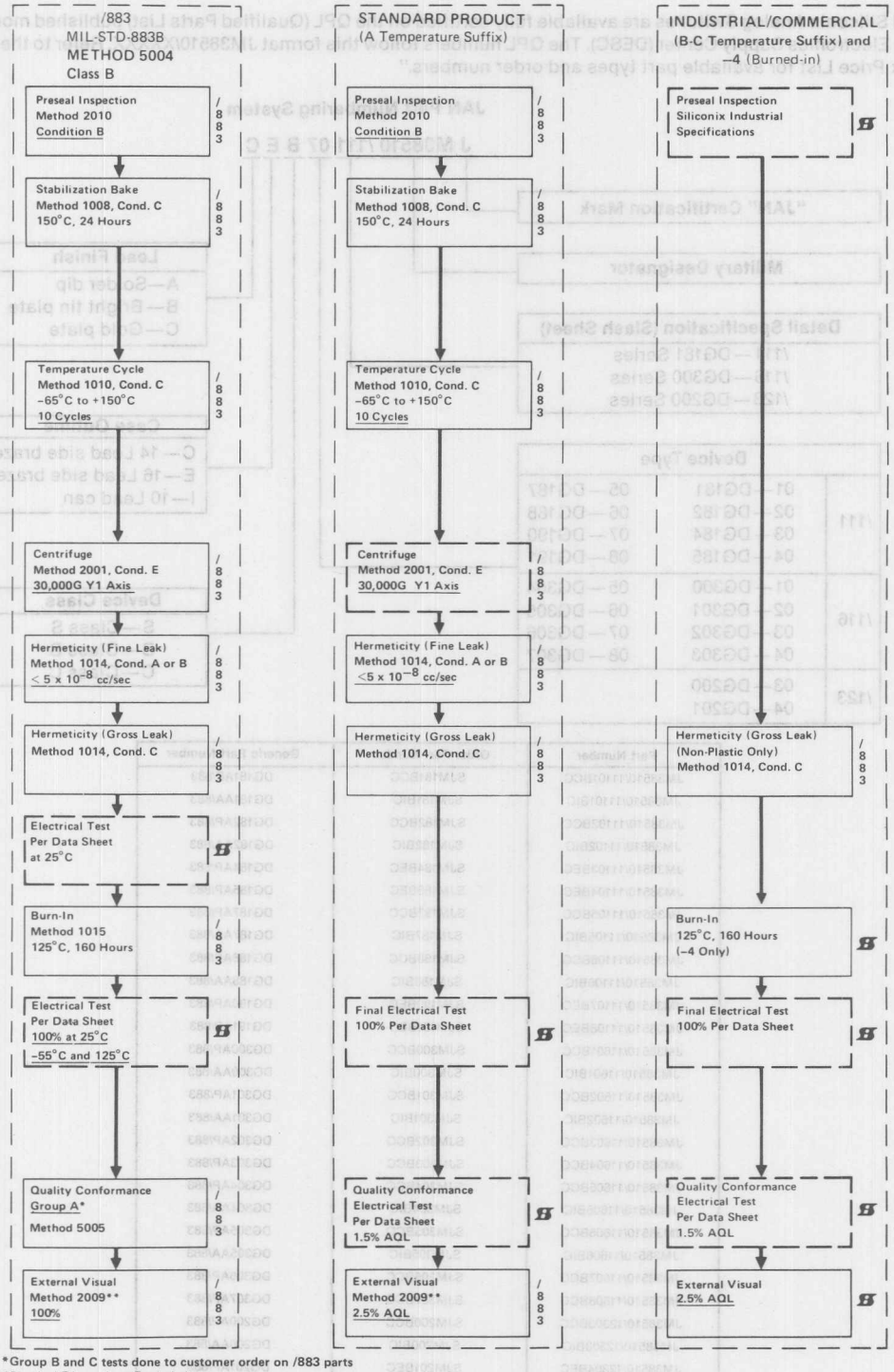
The Process Option Flow Chart shows the standard screening options provided by Siliconix for Integrated Circuits

Column 1: Denotes the screening process for MIL-883, Class B. To order a part screened to this option, add a "/883" following the package suffix letter. If Group B or C Quality Conformance is also required, call out as a separate line item. Parts in this classification are carried in inventory.

Column 2: Is the screening procedure for military grade standard products ("A" temperature suffix).

Column 3: Is the normal screening procedure for industrial and commercial grade products (B and C temperature suffixes). An industrial and commercial grade product (B and C temperature range) may be given a 160 hour burn-in at 125°C by adding a Dash 4 (–4) following the package suffix letter.

Process Option Flow Chart



*Group B and C tests done to customer order on /883 parts
**Physical Dimensions Excluded
The latest revision of MIL-STD-883 is applicable

"Several Siliconix Analog Switches are available fully certified on the QPL (Qualified Parts List) published monthly by Defense Electronics Supply Center (DESC). The QPL numbers follow this format JM38510/XXXXX. Refer to the current Siliconix Price List for available part types and order numbers."

JAN Part Numbering System

J M38510 /111 07 B E C

"JAN" Certification Mark

Military Designator

Detail Specification (Slash Sheet)

- /111 — DG181 Series
- /116 — DG300 Series
- /123 — DG200 Series

Device Type

/111	01 — DG181	05 — DG187
	02 — DG182	06 — DG188
	03 — DG184	07 — DG190
	04 — DG185	08 — DG191
/116	01 — DG300	05 — DG304
	02 — DG301	06 — DG305
	03 — DG302	07 — DG306
	04 — DG303	08 — DG307
/123	03 — DG200	
	04 — DG201	

Lead Finish

- A — Solder dip
- B — Bright tin plate
- C — Gold plate

Case Outline

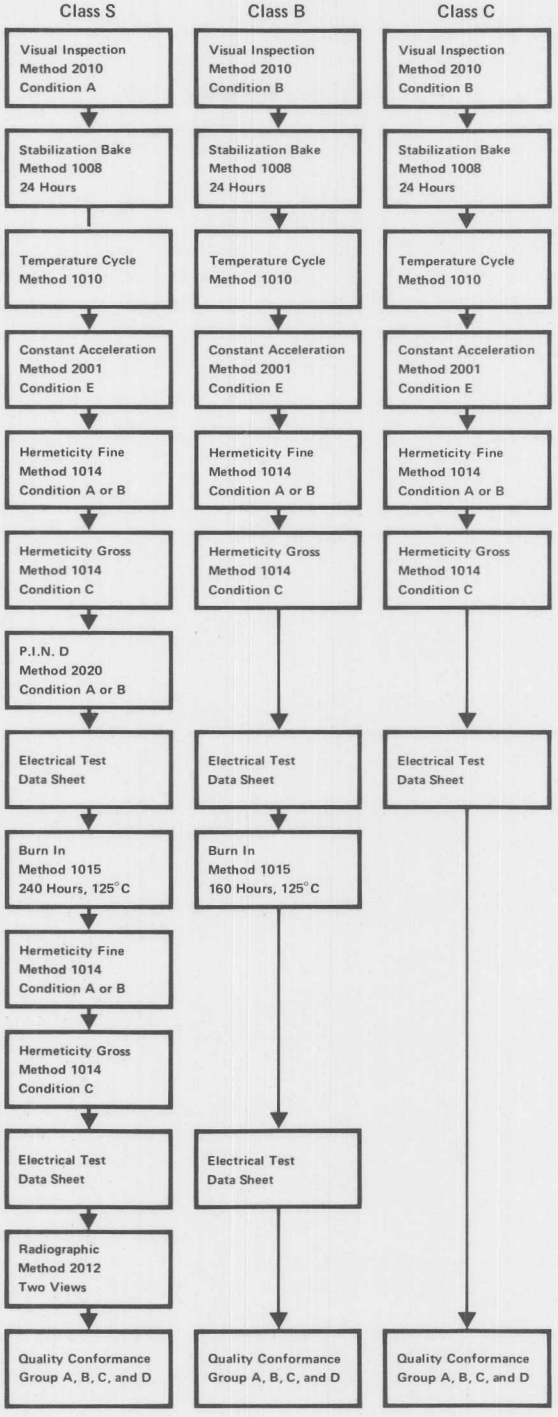
- C — 14 Lead side braze
- E — 16 Lead side braze
- I — 10 Lead can

Device Class

- S — Class S
- B — Class B
- C — Class C

Part Number	Order Part Number	Generic Part Number
JM38510/11101BCC	SJM181BCC	DG181AP/883
JM38510/11101BIC	SJM181BIC	DG181AA/883
JM38510/11102BCC	SJM182BCC	DG182AP/883
JM38510/11102BIC	SJM182BIC	DG182AA/883
JM38510/11103BEC	SJM184BEC	DG184AP/883
JM38510/11104BEC	SJM185BEC	DG185AP/883
JM38510/11105BCC	SJM187BCC	DG187AP/883
JM38510/11105BIC	SJM187BIC	DG187AA/883
JM38510/11106BCC	SJM188BCC	DG188AP/883
JM38510/11106BIC	SJM188BIC	DG188AA/883
JM38510/11107BEC	SJM190BEC	DG190AP/883
JM38510/11108BEC	SJM191BEC	DG191AP/883
JM38510/11601BCC	SJM300BCC	DG300AP/883
JM38510/11601BIC	SJM300BIC	DG300AA/883
JM38510/11602BCC	SJM301BCC	DG301AP/883
JM38510/11602BIC	SJM301BIC	DG301AA/883
JM38510/11603BCC	SJM302BCC	DG302AP/883
JM38510/11604BCC	SJM303BCC	DG303AP/883
JM38510/11605BCC	SJM304BCC	DG304AP/883
JM38510/11605BIC	SJM304BIC	DG304AA/883
JM38510/11606BCC	SJM305BCC	DG305AP/883
JM38510/11606BIC	SJM305BIC	DG305AA/883
JM38510/11607BCC	SJM306BCC	DG306AP/883
JM38510/11608BCC	SJM307BCC	DG307AP/883
JM38510/12303BCC	SJM200BCC	DG200AP/883
JM38510/12303BIC	SJM200BIC	DG200AA/883
JM38510/12304BEC	SJM201BEC	DG201AP/883

JM38510/883 Process Option Flow Chart



JM38510/883 Process Option Flow Chart

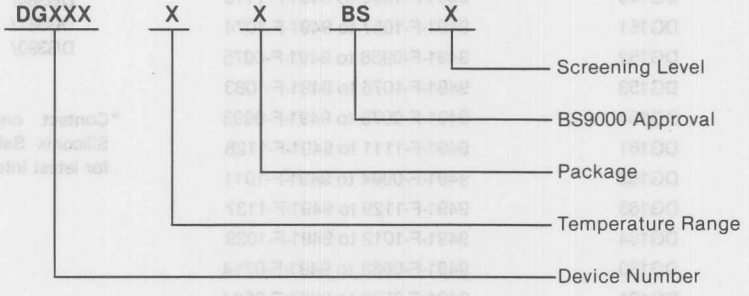
BS9000 Approved Analog Switches

Siliconix is the first company to receive BS9000 approval for Analog Switch Devices. The advantages of such approval are:

- A controlled inspection is known to the customer, so reduces the customer's needs for Goods Inwards Inspection
- A more consistent quality of product
- Easier interchangeability of suppliers
- A product of known quality levels with, in general, a minimal increase in costs

It is the policy of the UK government to encourage the growth of the BS9000 scheme for the benefit of both government and industry. All the Siliconix BS9000-Approved parts are included in the British Ministry of Defence Preferred Range defined in DEF-STAN 56/36 and as such are first choice components for use in UK defense equipment. Under STANAG 4093 they carry approved status with other NATO member nations.

Interpretation of Ordering Information



Key

Temperature Range

A	– 55°C to 125°C
B	– 20°C to 85°C

Package

A	Metal Can
L	Flatpack
P, R	Dual-In-Line

Screening Level

(Blank)	Full Assessment
.S1	Screening Level S1
S2	Screening Level S2
S3	Screening Level S3
S4	Screening Level S4

BS9000 Approved Analog Switches (Cont'd)

DEVICE PART NUMBER	BS DETAIL SPECIFICATION
DG126	9491-F-0814 to 9491-F-0831
DG129	9491-F-0832 to 9491-F-0849
DG133	9491-F-0850 to 9491-F-0867
DG134	9491-F-0868 to 9491-F-0885
DG139	9491-F-0886 to 9491-F-0903
DG140	9491-F-1030 to 9491-F-1038
DG141	9491-F-1039 to 9491-F-1056
DG142	9491-F-0904 to 9491-F-0921
DG143	9491-F-0922 to 9491-F-0939
DG144	9491-F-0940 to 9491-F-0957
DG145	9491-F-1084 to 9491-F-1092
DG146	9491-F-1093 to 9491-F-1110
DG151	9491-F-1057 to 9491-F-1074
DG152	9491-F-0958 to 9491-F-0975
DG153	9491-F-1075 to 9491-F-1083
DG154	9491-F-0976 to 9491-F-0993
DG161	9491-F-1111 to 9491-F-1128
DG162	9491-F-0994 to 9491-F-1011
DG163	9491-F-1129 to 9491-F-1137
DG164	9491-F-1012 to 9491-F-1029
DG180	9491-F-0688 to 9491-F-0714
DG181	9491-F-0508 to 9491-F-0534
DG182	9491-F-0535 to 9491-F-0561
DG183	9491-F-0733 to 9491-F-0750
DG184	9491-F-0562 to 9491-F-0579
DG185	9491-F-0580 to 9491-F-0597
DG186	9491-F-0751 to 9491-F-0777
DG187	9491-F-0598 to 9491-F-0624
DG188	9491-F-0625 to 9491-F-0651
DG189	9491-F-0715 to 9491-F-0732
DG190	9491-F-0652 to 9491-F-0669
DG191	9491-F-0670 to 9491-F-0687
DG200	9491-F-0778 to 9491-F-0804
DG201	9491-F-0805 to 9491-F-0813
DG501	9491-F-1138 to 9491-F-1146
DG503	9491-F-1147 to 9491-F-1155
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DG509	9491-F-1192 to 9491-F-1200
SI3705	9491-F-1156 to 9491-F-1164

Awaiting Approval*

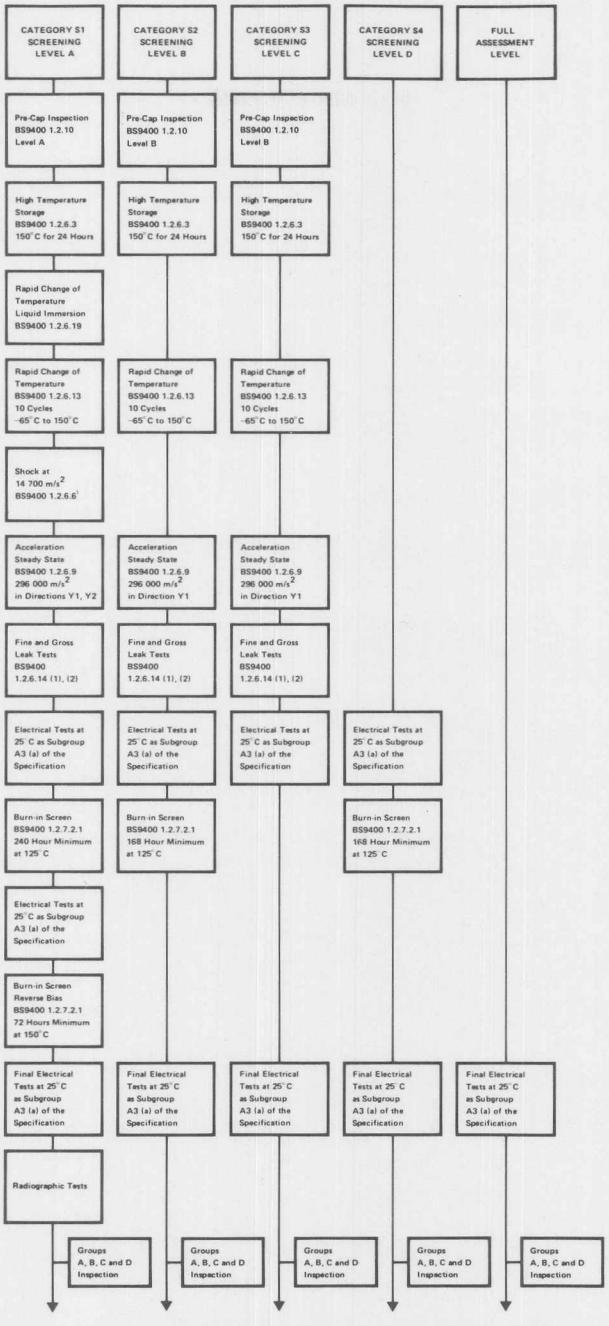
Generic Part No.

DG281/ /BS
DG284/ /BS
DG287/ /BS
DG290/ /BS
DG300/ /BS
DG301/ /BS
DG302/ /BS
DG303/ /BS
DG304/ /BS
DG305/ /BS
DG306/ /BS
DG307/ /BS
DG381/ /BS
DG384/ /BS
DG387/ /BS
DG390/ /BS

*Contact one of the Siliconix Sales Offices for latest information.

Specifications are being raised for additional parts to BS9000, which will be qualified during the currency of this catalogue. For approval status and copies of the detail specifications for the products approved (or in course of qualification approval) please contact Siliconix Ltd., Morriston, Swansea SA6 6NE. Telephone (0792) 74681, Telex: 48197.

BS9000 Series Process Option Flow Chart



INSPECTION REQUIREMENTS: All tests to be conducted at $T_{amb} = 25°C$ unless otherwise specified. Samples submitted to tests marked 'D' shall not be accepted for release under BS9000 (see 2.6.5 of BS9000 Part I).

Flow chart for 100% screening test procedures (see also Inspection Requirements). Production batches containing greater than 10% defective units subsequent to Burn-in will not be issued for release. The following acceptance/rejection criteria apply to the electrical tests after Burn-in for screening levels A, B and D.

(a) Lots exhibiting greater than 20% defectives shall be rejected.
(b) Lots exhibiting less than 10% defectives shall be accepted.
(c) Lots exhibiting between 10% and 20% defectives (inclusive) shall have the defectives removed and the remainder of the lot subjected to an identical Burn-in. If such a Lot then exhibits greater than 5% defectives is shall be rejected.

Radiographic tests. Each device shall be examined, for extraneous matter and assembly defects, in the X and Y directions.

Siliconix

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INTERFACE

DECODERS/DISPLAY DRIVERS

Title		Page
DF412	Decodes Four Digit Multiplexed BCD to LCD Display Driver/Decodes up to 4 digits of multiplexed BCD information and derives the AC signals needed to drive a 4 digit LCD display. Any digit can be blanked as required.	1-1

LEVEL SHIFTERS

	Channels	Input Load	Output Drive	t_{ON}/t_{OFF}	
D123	6	1 mA/1 μA 1.0 V/0.4 V	ON—5 mA Sink, OFF—Block 30 V	500/1500 ns	1-8
D125	6	−0.7 mA/+1 μA 0 V/4.6 V	ON—5 mA Sink, OFF—Block 30 V	500/1500 ns	1-10
D129	4	−0.2 mA/+.25 μA 0 V/5 V	ON—10 mA Sink, OFF—Block 50 V	300/1500ns	1-12
D139	2	−500 μA/+10 μA 0 V/+5 V	30 V p-p @ 10 mA	170/200 ns	1-14
D169	2	−100 μA/+5 μA 0 V/+3 V	33 V p-p @ 40 mA	70–110 ns	1-20

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Four Digit LCD Decoder Driver

Siliconix

designed for . . .

■ Driving Liquid Crystal Displays Directly

BENEFITS

- Reduces Complexity of Driving LCD Displays
- Blanking of any Digit with Input Code of 1111
- Only 1 Package Required to Drive Up to a 4 Digit Display
- Minimal Power Consumption
 - Typically 1.5 mW
 - Operates over 3.5 to 6.0 V supply
- Interfaces Readily with Most Logic Families
- No External Oscillator Required
- No Display Buffering Required
- Easy Multiple Driver Interfacing
- Eliminates DC Bias Levels That Degrade Display Lifetime

DESCRIPTION

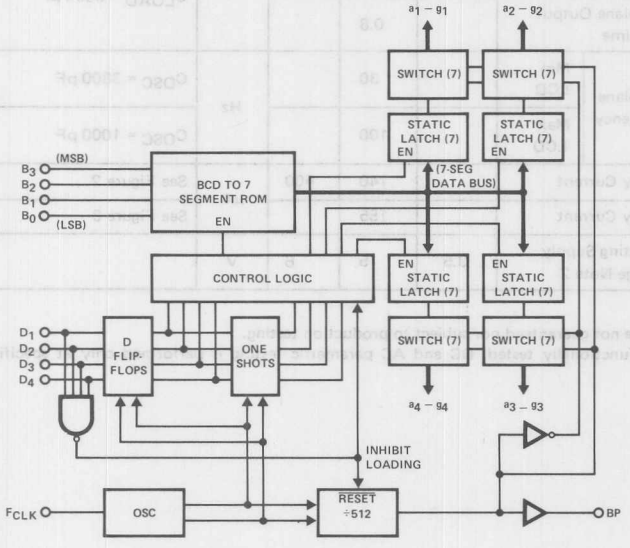
The DF412 Four Digit LCD Decoder Driver is a CMOS Monolithic device employing multiplexed BCD to LCD Decoding. A single DF412 contains all of the circuitry needed to decode up to 4 digits of multiplexed BCD information and derive the AC signals needed to directly drive a 4 digit LCD display. Included is the decoding of BCD input 1111 to blank a digit.

An internal oscillator, its frequency being controlled by an external capacitor, develops a backplane (BP) signal that is a square wave swinging between ground (V_{SS}) and the positive supply (V_{DD}). Segment drivers supply square waves of the same frequency as the backplane but either in phase for an OFF segment or out of phase for an ON segment. In this manner of LCD digit driving the net DC potential applied between segment and backplane is zero, a necessary requirement for long display life. Digital input levels are defined as input voltages > 4 V being a logic "1" and input voltages < 0.8 V being a logic "0" with $V_{DD} = 5$ V.

BCD input data is decoded into 7 segment form using an on board ROM. The 7 segment data is then latched into the appropriate static latches via the digit strobe inputs and control logic.

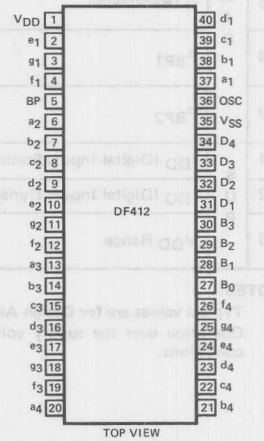
The pinout of the DF412 allows easy PC board interfaces to Dual-In-Line LCDs as well as edge connecting types of displays.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

V_{DD} COMMON TO SUBSTRATE

ORDER NUMBER DF412CJ
SEE PACKAGE 22

ABSOLUTE MAXIMUM RATINGS

$V_{DD} - V_{SS}$ −0.3 V to 8 V
Voltage on Any Pin $V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V
Current at Any Pin 10 mA
Operating Temperature 0 to 70°C
Storage Temperature −65 to 125°C
Power Dissipation (Package)* 450 mW
*Device mounted with all leads welded or soldered to PC board. Derate 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters to assure conformance with specifications.

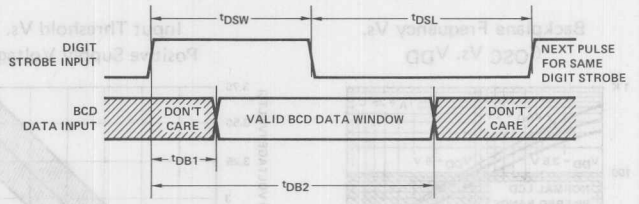
		Characteristic			Limits Min	Limits Typ[1]	Limits Max	Unit	Test Conditions V_{DD} = 5 V, T_A = 25°C, V_{SS} = 0 V, C_{OSC} = 200 pF
1	INPUTS	I_{IN} (Digits)	Digital Inputs Leakage Currents			0.01	1	µA	V_{IN} = 5 V
2	INPUTS	I_{IN} (F_{CLK})	Oscillator Input Current			350		µA	V_{IN} = 0 V
						−350			
3	INPUTS	V_{INL}	Digital Inputs Logic Low Voltage				0.8	V	BCD and DS Inputs
4	INPUTS	V_{INL}	Digital Inputs Logic Low Voltage				0.5	V	Clock Input
5	INPUTS	V_{INH}	Digital Inputs Logic High Voltage		4.0			V	BCD and DS Inputs
6	INPUTS	V_{INH}	Digital Inputs Logic High Voltage		4.5			V	Clock Input
7	OUTPUTS	V_{OL} (Segments)	Segment Output Voltage in "0" State			0.3	0.7	V	I_{OL} = 250 µA
8	OUTPUTS	V_{OL} (Segments)	Segment Output Voltage in "0" State			0.03		V	I_{OL} = 25 µA
9	OUTPUTS	V_{OH} (Segments)	Segment Output Voltage in "1" State		4.3	4.7		V	I_{OH} = −250 µA
10	OUTPUTS	V_{OH} (Segments)	Segment Output Voltage in "1" State			4.97		V	I_{OH} = −25 µA
11	OUTPUTS	V_{OL} (Backplane)	Backplane Output Voltage in "0" State			0.3	0.7	V	I_{OL} = 5 mA
12	OUTPUTS	V_{OL} (Backplane)	Backplane Output Voltage in "0" State			0.03		V	I_{OL} = 0.5 mA
13	OUTPUTS	V_{OH} (Backplane)	Backplane Output Voltage in "1" State		4.3	4.7		V	I_{OH} = −5 mA
14	OUTPUTS	V_{OH} (Backplane)	Backplane Output Voltage in "1" State			4.97		V	I_{OH} = −0.5 mA
15	DYNAMIC	t_r (Segments)	Segment Output Rise Time			1.0		µs	C_{LOAD} = 200 pF
16	DYNAMIC	t_f (Segments)	Segment Output Fall Time			1.0		µs	C_{LOAD} = 200 pF
17	DYNAMIC	t_r (Backplane)	Backplane Output Rise Time			0.8		µs	C_{LOAD} = 3900 pF
18	DYNAMIC	t_f (Backplane)	Backplane Output Fall Time			0.8		µs	C_{LOAD} = 3900 pF
19	DYNAMIC	F_{BP1}	Backplane Frequency	Min LCD		30		Hz	C_{OSC} = 3800 pF
20	DYNAMIC	F_{BP2}	Backplane Frequency	Max LCD		100		Hz	C_{OSC} = 1000 pF
21	SUP	I_{DD} (Digital Inputs Static)	Supply Current			140	400	µA	See Figure 2
22	SUP	I_{DD} (Digital Inputs Dynamic)	Supply Current			155		µA	See Figure 3
23	SUP	V_{DD} Range	Operating Supply Voltage Note 2		3.5	5	6	V	

NOTES:
1. Typical values are for Design Aid Only, and are not guaranteed nor subject to production testing.
2. Operation over the supply voltage range is functionally tested. DC and AC parametric testing is performed only at specified test conditions.

TRUTH TABLE

B_3	B_2	B_1	B_0	DISPLAY CHARACTER
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	-
1	0	1	1	=
1	1	0	0	L
1	1	0	1	L
1	1	1	0	L
1	1	1	1	BLANK

TIMING WAVEFORMS AND DEFINITIONS



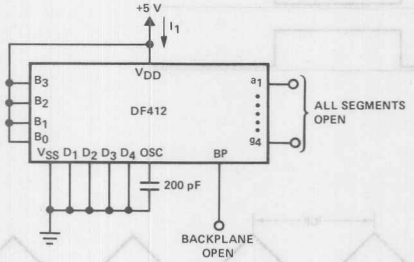
Recommended Drive Conditions*		Min	Max
t_{CP}	Clock Period	19.5 μs**	65 μs**
t_{DSW}	Digit Strobe Pulse Width	t_{CP} + 1 μs	–
t_{DSL}	Digit Strobe Low Time	2 t_{CP}	
t_{DB1}	Digit Strobe to BCD Setup Time	−∞	t_{CP}−2 μs
t_{DB2}	Digit Strobe to BCD Hold Time	2 t_{CP} + 2 μs	∞

* These minimum/maximum conditions indicate the necessary conditions to insure operation. They are based on design structure (shown in Figure 8a) with sufficient guardband to allow for propagation delay changes. *They are not tested nor guaranteed.*

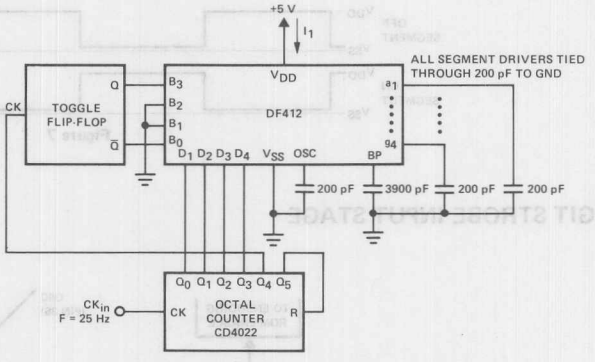
** The min-max clock periods correspond to a 30 Hz–100 Hz LCD backplane frequency range.

Figure 1

TEST CIRCUITS



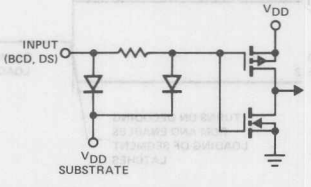
Static Supply Current Test Setup
Figure 2



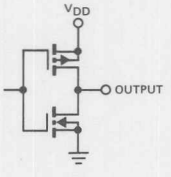
Dynamic Supply Current Test Setup
Figure 3

INPUT-OUTPUT SCHEMATICS

Input Structure



Output Structure



TYPICAL CHARACTERISTICS

Backplane Frequency Vs. C_{OSC} Vs. V_{DD}

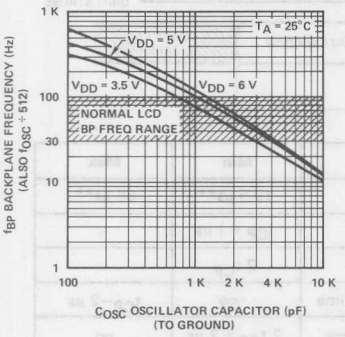


Figure 4

Input Threshold Vs. Positive Supply Voltage

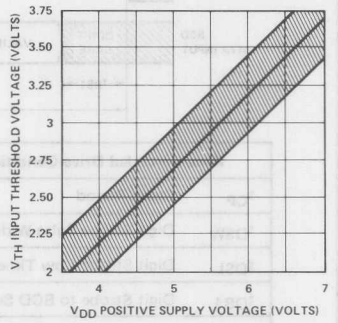


Figure 5

Supply Current Vs. Temperature

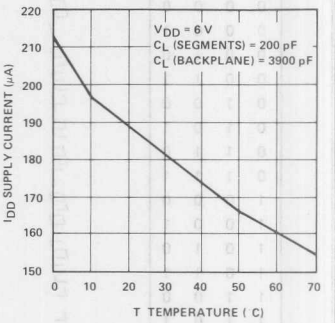


Figure 6

TYPICAL WAVEFORMS

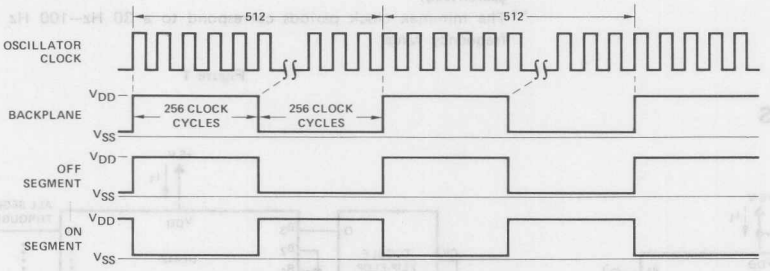
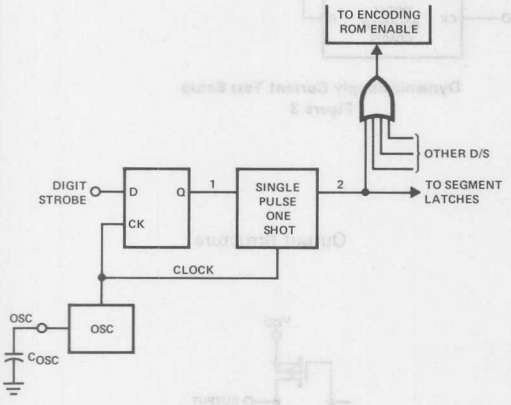
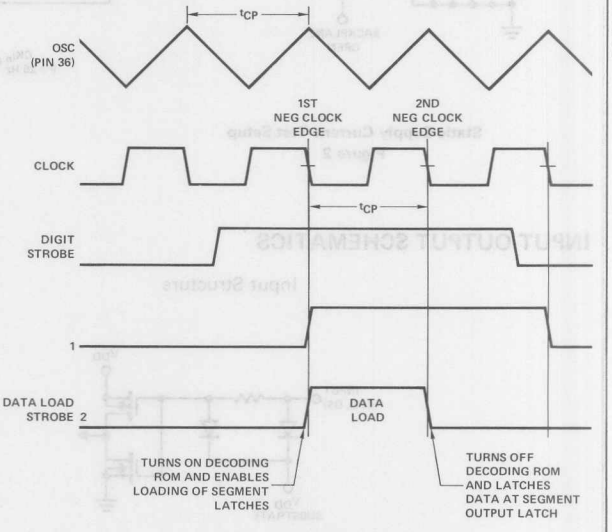


Figure 7

DIGIT STROBE INPUT STAGE



Digit Strobe Input Circuit
Figure 8a



Digit Strobe and Clock Timing Relationships to Data Loading
Figure 8b

PIN DESCRIPTIONS

Oscillator – A capacitor connected between the oscillator pin and ground completes the integral clock generator. The frequency of the clock generator (f_{OSC}) is determined by the capacitance value and the V_{DD} voltage, as seen in Figure 4. For driving LCDs with a 30 Hz to 100 Hz backplane frequency range, the typical oscillator capacitor is 1000 pF to 3800 pF (for V_{DD} = 5 V). The oscillator pin can also be driven with an external clock whose output swings within 10% of V_{DD} and V_{SS}. This is useful when synchronization of more than one DF412 is necessary, such as when driving displays of more than 4 digits on a single backplane.

Backplane – The backplane of the liquid crystal display is driven by this pin whose output is a squarewave swinging between V_{DD} and V_{SS}. The frequency of the backplane signal is $f_{OSC}/512$. Most LCDs require backplane frequencies of between 30 Hz and 100 Hz. See Figure 4 for a graph of oscillator capacitance vs backplane frequency.

Digit Strobes D_1–D_4 and BCD Inputs B_3, B_2, B_1 and B_0– Multiplexed BCD information is entered into the DF412 by presenting the appropriate BCD code to the inputs B_3, B_2, B_1 and B_0 and by pulsing the appropriate digit strobe input D_1, D_2, D_3 or D_4 with positive true logic (i.e., $V_{INH} \geq [0.8 \times V_{DD}]$ for logic 1, $V_{INL} \leq 0.8$ V for logic 0). The minimum pulse width of a digit strobe should be not less than one period of the oscillator frequency. Information presented at the BCD inputs (B_3, B_2, B_1, B_0) must be valid during the digit strobe pulse. See the timing requirements in Figure 1.

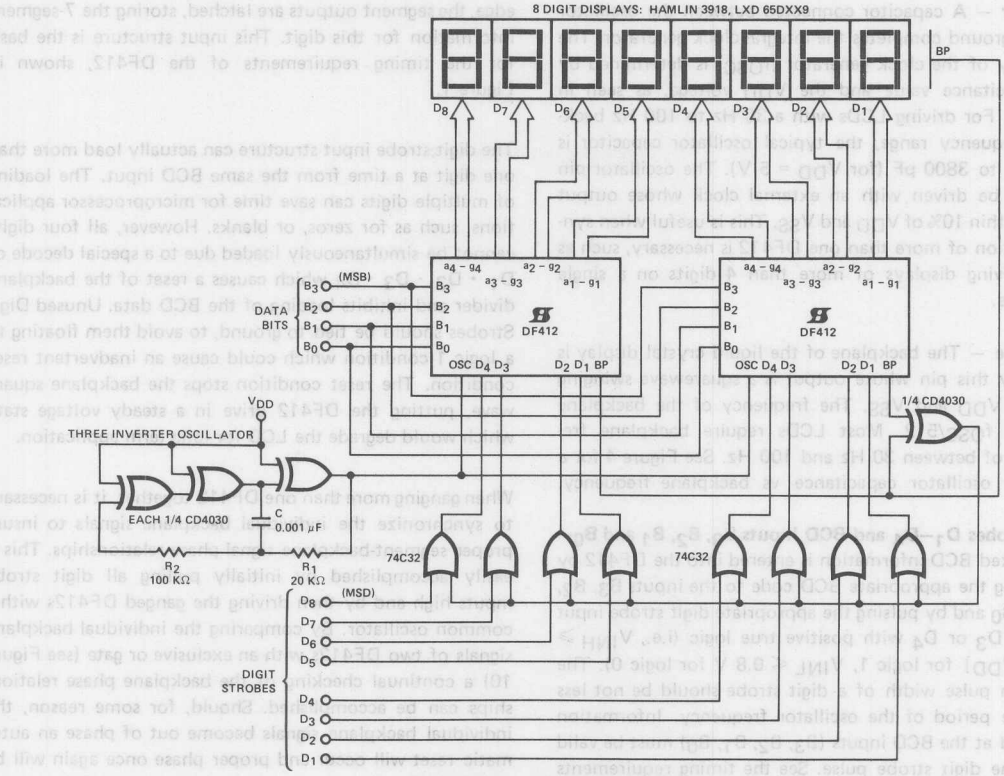
The digit strobe inputs are shaped by the input logic shown in Figure 8a. This logic causes a strobe signal which is a single clock period wide. The active time of this data load strobe (shown in Figure 8b) enables the BCD to 7-segment decoding ROM, which brings the new 7-segment data to the output latches. Delay time for data to get from BCD input to the segment outputs is typically 2 μs–3 μs. The end of the data load strobe is triggered by the second negative clock edge following the digit strobe going high. At this edge, the segment outputs are latched, storing the 7-segment information for this digit. This input structure is the basis for the timing requirements of the DF412, shown in Figure 1.

The digit strobe input structure can actually load more than one digit at a time from the same BCD input. The loading of multiple digits can save time for microprocessor applications, such as for zeros, or blanks. However, all four digits cannot be simultaneously loaded due to a special decode of $D_1 \cdot D_2 \cdot D_3 \cdot D_4$ which causes a reset of the backplane divider and inhibits loading of the BCD data. Unused Digit Strobes should be tied to ground, to avoid them floating to a logic 1 condition which could cause an inadvertent reset condition. The reset condition stops the backplane square wave, putting the DF412 drive in a steady voltage state which would degrade the LCD for long term application.

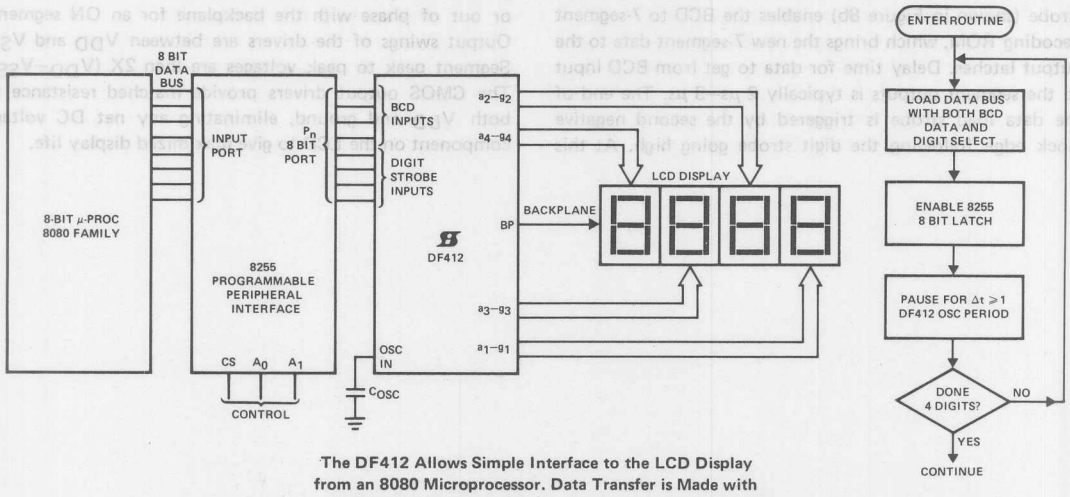
When ganging more than one DF412 together, it is necessary to synchronize the individual backplane signals to insure proper segment-backplane signal phase relationships. This is easily accomplished by initially pulling all digit strobe inputs high and by then driving the ganged DF412s with a common oscillator. By comparing the individual backplane signals of two DF412s with an exclusive or gate (see Figure 10) a continual checking of the backplane phase relationships can be accomplished. Should, for some reason, the individual backplane signals become out of phase an automatic reset will occur and proper phase once again will be established.

Segment Outputs – Segments are driven with the DF412 segment outputs which generate square waves which are either in phase with the backplane for an OFF segment or out of phase with the backplane for an ON segment. Output swings of the drivers are between V_{DD} and V_{SS}. Segment peak to peak voltages are then 2X (V_{DD}–V_{SS}). The CMOS output drivers provide matched resistance to both V_{DD} and ground, eliminating any net DC voltage component on the LCD to give maximized display life.

APPLICATIONS

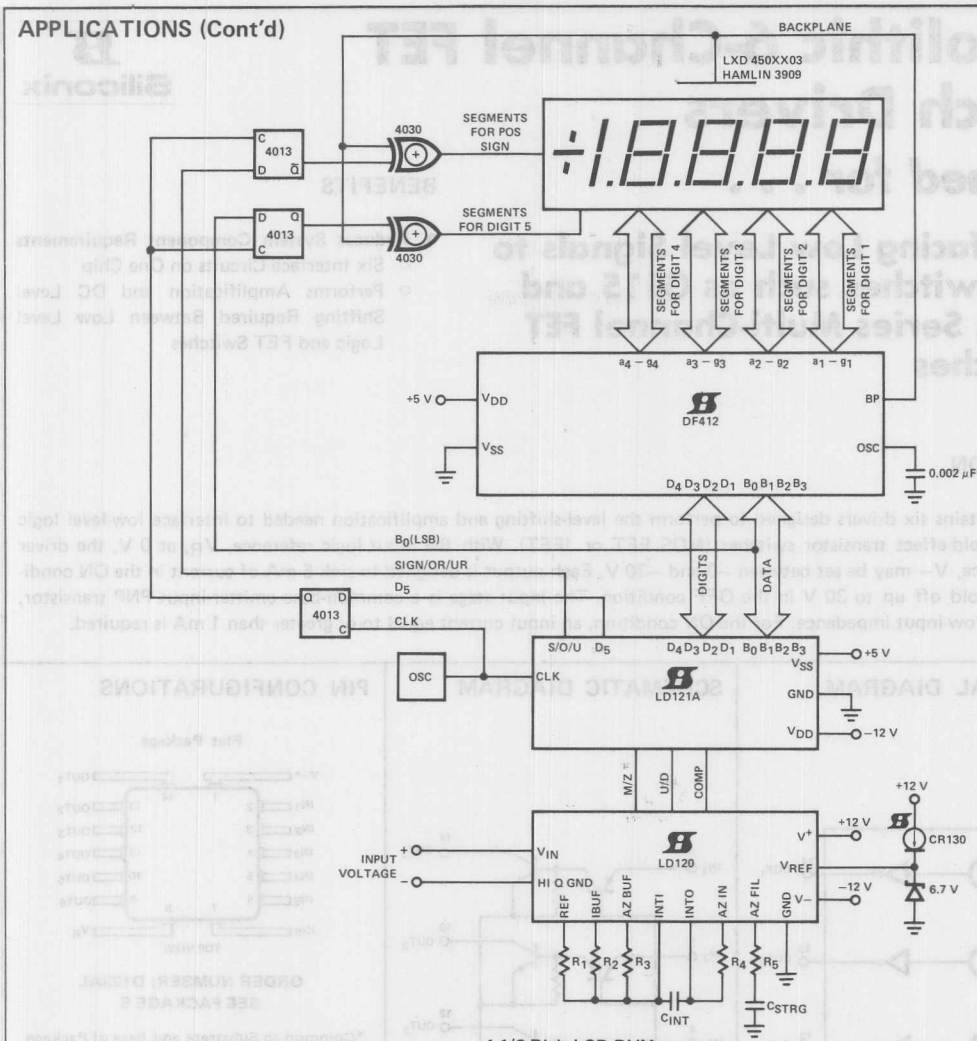


Ganged DF412's Drive 8 Digit LCD
Figure 9

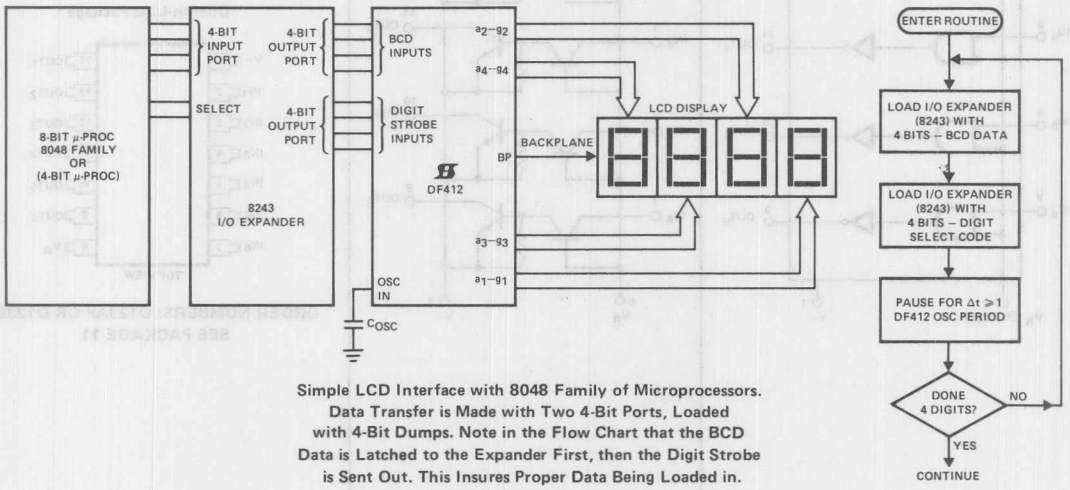


The DF412 Allows Simple Interface to the LCD Display from an 8080 Microprocessor. Data Transfer is Made with an 8 Bit Dump, Bringing Both the BCD Input and the Digit Strobes to the Chip in Parallel
Figure 10

APPLICATIONS (Cont'd)



4 1/2 Digit LCD-DVM
Figure 11



Simple LCD Interface with 8048 Family of Microprocessors. Data Transfer is Made with Two 4-Bit Ports, Loaded with 4-Bit Dumps. Note in the Flow Chart that the BCD Data is Latched to the Expander First, then the Digit Strobe is Sent Out. This Insures Proper Data Being Loaded in.
Figure 12

Monolithic 6-Channel FET Switch Drivers

Siliconix

designed for . . .

- **Interfacing Low Level Signals to FET Switches such as G115 and G122 Series Multi-Channel FET Switches**

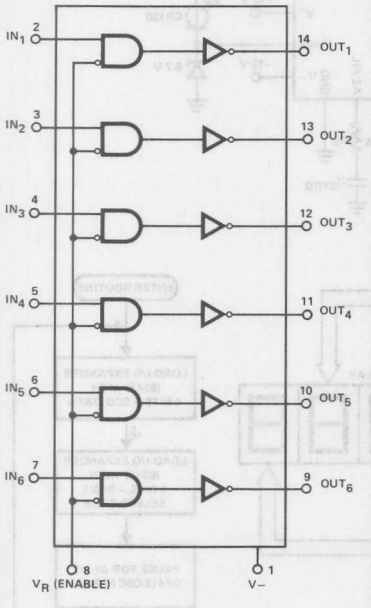
BENEFITS

- **Reduces System Component Requirements**
 - Six Interface Circuits on One Chip
 - Performs Amplification and DC Level Shifting Required Between Low Level Logic and FET Switches

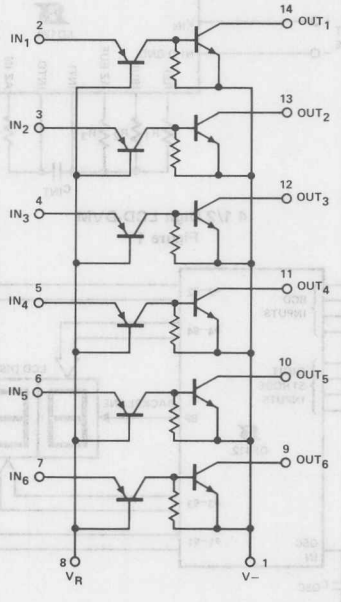
DESCRIPTION

The D123 contains six drivers designed to perform the level-shifting and amplification needed to interface low-level logic outputs and field-effect transistor switches (MOS FET or JFET). With the input logic reference, V_R, at 0 V, the driver output reference, V– may be set between –3 and –30 V. Each output is designed to sink 5 mA of current in the ON condition, and to hold off up to 30 V in the OFF condition. The input stage is a common-base emitter-input PNP transistor, and thus has a low input impedance. For the ON condition, an input current equal to or greater than 1 mA is required.

FUNCTIONAL DIAGRAM

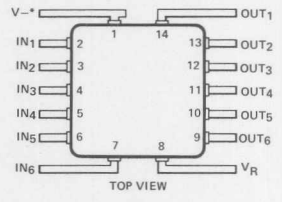


SCHEMATIC DIAGRAM



PIN CONFIGURATIONS

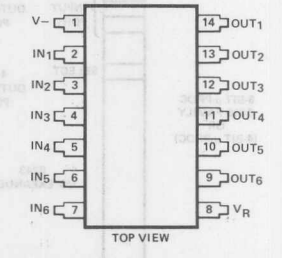
Flat Package



ORDER NUMBER: D123AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

Dual-In-Line Package



ORDER NUMBERS: D123AP OR D123BP
SEE PACKAGE 11

ABSOLUTE MAXIMUM RATINGS

V_O to V− 36 V
V_R to V− 25 V
V_{IN} to V− 30 V
V_{IN} to V_R ±2 V
Current (Any Terminal) 30 mA
Storage Temperature −65 to 150°C

Operating Temperature (A Suffix) −55 to 125°C
(B Suffix) −20 to 85°C
Power Dissipation*
Flat Package** 750 mW
14 Pin DIP*** 825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

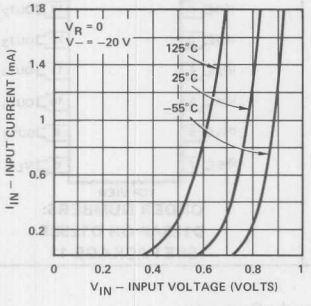
All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS D123A −55°C	D123A 25°C	D123A 125°C	D123B −20°C	D123B 25°C	D123B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V− = −20 V, V_R = 0	
1	OUT	V_{OL}	Output Voltage, Low	−19.6	−19.6	−19.5	−19.6	−19.6	−19.5	V	I_O = 5 mA, I_{IN} = 1 mA	
2	OUT	I_{OH}	Output Current, High	0.1	0.1	10	0.1	0.1	10	µA	V_O = 10 V, V_{IN} = 0.4 V	
3	IN	I_{INL}	Input Current, Input Voltage Low	1	1	100	1	1	100	µA	V_{IN} = 0.4 V	
4	IN	V_{INH}	Input Voltage, High	1.3	1	0.8	1.3	1	1	V	I_{IN} = 1 mA	
5	TIME	t_{on}	Turn-ON Time		0.5			0.5		µs	See Switching Time Test Circuit	
6	TIME	t_{off}	Turn-OFF Time		1.2			1.5				
7	SUPPLY	I−	Negative Supply Current	−1	−1	−1.5	−1	−1	−1.5	mA	I_O = 0	I_{IN1} = 1 mA, All Other V_{IN} = 0.4 V
8	SUPPLY	I_R	Reference Supply Current	−0.5	−0.5	−0.5	−0.6	−0.6	−0.6			
9	SUPPLY	I−	Negative Supply Current	−2	−2	−200	−5	−5	−100	µA	V_O = 10 V	All V_{IN} = 0.4 V
10	SUPPLY	I_R	Reference Supply Current	−1	−1	−150	−5	−5	−100			

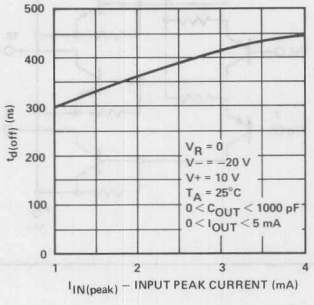
IBAF-A

TYPICAL CHARACTERISTICS

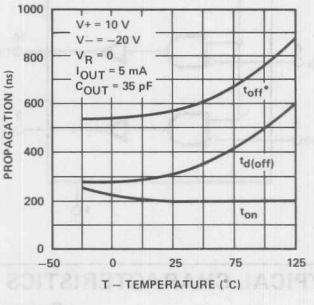
I_{IN} vs V_{IN}



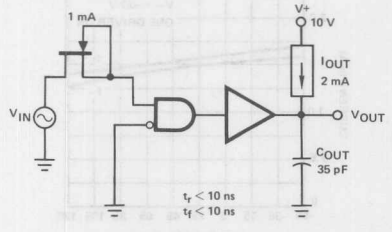
$t_{d(off)}$ vs $I_{IN(PEAK)}$

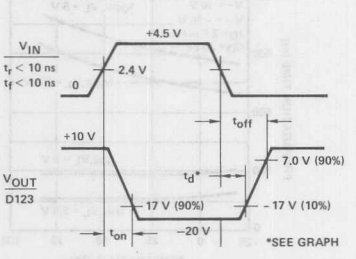


Propagation vs Temperature



SWITCHING TIME TEST CIRCUIT





Designed for . . .

■ Interfacing Low Level Signals to FET Switches such as G115 and G122 Series Multi-Channel FET Switches

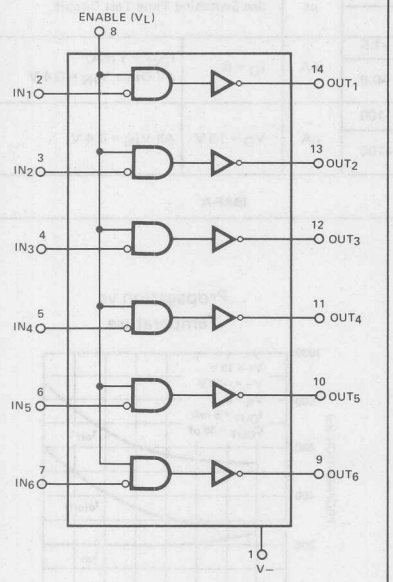
BENEFITS

- **Reduces System Component Requirements**
 - Six Interface Circuits in One Chip
 - Performs Amplification and DC Level Shifting
- **Required Between Low Level Logic and FET Switches**

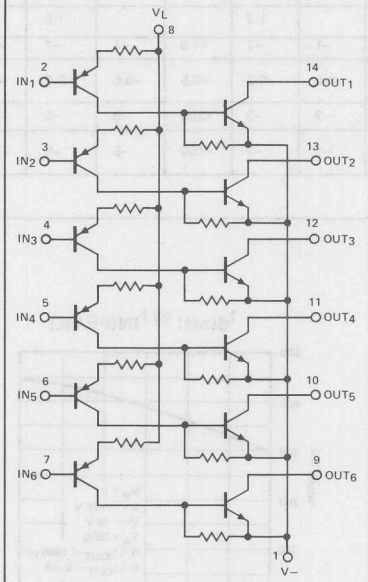
DESCRIPTION

The D125 contains six drivers, designed to perform the level-shifting and amplification needed to interface low-level logic outputs and field-effect transistor switches (MOS FET or JFET). With the input logic supply, V_L, at 5 V, the driver output reference, V– may be set between –1 and –25 V. Each output is designed to sink 5 mA of current in the ON condition, and to hold off up to 30 V in the OFF condition. The input stage is a base-input PNP transistor, with the emitter returned to the V_L supply through a resistor. To turn the driver ON, the logic stage driving it must be capable of sinking 0.7 mA.

FUNCTIONAL DIAGRAM

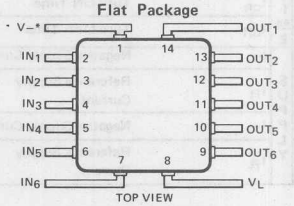


SCHEMATIC DIAGRAM



PIN CONFIGURATIONS

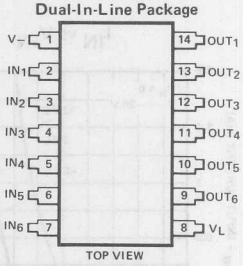
Flat Package



ORDER NUMBER:
D125AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

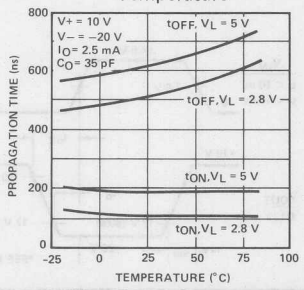
Dual-In-Line Package



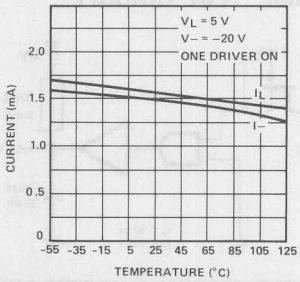
ORDER NUMBERS:
D125AP OR D125BP
SEE PACKAGE 11

TYPICAL CHARACTERISTICS

Propagation vs Temperature



Supply Current vs Temperature



V_{IN} to V_L	±6 V
Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C

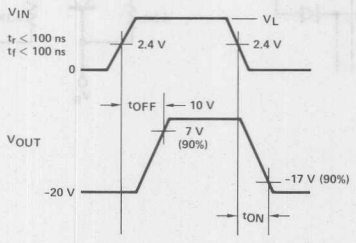
ELECTRICAL CHARACTERISTICS

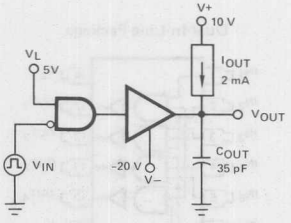
All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS D125A −55°C	D125A 25°C	D125A 125°C	D125B −20°C	D125B 25°C	D125B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V− = −20 V, V_L = 5 V	
1	OUT	V_{OL}	Output Voltage, Low	−19.6	−19.6	−19.5	−19.6	−19.6	−19.5	V	I_O = 5 mA, V_L = 4.5 V, V_{IN} = 0.5 V	
2	OUT	I_{OH}	Output Current, High	0.1	0.1	10	0.1	0.1	10	µA	V_O = 10 V, V_{IN} = 4.6 V	
3	IN	I_{INH}	Input Current, Input Voltage High	±1	±1	±10	±10	±10	±20	µA	V_{IN} = 4.6 V	
4	IN	I_{INL}	Input Current, Input Voltage Low	−0.7	−0.7	−0.7	−1	−1	−1	mA	V_{IN} = 0	
5	TIME	t_{on}	Turn-ON Time		0.5			0.5		µs	See Switching Time Test Circuit	
6	TIME	t_{off}	Turn-OFF Time		1.2			1.5		µs	See Switching Time Test Circuit	
7	SUPPLY	I−	Negative Supply Current	−2.5	−2.5	−2.5	−2.5	−2.5	−2.5	mA	I_O = 0	V_{IN1} = 0, All Other V_{IN} = 4.6 V
8	SUPPLY	I_L	Logic Supply Current	2.5	2.5	2.5	2.5	2.5	2.5	mA	I_O = 0	V_{IN1} = 0, All Other V_{IN} = 4.6 V
9	SUPPLY	I−	Negative Supply Current	−2	−2	−200	−2	−2	−100	µA	V_O = 10 V	All V_{IN} = 4.6 V
10	SUPPLY	I_L	Logic Supply Current	1	1	100	2	2	100	µA	V_O = 10 V	All V_{IN} = 4.6 V

IBAF-B

SWITCHING TIME TEST CIRCUIT





4-Channel MOS FET Switch Driver with Decode

Siliconix

designed for . . .

- **Interfacing Low Level Signals to FET Switches such as G115 and G123 Series Multi-Channel FET Switches**

BENEFITS

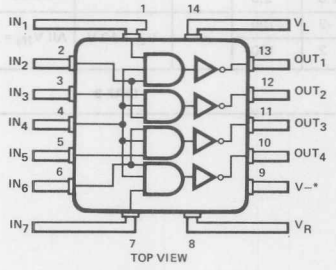
- **Reduces System Component Requirements**
 - Four Interface Circuits in One Chip
- **Easily Interfaced**
 - Inputs Compatible with Low Power TTL and DTL I_F = 200 μA Max
 - Output Current Sinking Capability 10 mA

DESCRIPTION

The D129 is a four-channel driver designed to provide the DC level-shifting and amplification functions needed to interface low-level logic outputs (0.7 to 2.2 V) and field-effect transistor switch inputs (up to 50 V peak-to-peak). With an input logic supply of 5 V, the output transistor emitter, V−, may be set at any voltage between −5 and −30 V. In the ON state, the output collector will sink up to 10 mA of current, and in the OFF state will hold off voltages up to 50 V above V−. Each of the four drivers has a 3-input logic gate, with each of the inputs either open or at positive logic "1", the driver will be ON. With any of the inputs either grounded or at positive logic "0", the driver will be OFF. Some of the logic inputs to the four gates are internally connected to facilitate decoding from a binary counter; however, one input to each gate provides a means for independent operation of each driver, if desired.

PIN CONFIGURATIONS

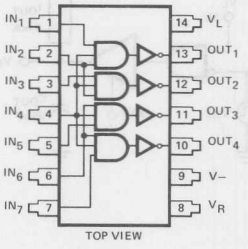
Flat Package



ORDER NUMBER: D129AL
SEE PACKAGE 5

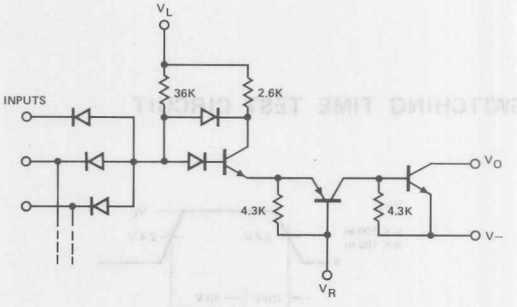
*Common to Substrate and Base of Package

Dual-In-Line Package



ORDER NUMBERS: D129AP OR D129BP
SEE PACKAGE 11

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_O to V– (A Suffix)	50 V
V_O to V– (B Suffix)	36 V
V_R to V– (A Suffix)	33 V
V_R to V– (A Suffix)	24 V
V_L to V_R	8 V
V_{IN} to V_R	±6 V
V_{IN} to V_{IN} (Any Other V_{IN} Terminals)	6 V
Current (Any Terminal)	30 mA
Storage Temperature	–65 to 150°C
Operating Temperature (A Suffix)	–55 to 125°C
(B Suffix)	–20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads soldered or welded to PC board.
**Derate 10 mW/°C above 75°C
***Derate 11 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

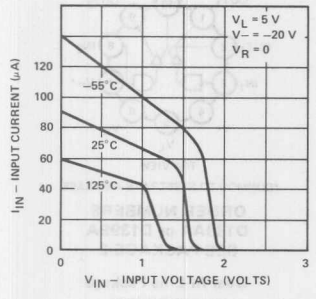
		CHARACTERISTIC		MAX LIMITS D129A –55°C	D129A 25°C	D129A 125°C	D129B –20°C	D129B 25°C	D129B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V– = –20 V, V_R = 0, V_L = 5 V	
1	OUT	V_{OL}	Output Voltage, Low	–19.3	–19.3	–19	–19.25	–19.25	–19	V	I_O = 10 mA	V_{IN} = 2.2 V, V_L = 4.5 V
2	OUT	V_{OL}	Output Voltage, Low	–19.8	–19.8	–19.75				V	I_O = 1 mA	V_{IN} = 2.2 V, V_L = 4.5 V
3	OUT	I_{OH}	Output Current, High	0.1	0.1	20	0.2	0.2	10	µA	V_O = 10 V, V_{IN} = 0.7 V	
4	IN	I_{INH}*	Input Current, Input Voltage High	0.25	0.25	5	1	1.0	5	µA	V_{IN} = 5 V Input Under Test, V_{IN} = 0 All Other Inputs	
5	IN	I_{INL}*	Input Current, Input Voltage Low	–250	–200	–160	–250	–225	–200	µA	V_{IN} = 0, V_L = 5.5 V	
6	TIME	t_{on}	Turn-ON Time		0.3			0.3		µs	See Switching Time Test Circuit	
7	TIME	t_{off}	Turn-OFF Time		1.5			1.5		µs	See Switching Time Test Circuit	
8	SUPPLY	I–	Negative Supply Current		–2			–2.25		mA	V– = –20 V, V_L = 5.5 V	One Channel "ON"
9	SUPPLY	I_L	Logic Supply Current		3			3.3		mA	V– = –20 V, V_L = 5.5 V	One Channel "ON"
10	SUPPLY	I–	Negative Supply Current		–10			–25		µA	V– = –20 V, V_L = 5.5 V	All V_{IN} = 0, All Channels "OFF"
11	SUPPLY	I_L	Logic Supply Current		0.75			1		mA	V– = –20 V, V_L = 5.5 V	All V_{IN} = 0, All Channels "OFF"

*Per gate input

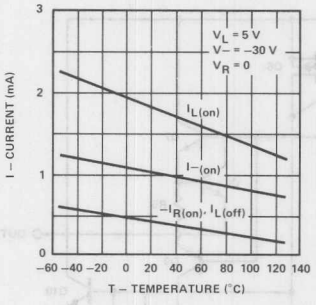
IBAD-A

TYPICAL CHARACTERISTICS

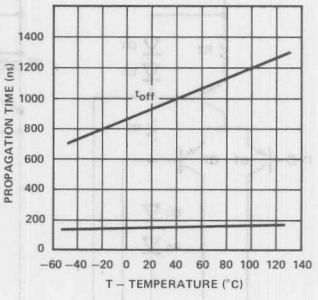
I_{IN} vs V_{IN}



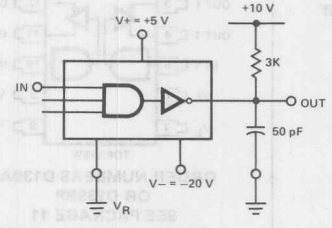
Current vs Temperature

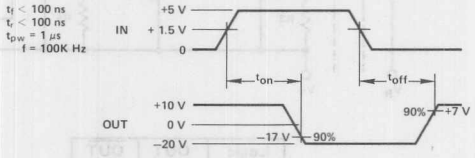


Propagation vs Temperature



SWITCHING TIME AND TEST CIRCUIT





Monolithic 2-Channel FET Switch Driver

Siliconix

designed for . . .

- **Interfacing Low Level Signals to FET Switches**
- **Interfacing TTL to CMOS**
- **Interface from TTL to Other Logic Levels, i.e. PROM Program Levels**

BENEFITS

- **Easily Interfaced**
 - TTL, DTL and RTL Compatible
- **Minimizes Switching Time**
 - 150 ns Typical Propagation Time
- **Versatile**
 - Complementary Outputs
 - Up to 30 V Output Swing

DESCRIPTION

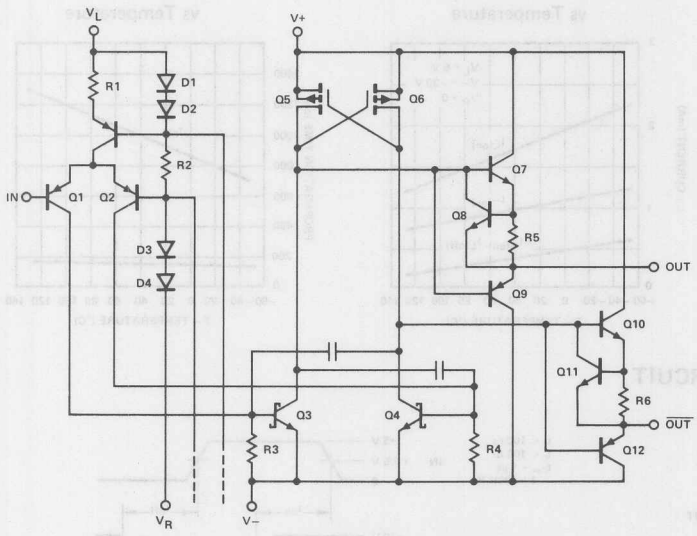
The D139 is a dual low level to high level voltage translator with complementary outputs. Uses include bipolar to MOS logic interface and bipolar logic to FET analog switch control.

The following characteristics of the input circuit provide an ideal interface to the common logic forms TTL, CMOS, and DTL: light loading (≈ 1/3 TTL load) to "0" inputs, a 1.2 V trip point, and high input impedance with high breakdown to "1" inputs.

The output can drive up to 30 V peak-to-peak into pure capacitive loads or moderate resistive loads. Current source coupling between the input and output and split power supplies allow wide flexibility in the actual output voltage levels. Complementary outputs permit maximum application versatility, allowing functions such as double-throw analog switch control.

A positive logic "1" at the input provides a "1" at OUT and a "0" at $\overline{\text{OUT}}$.

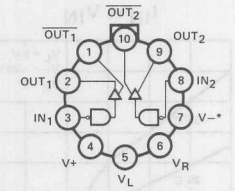
SCHEMATIC DIAGRAM (Typical Channel)



Logic	OUT	$\overline{\text{OUT}}$
0	V−	V+
1	V+	V−

PIN CONFIGURATIONS

Metal Can Package

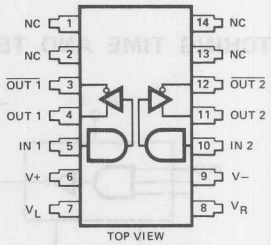


TOP VIEW

*COMMON TO SUBSTRATE AND CASE

ORDER NUMBERS
D139AA or D139BA
SEE PACKAGE 2

Dual-In-Line Package



TOP VIEW

ORDER NUMBERS D139AP
OR D139BP
SEE PACKAGE 11
ORDER NUMBER D139CJ
SEE PACKAGE 7

ABSOLUTE MAXIMUM RATINGS

$V+$ to $V-$ 36 V
$V+$ to V_R 36 V
$V+$ to V_O 36 V
V_L to V_R 8 V
V_{IN} to V_R 8 V
V_R to $V-$ 36 V
V_L to $V-$ 36 V
V_O to $V-$ 36 V
V_L to V_{IN} 8 V
Current (Any Terminal) DC 12 mA
Peak (Any Terminal) 100 mA
(200 μs pulse width, 100 pps)
Operating Temperature
(A Suffix) −55 to 125°C
(B Suffix) −20 to 85°C
(C Suffix) 0 to 70°C

Storage Temperature
(A & B Suffix) −65 to 150°C
(C Suffix) −65 to 125°C
Power Dissipation (L Package)* 750 mW
(P Package)* 825 mW
(J Package)* 470 mW
Thermal Resistance (θ_{JA}, J Package) . . . 0.16°C/mW

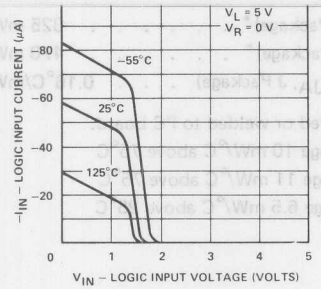
*All leads soldered or welded to PC board.
Derate L package 10 mW/°C above 75°C
Derate P package 11 mW/°C above 75°C
Derate J package 6.5 mW/°C above 25°C

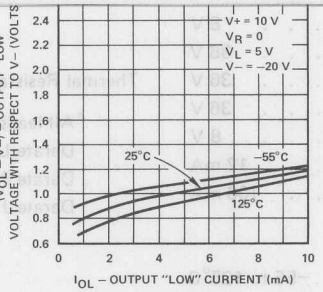
ELECTRICAL CHARACTERISTICS

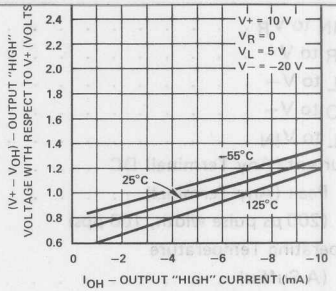
All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

	CHARACTERISTIC		D139AA/AP (MIN)/MAX LIMITS			D139BA/BP (D139CJ) (MIN)/MAX LIMITS			UNIT	TEST CONDITIONS, UNLESS NOTED: $V+ = 10$ V, $V_L = 5$ V, $V- = -20$ V, $V_R = 0$	
			−55°C	25°C	125°C	−20°C (0°C)	25°C	85°C (70°C)			
1	$V_{OH}/V_{\overline{OH}}$	Output Voltage, High ($V+$ to V_O)	1.1	0.9	0.7	1.1	0.9	0.7	V	$I_{OUT} = -10\ \mu A$	V_{IH} = 2 V for $V_{OH}/V_{\overline{OL}}$, V_{IL} = 0.8V for $V_{\overline{OH}}/V_{OL}$
2			1.5	1.5	1.5	1.5	1.5	1.5		$I_{OUT} = -2$ mA	
3	$V_{OL}/V_{\overline{OL}}$	Output Voltage, Low (V_O to $V-$)	1.3	1.1	0.9	1.3	1.1	0.9		$I_{OUT} = 10\ \mu A$	
4			1.5	1.5	1.5	1.5	1.5	1.5		$I_{OUT} = 2$ mA	
5	I_{INH}	Input Current, Input Voltage High		10	20		10	20	μA	$V_{IN} = 5$ V	
6	I_{INL}	Input Current, Input Voltage Low	(−600)	(−500)	(−500)	(−600)	(−500)	(−500)		$V_{IN} = 0$	
7	$t_{(+)}$	Switching Time, Low to High, Delay Plus Rise Time		170			170		ns	See Switching Time Test Circuit (C_L = 35 pF)	
8	$t_{(-)}$	Switching Time, High to Low, Delay Plus Fall Time		200			200				
9	$I+$	Positive Supply Current		0.1			0.1		mA	Input Voltage High or Input Voltage Low	
10	I_L	Logic Supply Current		4.0			4.0				
11	$I-$	Negative Supply Current		−3.0			−3.0				
12	I_{RH}	Reference Supply Current Input Voltage High		(−1.6)			(−1.6)			$V_{IN1} = V_{IN2} = 5$ V	
13	I_{RL}	Reference Supply Current, Input Voltage Low		(−1.1)			(−1.1)			$V_{IN1} = V_{IN2} = 0$ V	

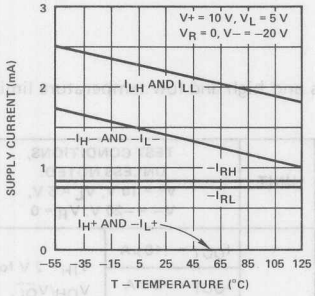
CMOA



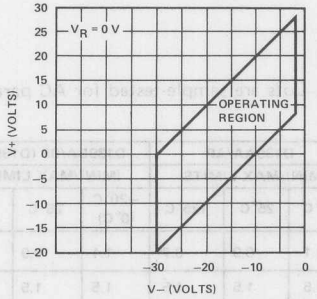




Supply Current vs Temperature



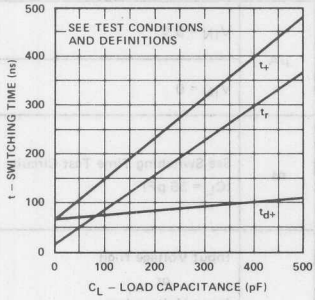
Selecting V+ and V−



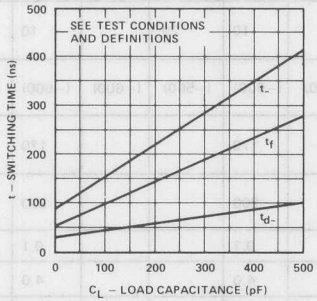
Selecting V+ and V−

The output swings between V+ and V− ($V_{OH} \cong$ V+ and $V_{OL} \cong$ V−). Select V+ and V−, within the operating region of curve at left, to provide the desired output swing. Note that V− can be −2.0 V to −30 V and V+ − V− must be at least 10 V.

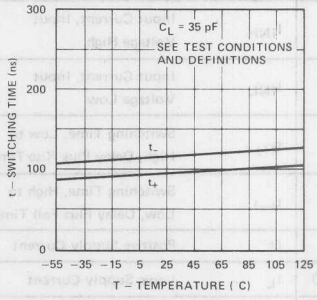
Switching Time, Low to High, vs Load Capacitance



Switching Time, High to Low, vs Load Capacitance

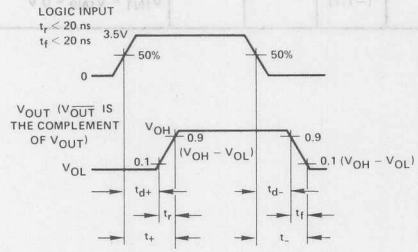


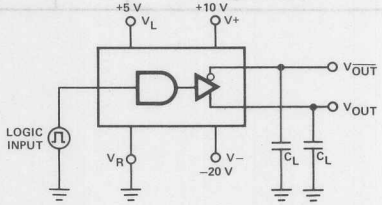
Switching Time vs Temperature



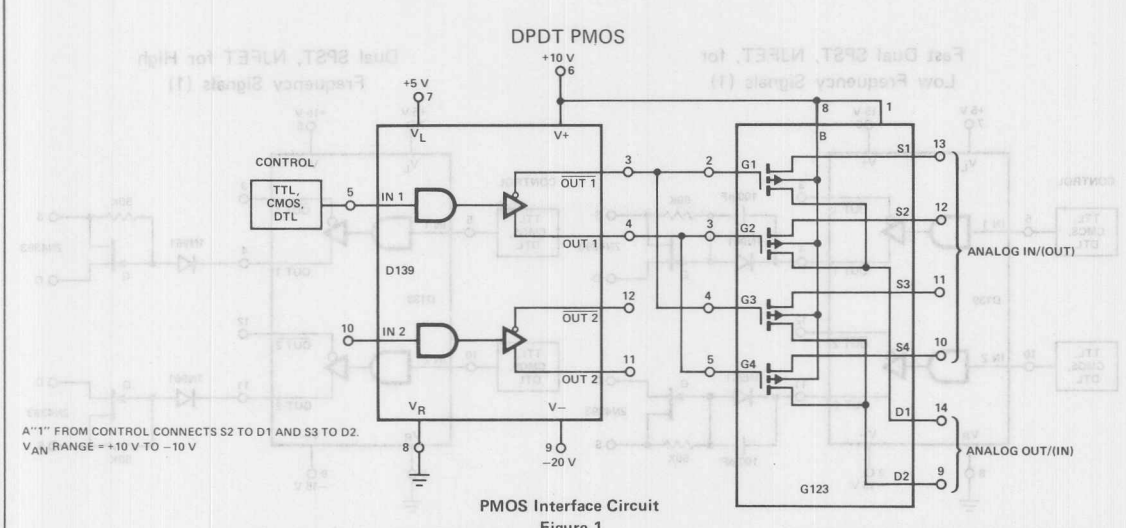
TEST CONDITIONS AND DEFINITIONS

Switching Time Test Circuit





DRIVING PMOS ANALOG SWITCHES



PMOS Interface Circuit
Figure 1

Driving PMOS Analog Switches. The D139 output swing is dictated by the analog signal range. V_{OH} is the PMOS "OFF" level and must equal the most positive analog voltage. V_{OL} is the PMOS "ON" level and must be 10 V more negative than the most negative analog voltage. Therefore for $V_{AN} = \pm 10$ V → V+ = +10 V and V− = −20 V. PMOS control is make-before-break.

PMOS LOGIC INTERFACE

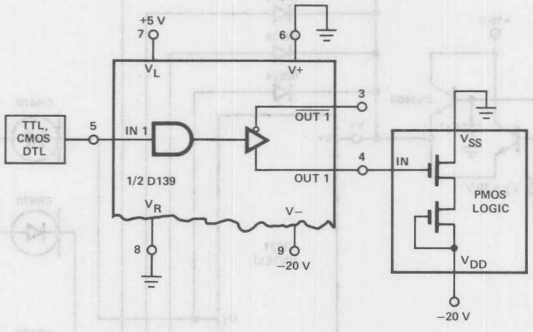


Figure 2

DRIVING NJFET ANALOG SWITCHES

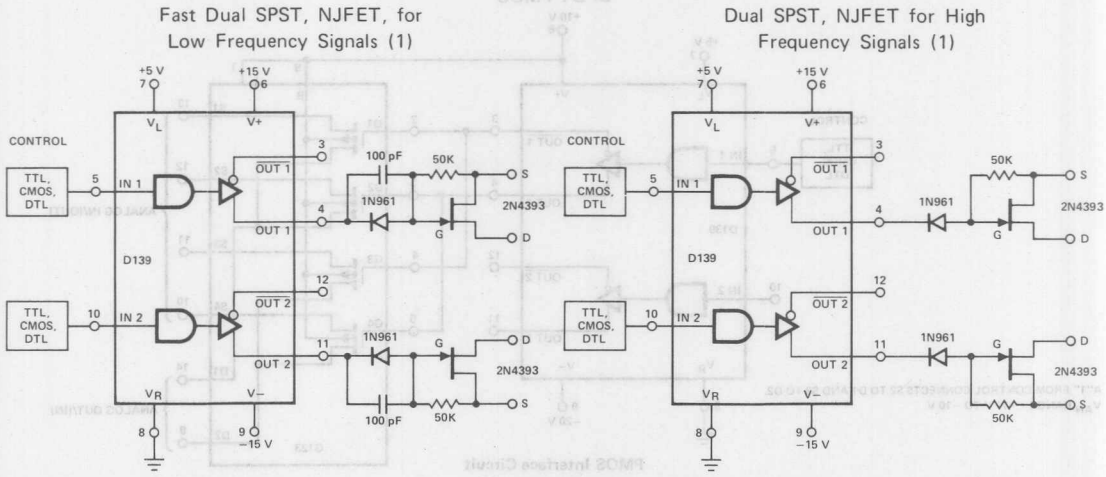
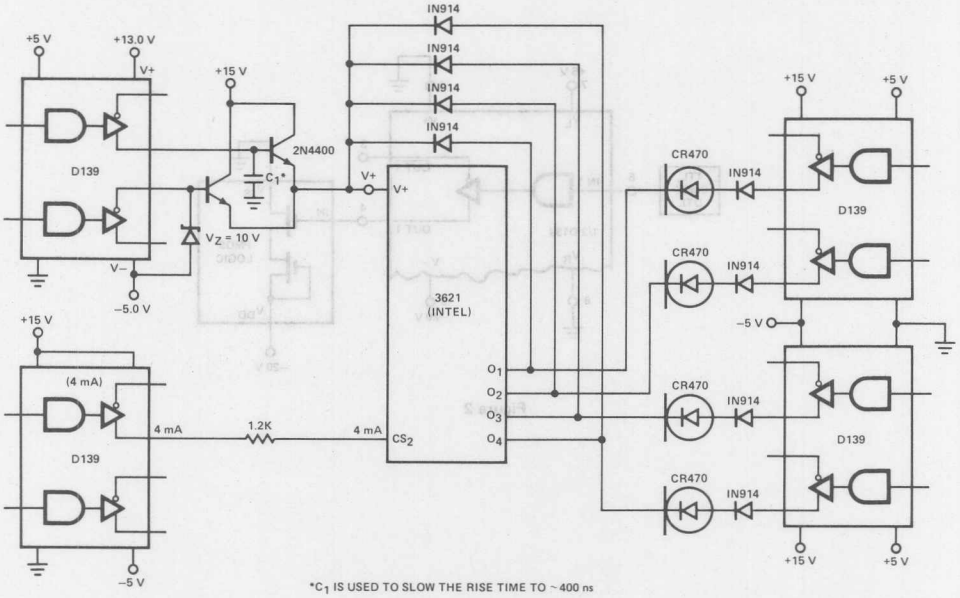


Figure 3

Driving NJFET Analog Switches. V_{OH} is the "ON" NJFET level and must be isolated from the gate by a series diode as shown above to prevent forward gate current. V_{OL} is the "OFF" NJFET level and must be more negative than the most negative analog signal voltage by ($|V_{GS(off)}|$ +2 V). NJFET control is break-before-make.

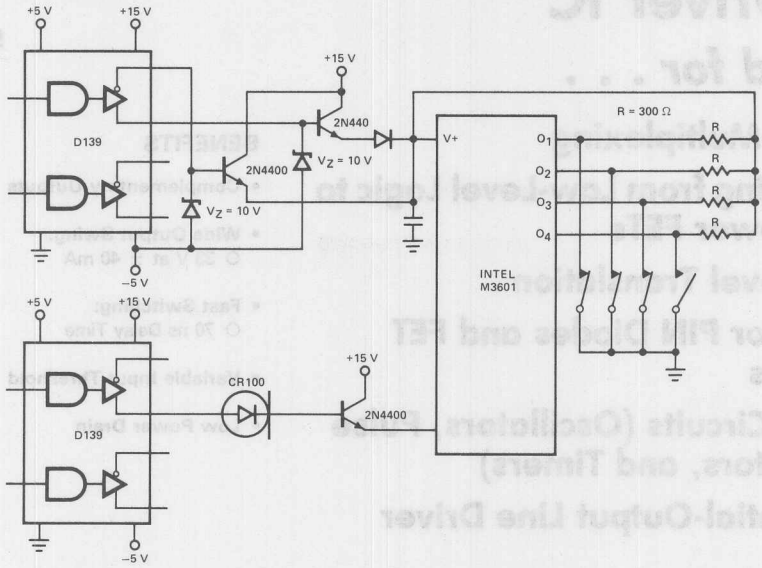
(1) See Siliconix Application Note "Driver Circuits for the J-FET Analog Switch" AN73-5, August 1973.

APPLICATIONS

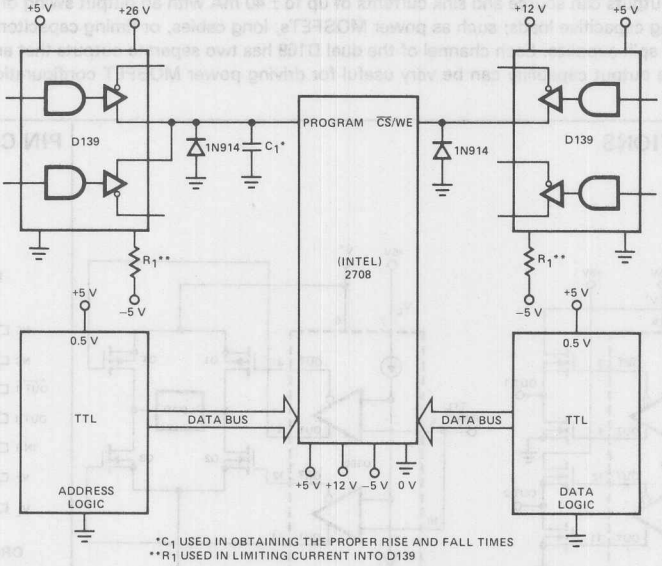


D139 Used in Programming the Intel 3621 PROM
Figure 4

APPLICATIONS (Cont'd)



D139 Used in Programming the Intel 3601 PROM
Figure 5



D139 Used in Programming the Intel 2708 PROM
Figure 6

D139 2-Channel Interface. The D139 may be used to interface 0.5 V TTL to CMOS Logic by setting V_L, V_R, V+ and V– to the proper levels. If 0 to 5 V TTL levels are to be used to control the switch, V_L should be set to 5 V and V_R grounded.

V+ and V– may be set to whatever levels are needed. The operating region of the D139 is determined by the graph of V+ vs V–.

Note. V– must be at least 2 V below V_R in order for the D139 to operate. See the V+ vs V– graph for selecting the supply voltages within the operating region.

Dual Driver IC

designed for . . .

- **Analog Multiplexing**
- **Interfacing from Low-Level Logic to MOS Power FETs**
- **Logic Level Translation**
- **Driver for PIN Diodes and FET Switches**
- **Timing Circuits (Oscillators, Pulse Generators, and Timers)**
- **Differential-Output Line Driver**

Siliconix

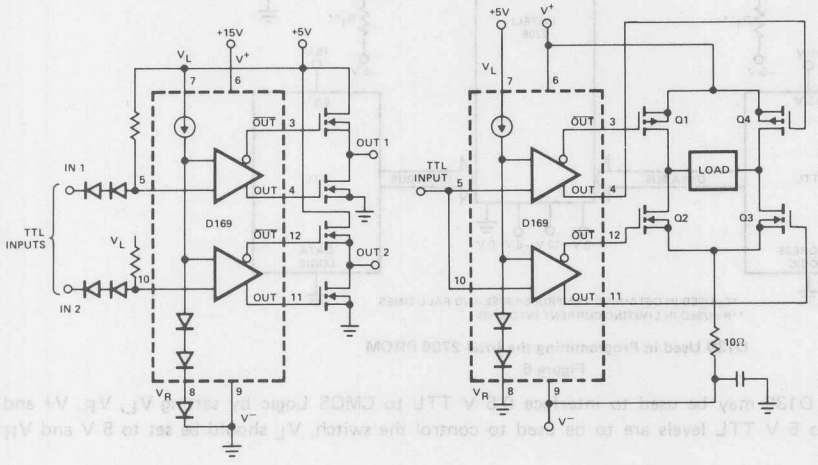
BENEFITS

- **Complementary Outputs**
- **Wide Output Swing:**
 - 33 V at ± 40 mA
- **Fast Switching:**
 - 70 ns Delay Time
- **Variable Input Threshold**
- **Low Power Drain**

DESCRIPTION

The D169 is a versatile high-voltage dual driver with complementary outputs. Low-level logic inputs can be translated up to ± 33 V output levels. A differential input stage with adjustable threshold provides high input impedance and easy interfacing to low-level logic or analog inputs. Current-source coupling to the output stage allows wide flexibility in output voltage levels. The complementary emitter-follower outputs can source and sink currents of up to ± 40 mA with an output swing of up to 33 V. This output stage is excellent for driving capacitive loads; such as power MOSFETs, long cables, or timing capacitors. The output stage can be operated from single or split supplies. Each channel of the dual D169 has two separate outputs that are complementary (OUT and $\overline{OUT}$). This two-phase output capability can be very useful for driving power MOSFET configurations.

TYPICAL APPLICATIONS



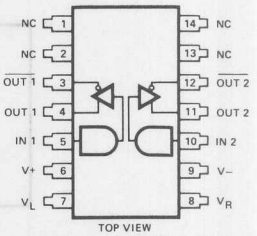
Driver for Dual Totem-Pole VMOS Switches

Driver for VMOS H-Switch

Figure 1

PIN CONFIGURATIONS

Dual-In-Line Package



TOP VIEW

ORDER NUMBERS D169AP
SEE PACKAGE 11
D169AK OR D169CK
SEE PACKAGE 9
D169CJ
SEE PACKAGE 7

LOGIC	OUT	$\overline{OUT}$
0	V−	V+
1	V+	V−

ABSOLUTE MAXIMUM RATINGS

V^+ to V^-, V^+ to V_R, and V^+ to V_O 36 V
V_L to V_R, V_{IN} to V_R, and V_L to V_{IN} 10 V
V_R to V^-, V_L to V^-, and V_O to V^- 36 V
Current (Any Terminal) DC 40 mA
Peak (Pulsed 1 ms, 10% Duty Cycle) 150 mA
Operating Temperature—"A" Suffix
(A Suffix) −55 to 125°C
(C Suffix) 0 to 70°C
Storage Temperature
(A Suffix) −65 to 150°C
(C Suffix) −65 to 125°C

Power Dissipation
"P" Package* 825 mW
"J" Package* 470 mW
Thermal Resistance (θ_{JA}, J Package) 0.16°C/mW

*All leads soldered or welded to PC board. Derate P package 11 mW/°C above 75°C. Derate J package 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

	CHARACTERISTIC		25°C TYP†	D169AP MAX LIMITS −55°C	D169AP MAX LIMITS 25°C	D169AP MAX LIMITS 125°C	D169CJ MAX LIMITS 0°C	D169CJ MAX LIMITS 25°C	D169CJ MAX LIMITS 70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V_L = 5 V, V− = −15 V, V_R = 0	
1	$V_{OH}/V_{\overline{OH}}$	Output Voltage, High (V+ to V_O)	0.7	1.1	1.0	1.0	1.1	1.0	1.0	V	I_{OUT} = 1 mA	V_{IH} = 2 V for $V_{OH}/V_{\overline{OL}}$, V_{IL} = 0.8 V for $V_{\overline{OH}}/V_{OL}$
2			1.5	2.5	2.5	3.1	2.5	2.5	3.1		I_{OUT} = 40mA	
3	$V_{OL}/V_{\overline{OL}}$	Output Voltage, Low (V_O to V−)	−.75	−1.2	−1.2	−1.2	−1.2	−1.2	−1.2		I_{OUT} = 1 mA	
4			−2.2	−3.0	−3.0	−4.0	−3.0	−3.0	−4.0		I_{OUT} = 40 mA	
5	I_{INH}	Input Current, Input Voltage High	1.0		5.0	5000		5.0	200	nA	V_{IN} = 3 V	
6	I_{INL}	Input Current, Input Voltage Low	−25	−100	−50	−50	−70	−50	−50	μA	V_{IN} = 0	
7	$t_{(+)}$	Switching Time, Low to High, Delay Plus Rise Time	100		170			170		ns	See Switching Time Test Circuit (C_L = 35 pF)	
8	$t_{(-)}$	Switching Time, High to Low, Delay Plus Fall Time	130		200			200				
9	V_{XO}	Switching Crossover Level	.9							V	200 pF Load	
10	I+	Positive Supply Current	—		0.1			0.1		mA	No Load, $V_{IN1} = V_{IN2}$ = 0V	
11	I_L	Logic Supply Current	3.2		4.0			4.0				
12	I−	Negative Supply Current	−2.2		−3.0			−3.0				
13	I_R	Reference Supply Current	1.0		1.5			1.5				

†Typical values are for Design Aid only, not guaranteed and not subject to production testing.

CMOB

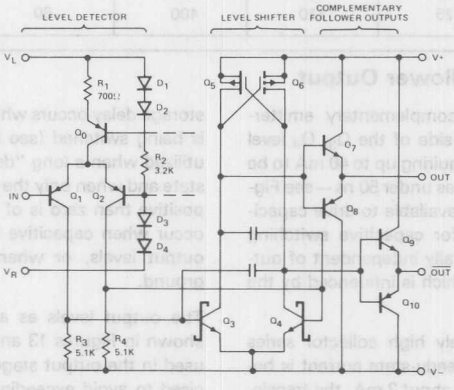


Figure 2. Schematic Diagram, One Channel

TEST CONDITIONS

TEST	V_L	V_R	V^+	V^-	C_L	R_L	V_{IN} V_{IL}	V_{IN} V_{IH}	WAVE-FORMS
1	5.0V	0.7V	10V	0	200 pF	–	1.0V	3.5V	A
2	5.0V	0.7V	15V	0	0	510 Ω	1.0V	3.5V	B
3	5.0V	0.7V	10V	0	200 pF	–	1.0V	3.5V	B
4	5.0V	0.7V	10V	0	1000 pF	–	1.0V	3.5V	B
5	5.0V	0	15V	−15V	200 pF	–	0	3.5V	B
6	5.0V	0	15V	−15V	1000 pF	–	0	3.5V	B

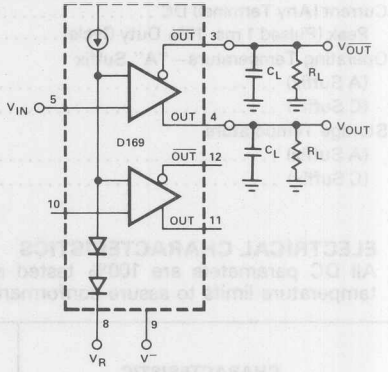
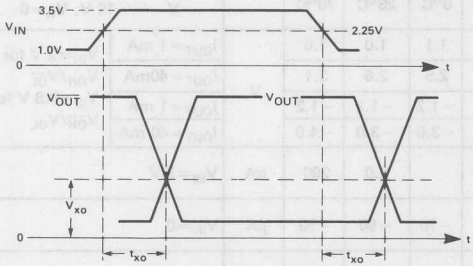
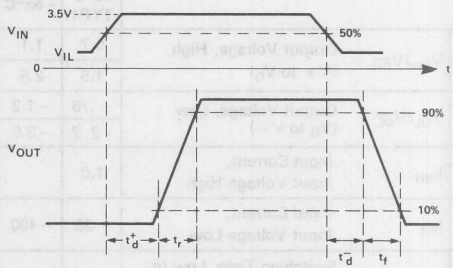


Figure 17. Switching Test Circuit



WAVEFORMS A



WAVEFORMS B

Table 1.

Test Conditions	Test 2 (Fig. 17)	Tests 5 & 6 (Fig. 17)		Tests 3 & 4 (Fig. 17)		Units
	Resistive, I_O = 25 mA	V^+ = +15V, V^- = −15V Capacitive Load		V^+ = +15V, V^- = 0 Capacitive Load		
		200 pF	1000 pF	200 pF	1000 pF	
	Typ	Typ	Typ	Typ	Typ	
Low-to-High						
Delay Time, t_d^+	70	95	220	110	230	ns
Rise Time, t_r^+	35	60	240	55	200	ns
High-to-Low						
Delay Time, t_d^-	50	50	80	55	80	ns
Fall Time, t_f^-	25	110	400	80	275	ns

Complementary Emitter-Follower Output

Transistors Q_7 through Q_{10} form complementary emitter-follower outputs connected to each side of the Q_3, Q_4 level shifter. This permits resistive loads requiring up to 40 mA to be driven at high speeds (rise and fall times under 50 ns — see Figure 10). Also high peak currents are available to drive capacitive loads (see Figures 11 and 12 for capacitive switching data). The switching times are generally independent of output swing, except for the fall time which is influenced by the negative rail, V^-.

The PNP transistors have a relatively high collector series resistance. Consequently, when a steady-state current is being drawn by the PNP which exceeds about 2 mA, the transistor becomes saturated and minority carrier storage takes place in the base and collector regions. Upon a change of state, a storage delay occurs which can be substantial if a large current is being switched (see Figures 6 and 16). This delay can be utilized when a long "dead time" is needed during change of state and when only the portion of the voltage waveform more positive than zero is of interest. This storage delay does not occur when capacitive loads are being driven, regardless of output levels, or when the load and V^- are returned to ground.

The output levels as a function of DC output current are shown in Figures 13 and 14. Note that no current limiting is used in the output stages. Consequently, care must be exercised to avoid exceeding the maximum current rating of the device.

TYPICAL CHARACTERISTICS

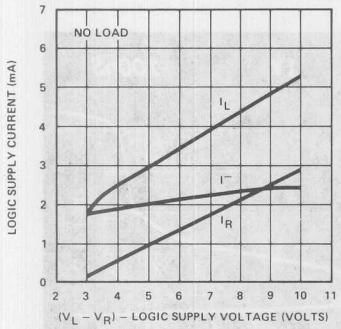


Figure 3. Supply Current Variation with Logic Supply

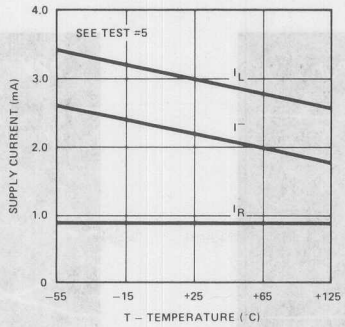


Figure 4. Effect of Temperature on Supply Currents

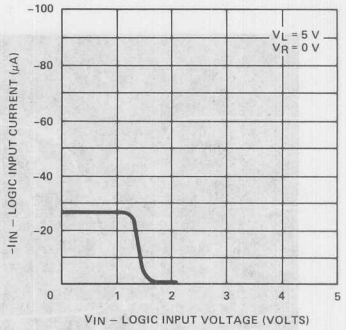


Figure 5. Logic Input Current vs. Logic Input Voltage

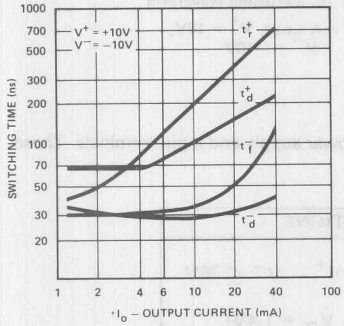


Figure 6. Switching Times with Resistive Load

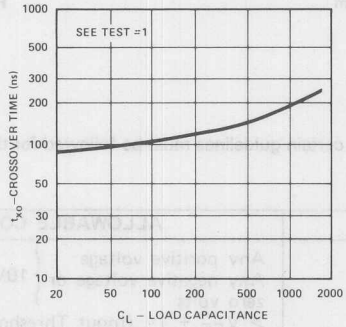


Figure 7. Effect of Load Capacitance on Crossover Time

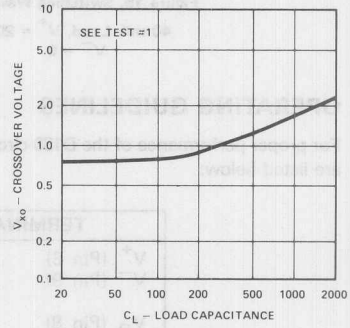


Figure 8. Effect of Load Capacitance on Crossover Level

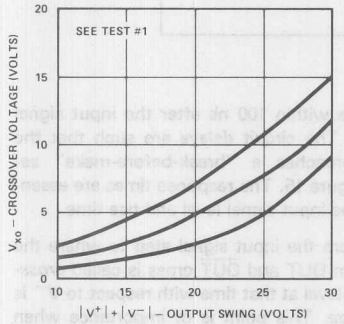


Figure 9. Effect of Voltage Output on Crossover Level

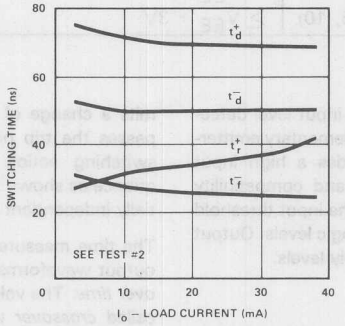


Figure 10. Resistive Load Switching

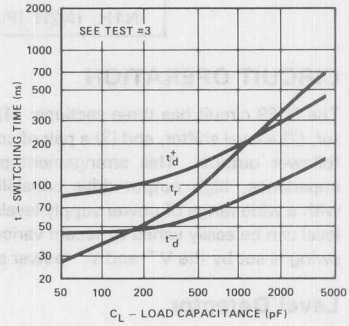


Figure 11. Switching Times with Capacitive Load

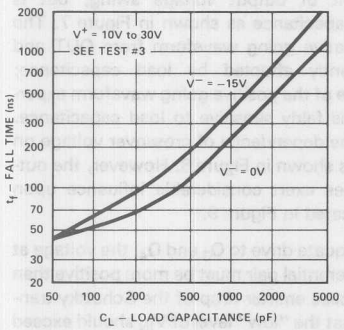


Figure 12. Fall Time with Capacitive Load

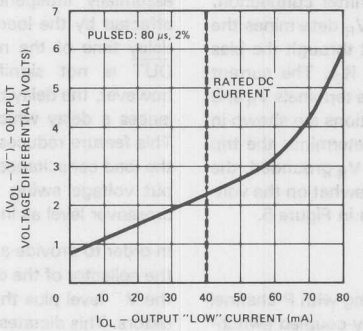


Figure 13. Output "Low" Characteristic

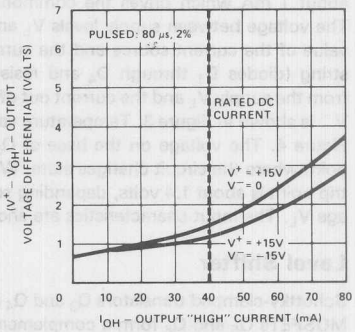


Figure 14. Output "High" Characteristic

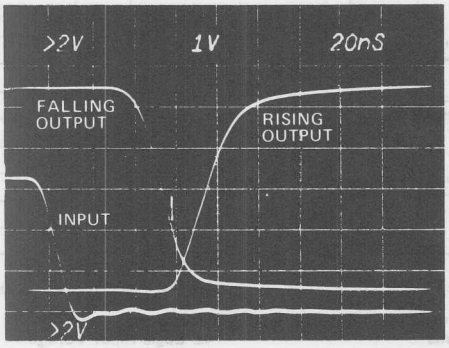


Figure 15. Switching Waveform
40 mA Load, $V^+ = 20V$, $V^- = 0$

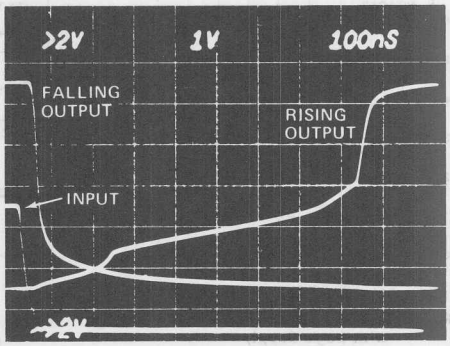


Figure 16. Switching Waveform
±40 mA Load, $V^+ = 10V$, $V^- = -10V$

OPERATING GUIDELINES

For proper performance of the D169 circuit, certain guidelines must be followed for the power supply and input terminals. These are listed below:

TERMINAL	ALLOWABLE CONDITIONS
V^+ (Pin 6) V^- (Pin 9)	Any positive voltage Any negative voltage or zero volts } $10V \leq V^+ - V^- \leq 36V$
V_R (Pin 8)	$\geq V_{EE} + 1V$ (Input Threshold = $V_R + 1.4V$)
V_L (Pin 7)	$V_L - V_R \geq 4V$
IN1L, IN2L (Pins 5, 10)	$\geq V_{EE} + 1V$
IN1H, IN2H (Pins 5, 10)	$\geq V_{EE} + 3V$

CIRCUIT OPERATION

The D169 circuit has three sections: (1) an input level detector, (2) a level shifter, and (3) a pair of complementary emitter-follower outputs. This arrangement provides a high input impedance, high output drive capability, and compatibility with a wide range of power supply levels. The input threshold level can be easily varied to accept various logic levels. Output swing is set by the V^+ and V^- power supply levels.

Level Detector

Transistors Q_1 and Q_2 form a differential input pair. Transistor Q_0, resistor R_1, and diodes D_1, D_2 form a current source of about 1 mA which drives the common emitter connection. The voltage between supply levels V_L and V_R determines the value of the current source and the current through the bias string (diodes D_1 through D_4 and resistor R_2). The current from the supply V_L and the current out of the terminals V_R and V^- is shown in Figure 3. Temperature variations are shown in Figure 4. The voltage on the base of Q_2 determines the trip point where the circuit changes state. With V_R grounded, the trip point is about 1.4 volts, depending somewhat on the voltage V_L. The input characteristics are shown in Figure 5.

Level Shifter

Schottky-clamped transistors Q_3 and Q_4 along with P-channel MOSFETs Q_5 and Q_6 form a complementary-coupled switching stage. This configuration draws no idle current and permits a change of state within 100 ns after the input signal passes the trip point. The circuit delays are such that the switching action approaches a "break-before-make" sequence as shown in Figure 15. The response times are essentially independent of the input signal level and rise time.

The time measured from the input signal step to where the output waveforms from OUT and $\overline{OUT}$ cross is called *crossover time.* The voltage level at that time with respect to V^- is called *crossover voltage.* This point is of importance when driving certain loads where a break-before-make action is necessary to avoid high current surges. The crossover time is essentially independent of output voltage swing, but is affected by the load capacitance as shown in Figure 7. The delay time of the negative going waveform from OUT and $\overline{OUT}$ is not significantly affected by load capacitance; however, the delay time of the positive going waveform experiences a delay which is fairly sensitive to load capacitance. This feature reduces the dependence of crossover voltage on the load capacitance as shown in Figure 8. However, the output voltage swing does exert considerable influence upon crossover level as indicated in Figure 9.

In order to provide adequate drive to Q_3 and Q_4, the voltage at the collector of the differential pair must be more positive than the V^- level plus the base emitter drop of the Schottky transistors. This dictates that the "low" level of V_{IN} should exceed V^- by at least one volt.

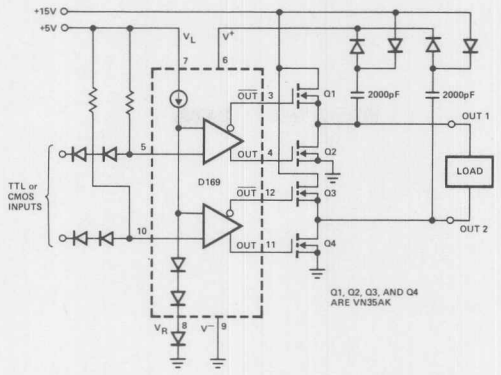


Figure 18. Totem-Pole Driver with Bootstrapping

Totem-Pole Driver with Bootstrapping

When driving VMOS in a totem-pole output configuration (see Figure 18), it is necessary to have the gate voltage 10 to 15 volts positive with respect to the source in order to handle load currents near the VMOS maximum ratings. The D169 lends itself to bootstrapping because of its high voltage ratings.

In the circuit shown, the voltage on the 2000 pF bootstrap capacitors is applied via diode "OR" gates to the V^+ terminal. Therefore, regardless of which output is high, 30 volts is present at V^+. Maximum switching frequency is determined by the input capacitance of the VMOS transistors used.

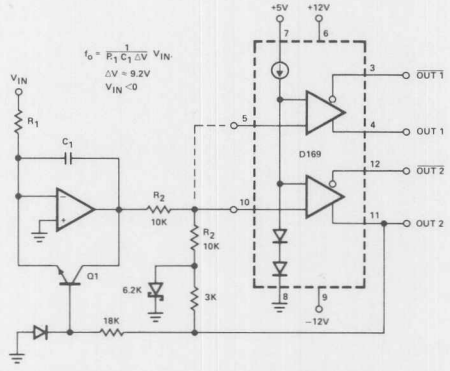


Figure 19. D169 Used as a Voltage-to-Frequency Converter

Voltage-to-Frequency Converter

A simple, low-cost VFC can be designed using the D169 and a single op amp (see Figure 19). The D169 serves as a level detector and provides complementary outputs. The op amp is used to integrate the input signal V_{IN} with a time constant of R_1C_1. The input, which must be negative, causes a positive ramp at the output of the integrator which is then summed with a negative zener voltage. When the ramp is positive enough to cause the D169 input (pin 10) to exceed the logic threshold of 1.4 V, then the D169 outputs change state and OUT 2 flips from negative to positive. This positive output of approximately 11 V puts transistor Q_1 into saturation which then resets the integrator to near zero. The integrator peak differential voltage ΔV will be approximately 9.2 V. The output frequency f_o, neglecting the short reset interval, will be

$$f_o = \frac{1}{R_1 C_1 \Delta V} V_{IN},\ V_{IN} < 0$$

The pulse repetition rate, f_o, is directly proportional to the negative input voltage V_{IN}.

Totem-Pole Driver with Bootstrapping

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Voltage-to-Frequency Converter

A simple, low-cost VFC can be designed using the DI169 and a single op amp (see Figure 19). The DI169 serves as a level detector and provides complementary outputs. The op amp is used to integrate the input signal V_{IN} with a time constant of R_1C_1. The input, which must be negative, causes a positive ramp at the output of the integrator which is then summed with a negative zener voltage. When the ramp is positive enough to cause the DI169 input (pin 10) to exceed the threshold of 1.4 V, then the DI169 outputs change state and OUT 2 flips from negative to positive. This positive output of approximately 11 V puts transistor Q_1 into saturation which then resets the integrator to near zero. The integrator peak differential voltage ΔV will be approximately 9.2 V. The output frequency f_O, neglecting the short reset interval, will be

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Siliconix

Introduction 0
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TELECOMMUNICATIONS

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DF320/320A/322	2-1
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LOOP DISCONNECT DIALERS

Product	Description	Application
DF320/DF320A/DF322	Crystal Oscillator	Replacing Conventional Rotary Dial Phones with Push Button Keyboard Phones
DF328	LC or Crystal Oscillator	

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extened periods may effect device reliability.

CMOS Loop Disconnect Dialers

Siliconix

designed for . . .

- **Push Button Telephones**
- **Repertory Dialers**
- **Telex**
- **Mobile Telephones**
- **Security and Fire Alert Systems**
- **Emergency Number Dialers**

BENEFITS

- **Eliminates the Need for Regulated Supplies**
 - 2.5 V to 5.5 V V_{DD} Range
- **Minimizes Power Consumption**
 - Standby Dissipation – 6 μW
- **Low Cost**
 - Simple Support Circuitry
 - Power On Reset
- **Minimizes External Components**
 - On Chip Circuitry for: Keyboard Debouncing; Last Number Repeat; Input Pull Up/Pull Down Terminations
- **Versatile**
 - Selectable Mark/Space Ratios, Impulsing Speeds
 - Hold Facility to Delay Impulsing
 - Fixed IDP: 8 Times Impulsing Period

DESCRIPTION

The DF320 series of monolithic CMOS Loop Disconnect Dialers each contain all the logic necessary to interface a standard double contact keyboard to a telephone system requiring loop disconnect signalling.

A dial pulsing output and two masking output options are provided to control the impulsing (loop disconnect) and muting functions. The circuit is capable of storing a number string of up to 20 digits and re-dialing this stored number automatically at a later time, initiated by a RE-DIAL input code. Impulsing mark/space ratio (M/S), and impulsing rate are pin programmable to meet most telephone authority specifications.

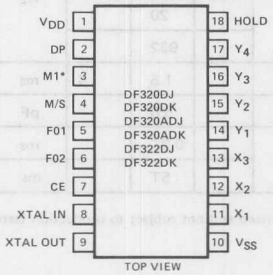
The use of Siliconix low voltage CMOS technology allows operation with an unregulated supply voltage down to a guaranteed minimum of 2.5 V. This feature, together with low operating current, negligible standby current and high noise immunity make the DF320 series easy to interface to long telephone lines.

External component count is minimized by the inclusion of an on-chip clock oscillator, high impedance pull-down terminations to programming inputs as well as pull-up terminations to the keyboard giving direct interfacing.

The DF320 provides the functions most commonly required in the push button telephone application. M1 is the masking option which remains at logic "1" throughout the dialing sequence. The DF322 is identical to the DF320 except that M2 is offered instead of M1. The M2 masking option is at logic "1" only during impulsing, allowing the telephone line to be monitored during the IDP. The DF320A has an extended post impulsing pause of 500 ms.

PIN CONFIGURATION

DUAL-IN-LINE PACKAGE



TOP VIEW

*M2 ON DF322DJ, DF322DK

ORDER NUMBERS DF320DJ, DF320ADJ OR DF322DJ
SEE PACKAGE 19
ORDER NUMBERS DF320DK, DF320ADK OR DF322DK
SEE PACKAGE 23

ABSOLUTE MAXIMUM RATINGS

*Derate 6.3 mW/°C above 25°C. All leads soldered to PC board.

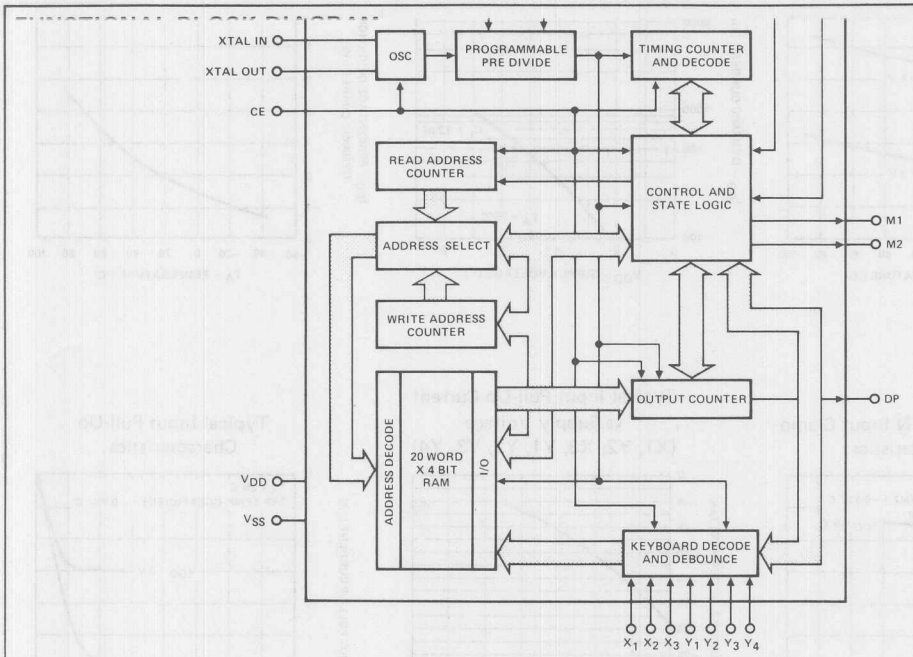
ELECTRICAL CHARACTERISTICS

All voltages referenced to V_{SS} unless otherwise noted.

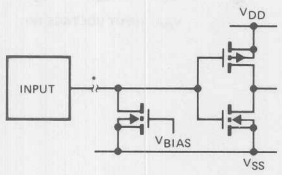
		Characteristic			Min	Typ*	Max	Units	Test Conditions Unless Noted: V_{DD} = 3.0 V, T_A = 25°C, f_{CLK} = 3.57945 MHz	
1	SUP	V_{DD}	Supply Voltage Operating Range		2.5		5.5	V		
2	SUP	I_{DSS}	Standby Supply Current			2.0	10.0	µA	CE = V_{SS}	
3	SUP	I_{DD}	Operating Supply Current			155	250	µA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12 pF	
4	INPUT	I_{IL}	Pull-Up Transistor Source Current		–0.5	–6	–10.0	µA	$V_{IN} = V_{SS}$	$X_1, X_2, X_3, Y_1, Y_2, Y_3, Y_4$
5	INPUT	I_{IH}	Input Leakage Current			0.1		nA	$V_{IN} = V_{DD}$	
6	INPUT	I_{IL}	Input Leakage Current			–0.1		nA	$V_{IN} = V_{SS}$	M/S, F01, F02, Hold
7	INPUT	I_{IH}	Pull-Down Transistor Sink Current		0.5	3.0	10.0	µA	$V_{IN} = V_{DD}$	
8	OUT	V_{IL}	Logic "0" Level				0.65	V		All Inputs
9	OUT	V_{IH}	Logic "1" Level		2.45			V		
10	OUT	V_{OL}	Voltage Levels	Low Level		0	0.01	V	No Load	DP, M1, M2
11	OUT	V_{OH}		High Level	2.99	3		V		
12	OUT	I_{OL}	Drive Current	N-Channel Sink	0.5	1.5		mA	V_{OUT} = 2.3 V	
13	OUT	I_{OH}		P-Channel Source	–0.5	1.5		mA	V_{OUT} = 0.7 V	
14	DYNAMIC	t_r	Output Rise Time			1.0		µs	DP, M1, M2, C_L = 50 pF	
15	DYNAMIC	t_f	Output Fall Time			1.0		µs		
16	DYNAMIC	f_{CLK}	Maximum Clock Frequency		3.58			MHz	3.579545 MHz Crystal	
17	DYNAMIC	M/S	Mark to Space Ratio			2:1			Note 1	
18	DYNAMIC					3:2				
19	DYNAMIC	IDP	Interdigital Pause			8T		ms	T = Selected Impulsing Period, Note 1	
20	DYNAMIC	Impulsing Rate = 1T				10		Hz	Note 1	
21	DYNAMIC					16				
22	DYNAMIC					20				
23	DYNAMIC					932				
24	DYNAMIC	t_{ON}	Clock Start Up Time			1.5	4	ms	Timed from CE = Logic "1"	
25	DYNAMIC	C_{IN}	Input Capacitance			5.0		pF	Any Input	
26	DYNAMIC	POIP	Post Impulsing Pause			0.3T		ms	DF320, DF322, DF320A	T = Selected Impulsing Period
27	DYNAMIC					5T		ms		

*Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

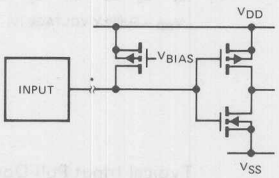
NOTES:
1. See Pin Function, Table 1



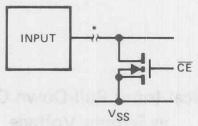
INPUT OUTPUT SCHEMATICS



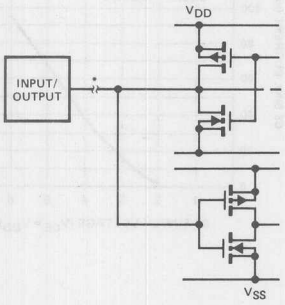
M/S, F01, F02, HOLD
Figure 1



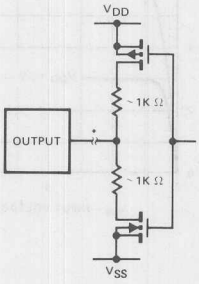
X_1, X_2, X_3, Y_1, Y_2, Y_3, Y_4
Figure 2



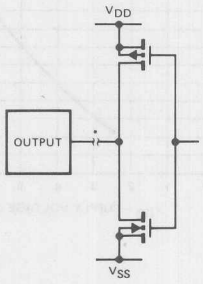
XTAL IN
Figure 3



CE
Figure 4



DP, M1, M2
Figure 5

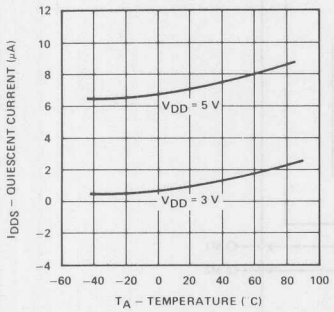


XTAL OUT
Figure 6

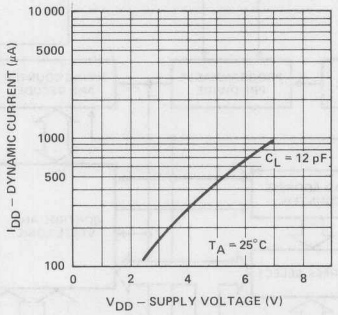
*Circuit Protection Not Shown

TYPICAL CHARACTERISTICS

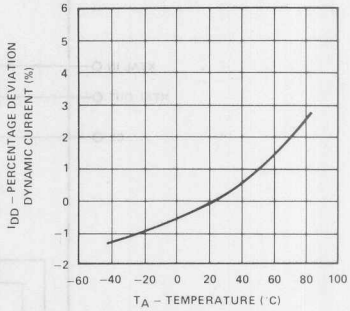
Typical Quiescent Current vs Temperature



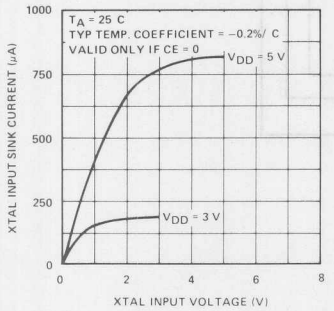
Typical Dynamic Current vs Supply Voltage



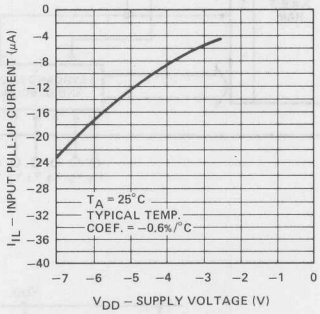
Typical Percentage Deviation of Dynamic Current vs Temperature (Normalized to 25°C)



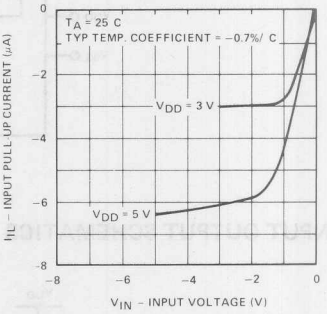
Typical XTAL IN Input Clamp Characteristics



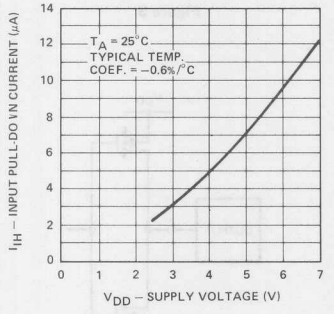
Typical Input Pull-Up Current vs Supply Voltage (X1, Y2, X3, Y1, Y2, Y3, Y4)



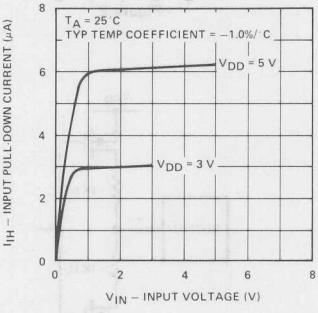
Typical Input Pull-Up Characteristics



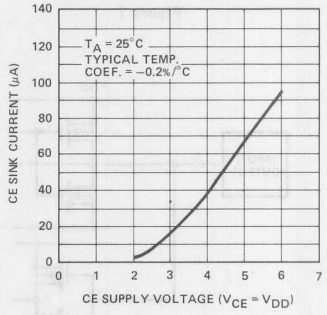
Typical Input Pull-Down Current vs Supply Voltage (M/S, FO1, FO2, Hold)



Typical Input Pull-Down Characteristics

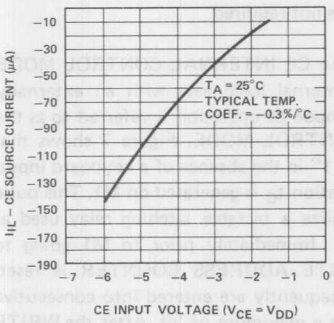


Typical CE Sink Current

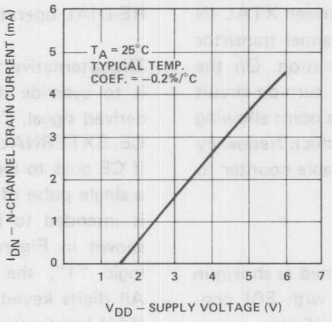


TYPICAL CHARACTERISTICS (Cont'd)

Typical CE Source Current



Typical N-Channel Output Drain Characteristics (DP, M1, M2)



Typical P-Channel Output Drain Characteristics (DP, M1, M2)

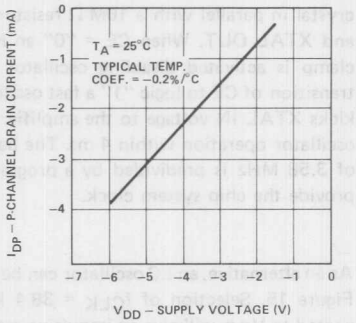


Table 1

PIN FUNCTION	DESCRIPTION
V_{DD}	Positive voltage supply
DP	Dial Pulsing Output Buffer
M1	Mask 1 (Buffered Output) = Logic "1" during Dialing Sequence
M2	Mask 2 (Buffered Output) = Logic "1" during an Impulse
M/S	Mark/Space (Break/Make) Ratio select. On-chip active pull-down to V_{SS}.

O C	2:1
V_{DD}	3:2

Note: O C = Open circuit, see Figure 7

F01, F02	Impulsing Rate Selection. On-chip active pull-down to V_{SS}.

F01	F02	Nominal Impulsing Rate	Actual* Impulsing Rate	System Clock Frequency
O C	O C	10 Hz	10.13 Hz	303.9 Hz
O C	V_{DD}	20 Hz	19.42 Hz	582.6 Hz
V_{DD}	O C	932 Hz	932.17 Hz	27,965.1 Hz
V_{DD}	V_{DD}	16 Hz	15.54 Hz	466.1 Hz

*Assumes f_{CLK} = 3.579545 MHz

CE	Chip Enable. Input/Output, left open it is internally controlled by keyboard decode logic. Can be externally forced for manually enabling chip.
XTAL IN	Crystal Input. Active, clamped low if CE = "0", high impedance if CE = "1".
XTAL OUT	Crystal Output. Buffer to drive crystal. Capacitive load on-chip.
V_{SS}	System ground
X_1, X_2, X_3	Column keyboard inputs having active pull-ups to V_{DD}. Active LOW
Y_1, Y_2, Y_3, Y_4	Row keyboard inputs having active pull-ups to V_{DD}. Active LOW
HOLD	Prevents further impulsing. On-chip active pull-down to V_{SS}

O C	Normal Operation
V_{DD}	No Impulsing. If activated during impulsing, hold occurs when the current digit is complete.

crystal in parallel with a 10M Ω resistor between XTAL IN and XTAL OUT. When CE = "0" an N-channel transistor clamp is activated, disabling oscillator operation. On the transition of CE to logic "1" a fast oscillator turn-on circuit kicks XTAL IN voltage to the amplifier bias point allowing oscillator operation within 4 ms. The basic clock frequency of 3.58 MHz is predivided by a programmable counter to provide the chip system clock.

As an alternative, an LC oscillator can be formed as shown in Figure 15. Selection of f_{CLK} = 38.4 kHz with F01 connected to V_{DD} will give an impulsing rate of 10 Hz.

It is also possible to control the DF320, DF320A, DF322 from an external clock applied to XTAL IN.

2.0 Chip Enable, CE – The Chip Enable pin is used to initialize the chip system. CE = "0" forces the chip into the static standby mode. In this mode the clock oscillator if OFF, internal registers are reset with the exception of the WRITE ADDRESS COUNTER and the circuit is ready to receive a new number or re-dial. While CE = "0" data cannot be received by the chip, but data previously entered and stored is maintained. When CE = "1" the clock oscillator is operating, the internal registers are enabled, and data can be entered from the keyboard up to a maximum of 20 digits.

CE is primarily controlled by a logic gate with function

F = KEYBOARD INPUT + M1 + HOLD

where + denotes logical OR.

To operate this gate, a resistor and capacitor should be connected in parallel between CE and V_{SS}. When the chip is used in the CE INTERNAL CONTROL MODE power ON reset occurs when V_{DD} is applied, since a logic "0" appears on the CE pin. The chip remains in the static standby condition until it receives the first valid keyboard input after V_{DD} is applied. This is statically decoded and causes CE = "1", hence enabling the clock oscillator. The debounce counter is then clocked by the system clock until the valid data condition is recognized. Data is then written into the on-chip RAM. CE is maintained at logic "1" by M1 during dialing.

The WRITE ADDRESS COUNTER is reset on recognition of the first valid debounced keyboard input provided that it is decoded during t_d of the pre-impulsing pause PIP (see Figure 8). In the CE INTERNAL CONTROL MODE this condition will always apply. When all keyed digits have been dialled, M1 goes to logic "0" and hence the chip returns to the static standby condition. If digits are sub-RE-DIAL operation is not required.

The alternative to the CE INTERNAL CONTROL MODE is to override the internal logic gate with an externally derived signal. This mode of operation is referred to as the CE EXTERNAL CONTROL MODE. Figure 7 shows that if CE goes to logic "1" in the absence of a keyboard input, a single pulse of duration t_d is generated on M1. This pulse is intended to initialize a bistable latching relay used as shown in Figure 12. Immediately prior to M1 going to logic "1", the WRITE ADDRESS COUNTER is reset. All digits keyed subsequently are entered into consecutive RAM locations up to a maximum of 20. After the WRITE ADDRESS COUNTER has been reset, the RE-DIAL input code will not be recognized by the circuit. It is necessary that CE be maintained at logic "0" $>$ 1 μs after V_{DD} is applied in order to ensure correct system initializing. If CE is linked to V_{DD} by the method shown in Figure 12, adequate delay is obtained.

3.0 Data Entry – Data is entered to the circuit via a double contact keyboard connected as shown in Figure 10. Keyboard inputs are active low and encoded as shown in Table 2.

Keyboard Code
Table 2

No. of O/P Pulses	Digit	Y_1	Y_2	Y_3	Y_4	X_1	X_2	X_3
1	1	0	1	1	1	0	1	1
2	2	0	1	1	1	1	0	1
3	3	0	1	1	1	1	1	0
4	4	1	0	1	1	0	1	1
5	5	1	0	1	1	1	0	1
6	6	1	0	1	1	1	1	0
7	7	1	1	0	1	0	1	1
8	8	1	1	0	1	1	0	1
9	9	1	1	0	1	1	1	0
10	0	1	1	1	0	1	0	1
RE-DIAL		1	1	1	0	1	1	0

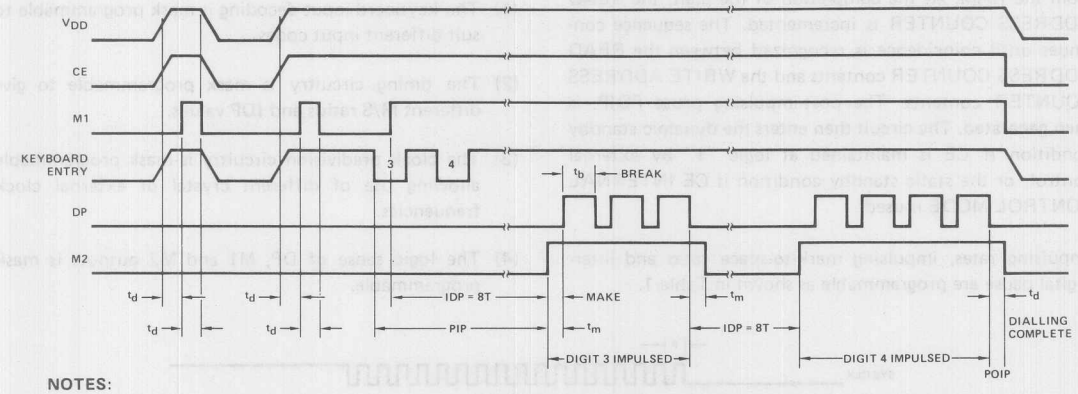
NOTE: "0" indicates pin taken low.

Keyboard inputs are fully decoded eliminating any possibility of invalid codes being recognized. A BCD format is used on-chip for data storage. Valid inputs have contact bounce removed via the debounce counter. Operation is illustrated in Figure 9. Input data is not written into the RAM until the input code has been present for a minimum of 3P and maximum of 4P (P = System Clock Period). The 1P uncertainty arises since data entry is not synchronized to the system clock. This is indicated by the shaded area on the keyboard entry waveform of Figure 9. The trailing edge of a keyboard entry is also debounced. The operation

FUNCTIONAL DESCRIPTION (Cont'd)

of the debounce circuitry results in a maximum data entry rate of SYS CLK ÷ 9. Referring to Figure 9, data must remain stable during the RAM data entry period. Maximum contact bounce rejection is 10 ms at 10 Hz, 6.3 ms at 16 Hz or 5 ms at 20 Hz impulsing rates. Minimum data valid time is 16.7 ms at 10 Hz, 10.4 ms at 16 Hz or 8.4 ms at 20 Hz impulsing rates.

Upon recognition of the first keyboard input of a number string, the dial out sequence is initiated by a pre-impulsing pause (Figure 7). The WRITE ADDRESS COUNTER is incremented on each digit entry. The contents of this counter indicate the length of the number to be dialled. The RE-DIAL code is recognized only if it is presented to the chip a maximum of 5P after CE = "1". Decoding of RE-DIAL then inhibits the reset of the WRITE ADDRESS COUNTER, initiates the dialling sequence and the previous number string entered is dialled. If the circuit application is to utilize RE-DIAL, external CE control is necessary in some cases to ensure that CE = "1" from the first keyboard entry throughout dialling in order to ensure all digits entered are stored consecutively should a delay occur during dialling.



NOTES:

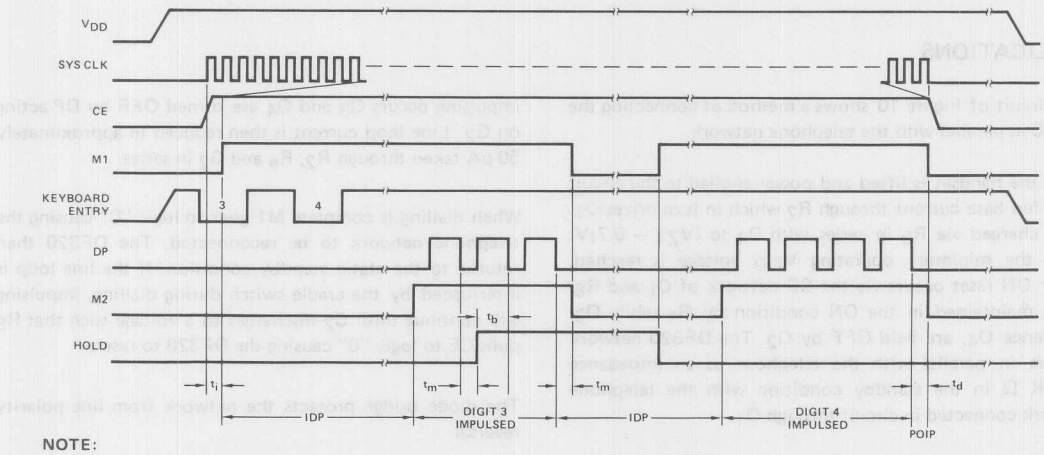
(1) $t_d = 10 \times P$
P = System clock period = T/30
T is selected impulsing period

(2) Pre-Impulsing Pause (PIP) = $8T + t_d$

(3) Post-Impulsing Pause (POIP) is equal to t_d ms on DF320, DF322 and 5T on DF320A.

(4) t_b/t_m is the BREAK/MAKE RATIO. $T = (t_m + t_b)$ ms.
$t_m = 10 \times P$ for 2:1 M/S ratio. $t_m = 12 \times P$ for 3:2 M/S ratio.

Loop Disconnect Dialler Timing Diagram CE—External Control
Figure 7



NOTE:

(1) $t_i = t_{ON} + t_d$ where t_{ON} = Clock Start Up Time

Loop Disconnect Dialler Timing Diagram CE—Internal Control
Figure 8

FUNCTIONAL DESCRIPTION (Cont'd)

4.0 Dialling Sequence – The dialling or impulsing sequence is initiated on recognition of the first keyboard entry after CE = "1". The dialling sequence is identical for both internal and external control of CE. (See Figure 7 and 8).

The basic impulsing pulse train is derived from the TIMING COUNTER AND DECODE. The IDP is timed by forcing a code on the OUTPUT COUNTER and inhibiting DP for the duration of IDP. The READ ADDRESS COUNTER then addresses the RAM and the first digit is used to program the decode of the OUTPUT COUNTER. A number of dial pulses is output via DP corresponding to the BCD data read from the RAM. At the completion of the digit, the READ ADDRESS COUNTER is incremented. The sequence continues until coincidence is recognized between the READ ADDRESS COUNTER contents and the WRITE ADDRESS COUNTER contents. The post-impulsing pause POIP, is then generated. The circuit then enters the dynamic standby condition if CE is maintained at logic "1" by external control, or the static standby condition if CE INTERNAL CONTROL MODE is used.

Impulsing rates, impulsing mark-to-space ratio and inter-digital pause are programmable as shown in Table 1.

The dialling sequence can be interrupted by applying logic "1" to HOLD. If HOLD = "1" is applied during dialling of a digit, the circuit does not enter the HOLD mode until the digit is complete. In the HOLD mode M1 = "0", allowing the telephone line to be monitored. When HOLD is released dialling continues preceded by an IDP. (See Figure 8). HOLD is used to extend the IDP allowing intermediate dial tone recognition if RE-DIAL is used in a PABX for example. Operation can be manual or via external control logic as shown in Figure 13.

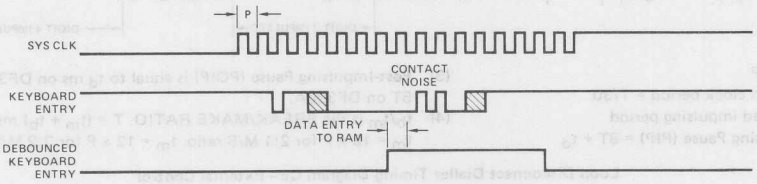
NOTES:

(1) The keyboard input decoding is mask programmable to suit different input codes.

(2) The timing circuitry is mask programmable to give different M/S ratios and IDP values.

(3) The clock predivision circuitry is mask programmable allowing use of different crystal or external clock frequencies.

(4) The logic sense of DP, M1 and M2 outputs is mask programmable.



Keyboard Input Debounce Timing Diagram
Figure 9

APPLICATIONS

The circuit of Figure 10 shows a method of connecting the DF320 in parallel with the telephone network.

When the handset is lifted and power applied to the circuit Q_2 is fed base current through R_2 which in turn drives Q_1. C_2 is charged via R_3 in series with D_1 to $(V_{Z1} - 0.7)V$. When the minimum operating V_{DD} voltage is reached, power ON reset occurs via the CE network of C_1 and R_8. Q_2 is maintained in the ON condition by G_1 while Q_3, and hence Q_4, are held OFF by G_2. The DF320 network appears in parallel with the telephone as an impedance $> 10K\ \Omega$ in the standby condition with the telephone network connected in circuit through Q_1.

On recognition of the first keyed digit, the DF320 clock is started. M1 then goes to logic "1" causing Q_2, Q_1 to turn OFF, and Q_3, Q_4 to turn ON. Hence the majority of the line loop current now flows through Q_4, and Z_1. When impulsing occurs Q_3 and Q_4 are turned OFF by DP acting on G_2. Line loop current is then reduced to approximately 50 μA taken through R_2, R_4 and G_2 in series.

When dialling is complete M1 goes to logic "0" causing the telephone network to be reconnected. The DF320 then returns to the static standby condition. If the line loop is interrupted by the cradle switch during dialling, impulsing will continue until C_2 discharges to a voltage such that R_8 pulls CE to logic "0" causing the DF320 to reset.

The diode bridge protects the network from line polarity reversal.

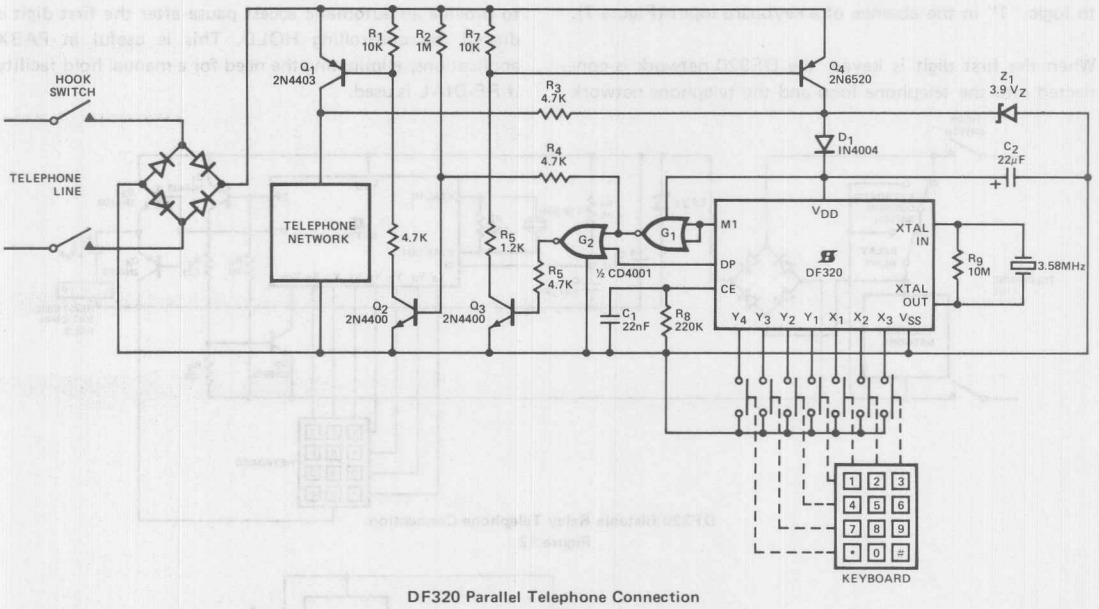
The circuit of Figure 11 shows a simple method of series connection of DF320 into the telephone set suitable for PABX or short line applications.

APPLICATIONS (Cont'd)

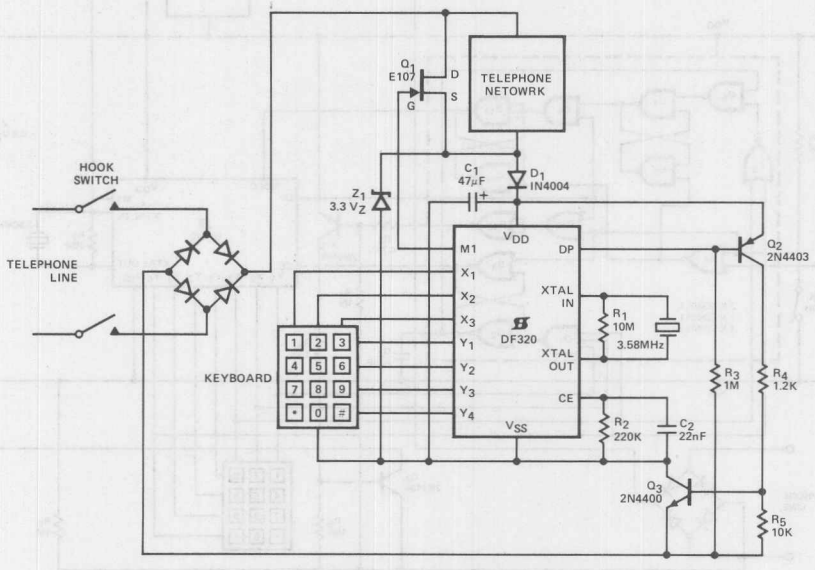
When the telephone handset is lifted, C_1 is charged via D_1 to (V_{Z1} – 0.7) volts and DF320 power ON reset occurs. When the first keyed digit is recognized, M1 goes to logic "1" muting the telephone network by switching on the low ON resistance JFET Q_1, and maximizing the line loop current for impulsing. Impulsing occurs through DP switching Q_2, and hence Q_3, OFF. Rapid discharge of C_1 through Z_1 is prevented during line break by the blocking diode D_1.

When dialling is complete the circuit returns to the static standby condition and Q_1 is switched OFF. Circuit reset during a line interruption by the cradle switch is as for the parallel connection mode.

If a requirement exists that no semiconductor components should appear in the telephone loop during normal speech, the circuit of Figure 12 is required.



DF320 Parallel Telephone Connection
Figure 10

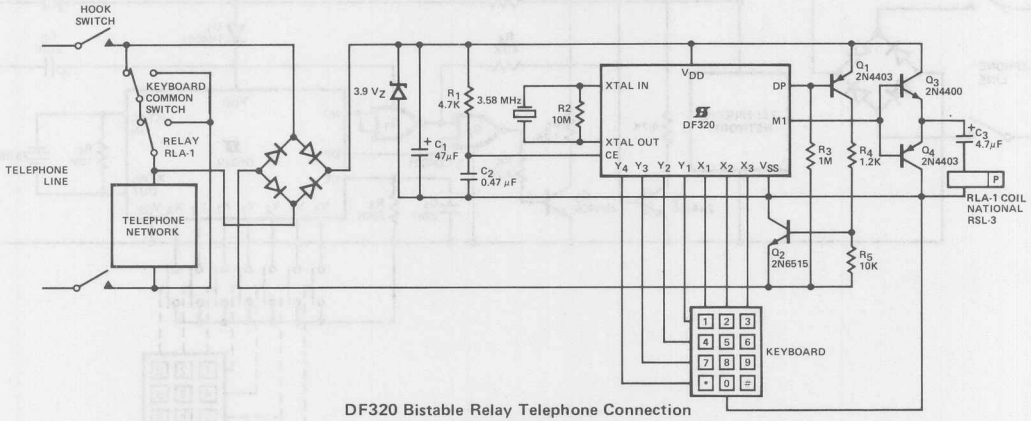


DF320 Series Telephone Connection
Figure 11

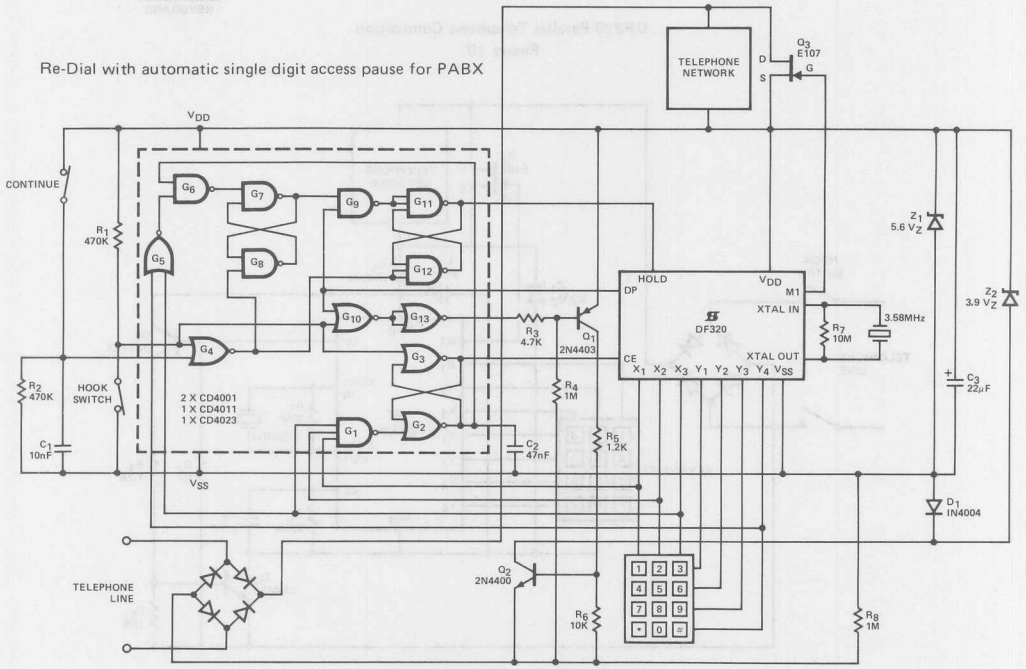
with a bistable relay. In this application external control of CE is provided by the R_1, C_2 network. If, when the handset is lifted, the relay contact is such that the DF320 network is connected in circuit, it is necessary to initialize this relay to reconnect the telephone network. This is achieved by the single pulse which occurs on M1 if CE goes to logic "1" in the absence of a keyboard input (Figure 7).

When the first digit is keyed, the DF320 network is connected into the telephone loop and the telephone network through DP switching Q_1 OFF which in turn switches Q_2. When dialling is complete the bistable relay is pulsed, switching the telephone network back in circuit and short circuiting the DF320 network.

The circuit of Figure 13 shows additional gating circuitry to provide an automatic access pause after the first digit is dialled, by controlling HOLD. This is useful in PABX applications, eliminating the need for a manual hold facility if RE-DIAL is used.



DF320 Bistable Relay Telephone Connection
Figure 12



DF320 Series Telephone Connection
Figure 13

APPLICATIONS (Cont'd)

The basic interface circuit is similar to that shown in Figure 11. Muting is achieved by Q_3 and line switching by Q_2 driven by Q_1.

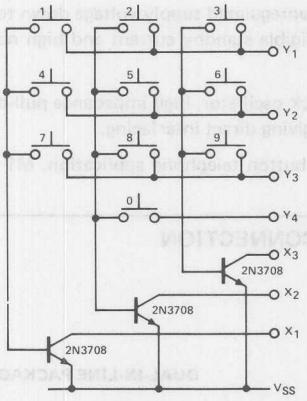
In the ON-hook condition, Q_1 is held OFF by G_{13} and standby current is supplied to the DF320 network by R_8; providing voltage limiting. CE is clamped to logic "0" by G_3. The DF320 is in the static standby mode and the previously dialled number is stored.

When the handset is lifted, G_{13} goes to logic "0" switching Q_1, and hence Q_2, ON. The DF320 network V_{DD} is now given by (V_{Z2} – 0.7) volts. The DF320 remains in the static standby mode until the first key operation. G_1 decodes the common key function toggling the latch formed by G_2 and G_3 causing CE = "1". CE remains at logic "1" throughout the remainder of the OFF-hook condition ensuring that all digits keyed are stored by the DF320 as one number string. (See FUNCTIONAL DESCRIPTION, 3.0 DATA ENTRY).

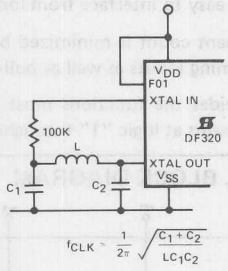
If the first key operated is RE-DIAL, this condition is decoded by G_5, and via G_6 sets the latch formed by G_7 and G_8. G_9 is enabled and the first dial pulse causes the latch formed by G_{11} and G_{12} to be set taking HOLD to logic "1". When the first digit is complete M1 goes to logic "0" enabling the telephone network. When dial tone is recognized the CONTINUE switch is operated causing HOLD = "0" by resetting the latches formed by G_{11}, G_{12} and G_7, G_8. The remainder of the number is then re-dialled. Subsequent operation of RE-DIAL is blocked by G_6.

Figure 14 shows a simple method of interfacing a single contact matrix-type keyboard to the DF320. Operation of a key causes the on-chip pull-up transistor of the Y input to provide base drive current to the corresponding X input external bipolar transistor, which sinks the X input pull-up current through its collector. Hence, a valid code is presented.

As an alternative to the crystal oscillator it is possible to operate the DF320 from an LC combination connected as shown in Figure 15. F01 is connected to V_{DD} selecting the 932 Hz impulsing condition. An oscillator frequency of 38.4kHz will give a 10 Hz impulsing rate.



Single Contact Keyboard Interface
Figure 14



LC Oscillator
Figure 15

CMOS Loop Disconnect Dialer

designed for . . .

- **Push Button Telephones**
- **Repertory Dialers**
- **Telex**
- **Mobile Telephones**
- **Security and Fire Alert Systems**
- **Emergency Number Dialers**

Siliconix

BENEFITS

- **Eliminates the Need for Regulated Supplies**
 - 2.5 V to 5.5 V V_{DD} Range
- **Minimizes Power Consumption**
 - Standby Dissipation $< 3\ \mu W$
- **Low Cost**
 - Simple Support Circuitry
 - No External Power Up Reset Components
- **Minimizes External Components**
 - On-Chip Circuitry for: Keyboard Debouncing; Last Number Repeat; Input Termination
- **Versatile**
 - Selectable Mark/Space Ratio, Impulsing Speeds
 - Oscillator Uses Either LC Network or Crystal

DESCRIPTION

The DF328 monolithic CMOS Loop Disconnect Dialers each contain all the logic necessary to interface a standard double contact keyboard to a telephone system requiring loop disconnect signalling.

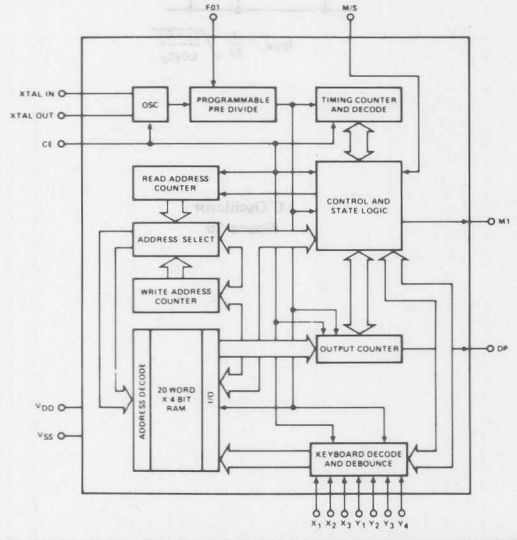
A dial pulsing output and muting output are provided to control the impulsing (loop disconnect) and muting functions. The circuit is capable of storing a number string of up to 20 digits and re-dialing this stored number automatically at a later time, initiated by a RE-DIAL input code. Impulsing mark/space ratio (M/S) and impulsing rate are pin programmable to meet most telephone requirements.

The use of Siliconix low voltage CMOS technology allows operation with an unregulated supply voltage down to a guaranteed minimum of 2.5 V. This feature, together with low operating current, negligible standby current and high noise immunity make the DF328 easy to interface from long telephone lines.

External component count is minimized by the inclusion of an on-chip clock oscillator, high impedance pull-down terminations to programming inputs as well as pull-up terminations to the keyboard giving direct interfacing.

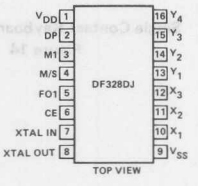
The DF328 provides the functions most commonly required in the push button telephone application. M1 is the muting output which remains at logic "1" throughout the dialing sequence.

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTION

DUAL-IN-LINE PACKAGE



ORDER NUMBER DF328DJ
SEE PACKAGE 8

ABSOLUTE MAXIMUM RATINGS

$V_{DD} - V_{SS}$ −0.3 V to 8 V
Voltage on Any Pin V_{SS} − 0.3 V to V_{DD} + 0.3 V
Current at Any Pin 10 mA
Operating Temperature −40 to +85°C
Storage Temperature (J Package) −65 to +125°C

Power Dissipation (J Package)* 450 mW

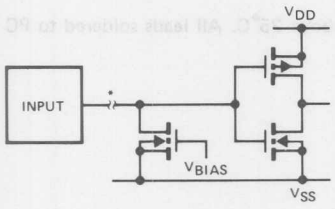
*Derate 6.3 mW/°C above 25°C. All leads soldered to PC board.

ELECTRICAL CHARACTERISTICS

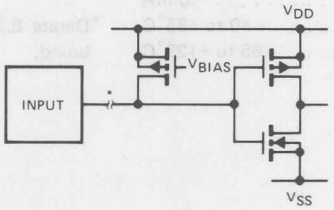
All voltages referenced to V_{SS} unless otherwise noted.

		Characteristic			Min	Typ*	Max	Units	Test Conditions Unless Noted V_{DD} = 3.0 V, T_A = 25°C, f_{CLK} = 3.579545 MHz	
1	SUP	V_{DD}	Supply Voltage Operating Range		2.5		5.5	V		
2	SUP	I_{DSS}	Standby Supply Current			1.0	15.0	µA	CE = V_{SS}	
3	SUP	I_{DD}	Operating Supply Current			180	250	µA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12 pF	
4	INPUT	I_{IL}	Pull-Up Transistor Source Current		−0.5	−3.0	−10.0	µA	$V_{IN} = V_{SS}$	$X_1, X_2, X_3,$
5	INPUT	I_{IH}	Input Leakage Current			0.1		nA	$V_{IN} = V_{DD}$	Y_1, Y_2, Y_3, Y_4
6	INPUT	I_{IL}	Input Leakage Current			−0.1		nA	$V_{IN} = V_{SS}$	M/S F01
7	INPUT	I_{IH}	Pull-Down Transistor Sink Current		0.5	3.0	10.0	µA	$V_{IN} = V_{DD}$	M/S F01
8	INPUT	V_{IL}	Logic "0" Level				0.65	V	All Inputs	
9	INPUT	V_{IH}	Logic "1" Level		2.45			V	All Inputs	
10	OUT	V_{OL}	Voltage Levels	Low Level		0	0.01	V	No Load	DP, M1
11	OUT	V_{OH}	Voltage Levels	High Level	2.99	3		V	No Load	DP, M1
12	OUT	I_{OL}	Drive Current	N-Channel Sink	0.5	2.0		mA	V_{OUT} = 2.3 V	DP, M1
13	OUT	I_{OH}	Drive Current	P-Channel Source	−0.5	−1.5		mA	V_{OUT} = 0.7 V	DP, M1
14	DYNAMIC	t_r	Output Rise Time			1.0		µs	DP, M1 C_L = 50 pF	
15	DYNAMIC	t_f	Output Fall Time			1.0		µs	DP, M1 C_L = 50 pF	
16	DYNAMIC	f_{CLK}	Clock Frequency		0.03		3.58	MHz		
17	DYNAMIC	M/S	Mark to Space Ratio			2:1			See Table 1	
18	DYNAMIC	M/S	Mark to Space Ratio			3:2			See Table 1	
19	DYNAMIC	IDP	Interdigital Pause			8T		ms	T = Impulsing Period	
20	DYNAMIC	Impulsing Rate = 1/T				10		Hz	See Table 1	
21	DYNAMIC	Impulsing Rate = 1/T				932		Hz	See Table 1	
22	DYNAMIC	t_{ON}	Clock Start Up Time			1.5	4	ms	Timed from CE = Logic "1"	
23	DYNAMIC	C_{IN}	Input Capacitance			5.0		pF	Any Input	
24	DYNAMIC	P_{OIP}	Post Impulsing Pause			0.3T		ms	T = Selected Impulsing Period	

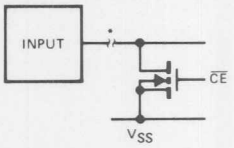
*Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.



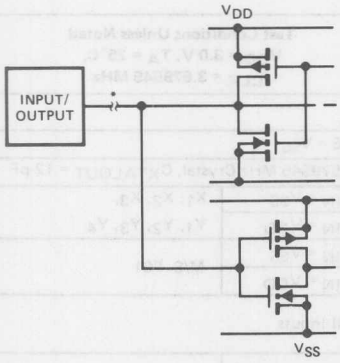
M/S, F01
Figure 1



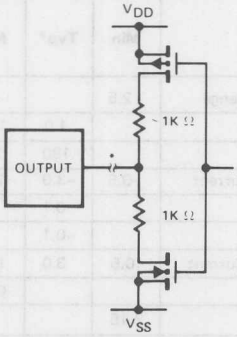
$X_1, X_2, X_3, Y_1, Y_2, Y_3, Y_4$
Figure 2



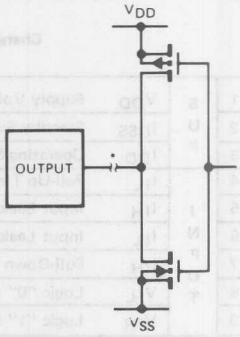
XTAL IN
Figure 3



CE
Figure 4



DP, M1
Figure 5

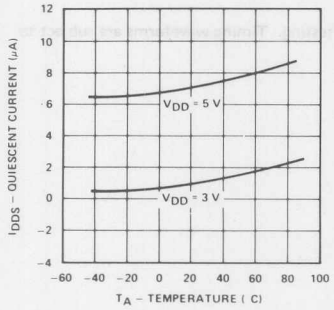


XTAL OUT
Figure 6

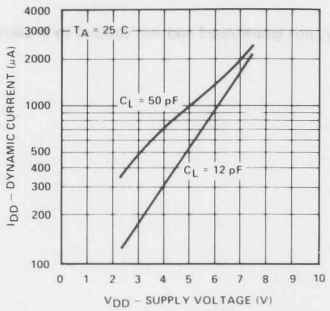
*Circuit protection not shown

TYPICAL CHARACTERISTICS

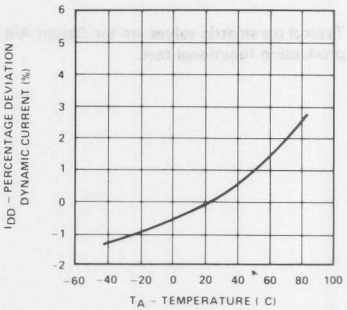
Typical Quiescent Current vs Temperature



Typical Dynamic Current vs Supply Voltage (V_{DD})

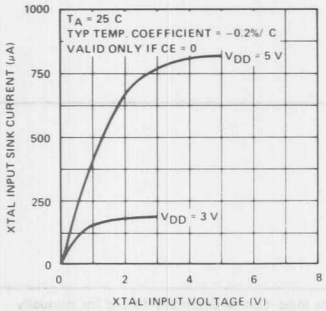


Typical Percentage Deviation of Dynamic Current vs Temperature (Normalized to 25°C)

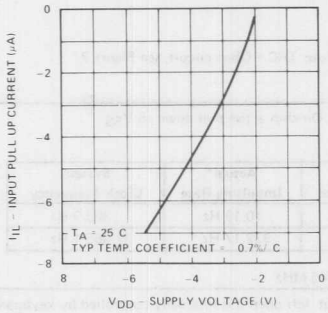


TYPICAL CHARACTERISTICS (Cont'd)

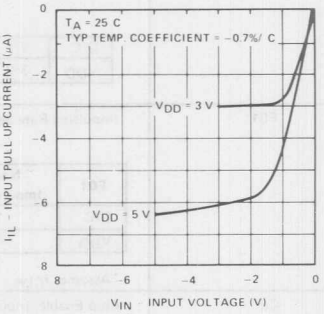
Typical XTAL IN Input Clamp Characteristics



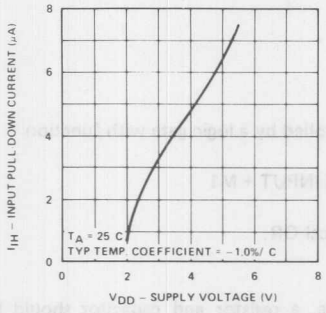
Typical Input Pull-Up Current vs Supply Voltage (X_1, X_2, X_3, Y_1, Y_2, Y_3, Y_4)



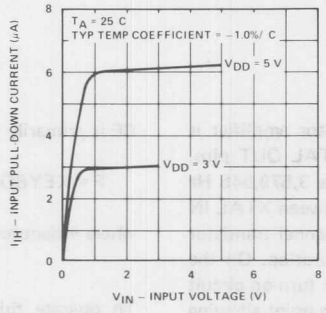
Typical Input Pull-Up Characteristics



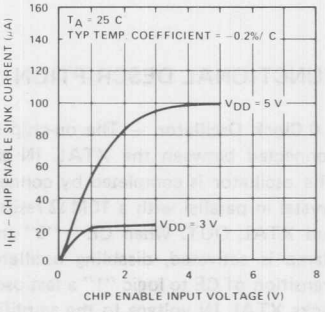
Typical Input Pull-Down Current vs Supply Voltage (M/S, F01)



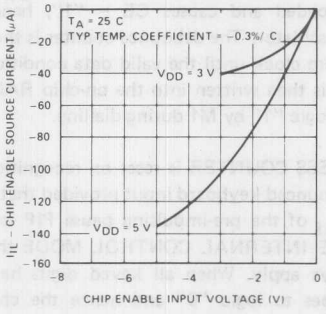
Typical Input Pull-Down Characteristics



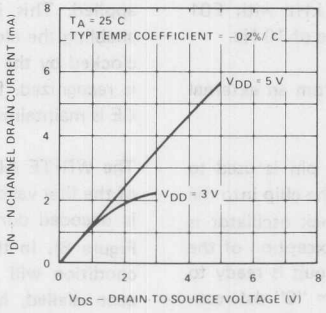
Typical Chip Enable Sink Characteristics



Typical Chip Enable Source Characteristics



Typical Output N-Channel Drain Characteristics (DP, M1)



Typical Output P-Channel Drain Characteristics (DP, M1)

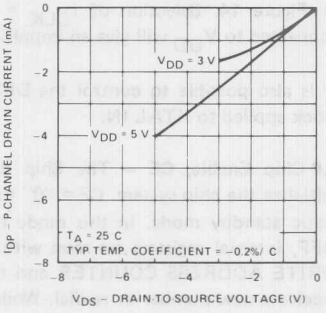


Table 1

PIN FUNCTION	DESCRIPTION
V_{DD}	Positive voltage supply
DP	Dial Pulsing Output Buffer
M1	Mask 1 (Buffered Output) = Logic "1" during Dialling Sequence
M/S	Mark/Space (Break/Make) Ratio select. On-chip active pull-down to V_{SS}. O/C = 2:1 V_{DD} = 3:2 Note: O/C = Open circuit, see Figure 7.
F01	Impulsing Rate Selection. On-chip active pull-down to V_{SS}. F01 = O/C: Nominal Impulsing Rate 10 Hz; Actual* Impulsing Rate 10.13 Hz; System Clock Frequency 303.9 Hz F01 = V_{DD}: Nominal Impulsing Rate 932 Hz; Actual* Impulsing Rate 932.17 Hz; System Clock Frequency 27,965.1 Hz *Assumes f_{CLK} = 3.579545 MHz
CE	Chip Enable. Input/Output, left open it is internally controlled by keyboard decode logic. Can be externally forced for manually enabling chip.
XTAL IN	Crystal Input. Active, clamped low if CE = "0", high impedance if CE = "1".
XTAL OUT	Crystal Output. Buffer to drive crystal. Capacitive load on-chip.
V_{SS}	System ground
X_1, X_2, X_3	Column keyboard inputs having active pull-ups to V_{DD}. Active LOW.
Y_1, Y_2, Y_3, Y_4	Row keyboard inputs having active pull-ups to V_{DD}. Active LOW

FUNCTIONAL DESCRIPTION

1.0 Clock Oscillator — The on-chip oscillator amplifier is connected between the XTAL IN and XTAL OUT pins. The oscillator is completed by connecting a 3,579,545 Hz crystal in parallel with a 10M Ω resistor between XTAL IN and XTAL OUT. When CE = "0" an N-channel transistor clamp is activated, disabling oscillator operation. On the transition of CE to logic "1" a fast oscillator turn-on circuit kicks XTAL IN voltage to the amplifier bias point allowing oscillator operation within 4 ms. The basic clock frequency of 3.58 MHz is predivided by a programmable counter to provide the chip system clock.

As an alternative, an LC oscillator can be formed as shown in Figure 14. Selection of f_{CLK} = 38.4 kHz with F01 connected to V_{DD} will give an impulsing rate of 10 Hz.

It is also possible to control the DF328 from an external clock applied to XTAL IN.

2.0 Chip Enable, CE — The Chip Enable pin is used to initialize the chip system. CE = "0" forces the chip into the static standby mode. In this mode the clock oscillator is OFF, internal registers are reset with the exception of the WRITE ADDRESS COUNTER and the circuit is ready to receive a new number or re-dial. While CE = "0" data cannot be received by the chip, but data previously entered and stored is maintained. When CE = "1" the clock oscillator is operating, the internal registers are enabled, and data can be entered from the keyboard up to a maximum of 20 digits.

CE is primarily controlled by a logic gate with function

F = KEYBOARD INPUT + M1

where + denotes logical OR.

To operate this gate, a resistor and capacitor should be connected in parallel between CE and V_{SS}. When the chip is used in the CE INTERNAL CONTROL MODE power ON reset occurs when V_{DD} is applied, since a logic "0" appears on the CE pin. The chip remains in the static standby condition until it receives the first keyboard input after V_{DD} is applied. This is decoded and causes CE = "1", hence enabling the clock oscillator. The debounce counter is then clocked by the system clock until the valid data condition is recognized. Data is then written into the on-chip RAM. CE is maintained at logic "1" by M1 during dialling.

The WRITE ADDRESS COUNTER is reset on recognition of the first valid debounced keyboard input provided that it is decoded during t_d of the pre-impulsing pause PIP (see Figure 8). In the CE INTERNAL CONTROL MODE this condition will always apply. When all keyed digits have been dialled, M1 goes to logic "0" and hence the chip returns to the static standby condition. If digits are subsequently keyed during the same OFF-hook period, after a pause in dialling for example, the digit string will be recognized as a new number. This is not important provided RE-DIAL operation is not required.

FUNCTIONAL DESCRIPTION (Cont'd)

The alternative to the CE INTERNAL CONTROL MODE is to override the internal logic gate with an externally derived signal. This mode of operation is referred to as the CE EXTERNAL CONTROL MODE. Figure 7 shows that if CE goes to logic "1" in the absence of a keyboard input, a single pulse of duration t_{td} is generated on M1. This pulse is intended to initialize a bistable latching relay used as shown in Figure 12. Immediately prior to M1 going to logic "1", the WRITE ADDRESS COUNTER is reset. All digits keyed subsequently are entered into consecutive RAM locations up to a maximum of 20. After the WRITE ADDRESS COUNTER has been reset, the RE-DIAL input code will not be recognized by the circuit. It is necessary that CE be maintained at logic "0" $>$ 1 μs after V_{DD} is applied in order to ensure correct system initializing. If CE is linked to V_{DD} by the method shown in Figure 12, adequate delay is obtained.

3.0 Data Entry – Data is entered to the circuit via a double contact keyboard connected as shown in Figure 10. Keyboard inputs are active low and encoded as shown in Table 2.

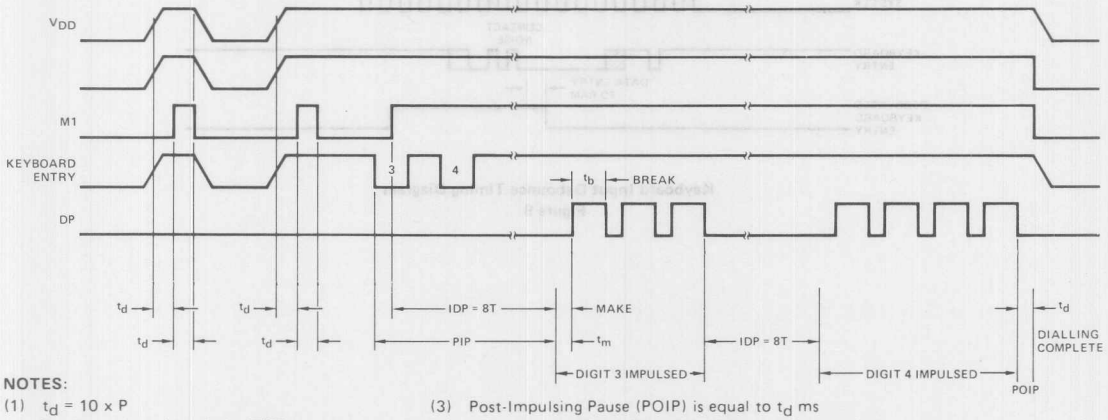
Keyboard inputs are fully decoded eliminating any possibility of invalid codes being recognized. A BCD format is used on-chip for data storage. Valid inputs have contact bounce removed via the debounce counter. Operation is illustrated in Figure 9. Input data is not written into the RAM until the input code has been present for a minimum of 3P and maximum of 4P (P = System Clock Period). The 1P uncertainty arises since data entry is not synchronized to the system clock. This is indicated by the shaded area on the keyboard entry waveform of Figure 9. The trailing edge of a keyboard entry is also debounced. The operation of the debounce circuitry results in a maximum data entry rate of SYS CLK ÷ 9. Referring to Figure 9, data must remain stable during the RAM data entry period. Maximum contact bounce rejection is 10 ms at 10 Hz impulsing rate. Minimum data valid time is 16.7 ms at 10 Hz impulsing rate.

Keyboard Code
Table 2

No. of O/P Pulses	Digit	Y_1	Y_2	Y_3	Y_4	X_1	X_2	X_3
1	1	0	1	1	1	0	1	1
2	2	0	1	1	1	1	0	1
3	3	0	1	1	1	1	1	0
4	4	1	0	1	1	0	1	1
5	5	1	0	1	1	1	0	1
6	6	1	0	1	1	1	1	0
7	7	1	1	0	1	0	1	1
8	8	1	1	0	1	1	0	1
9	9	1	1	0	1	1	1	0
10	0	1	1	1	0	1	0	1
RE-DIAL		1	1	1	0	1	1	0

NOTE: "0" indicates pin taken low.

Upon recognition of the first keyboard input of a number string, the dial out sequence is initiated by a pre-impulsing pause (Figure 7). The WRITE ADDRESS COUNTER is incremented on each digit entry. The contents of this counter indicate the length of the number to be dialled. The RE-DIAL code is recognized only if it is presented to the chip a maximum of 5P after CE = "1". Decoding of RE-DIAL then inhibits the reset of the WRITE ADDRESS COUNTER, initiates the dialling sequence and the previous number string entered is dialled. If the circuit application is to utilize RE-DIAL, external CE control is necessary in some cases to ensure that CE = "1" from the first keyboard entry throughout dialling in order to ensure all digits entered are stored consecutively should a delay occur during dialling.



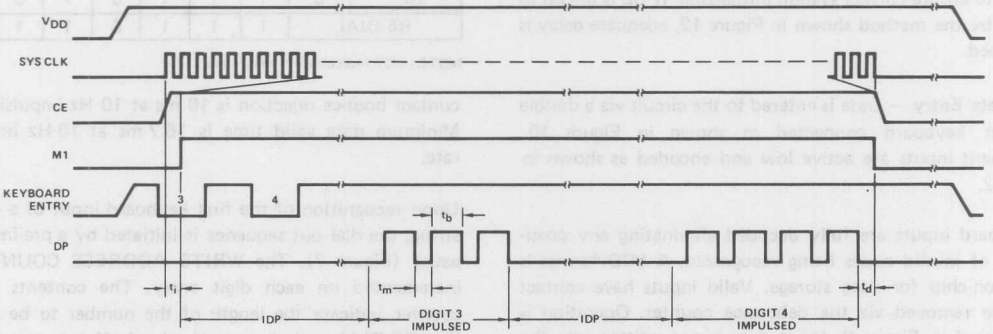
NOTES:
(1) t_d = 10 x P
P = System clock period = T/30
T is selected impulsing period
(2) Pre-Impulsing Pause (PIP) = 8T + t_d
(3) Post-Impulsing Pause (POIP) is equal to t_d ms
(4) t_b/t_m is the BREAK/MAKE RATIO. T = (t_m + t_b) ms.
t_m = 10 x P for 2:1 M/S ratio. t_m = 12 x P for 3:2 M/S ratio.

Loop Disconnect Dialler Timing Diagram CE–External Control
Figure 7

FUNCTIONAL DESCRIPTION (Cont'd)

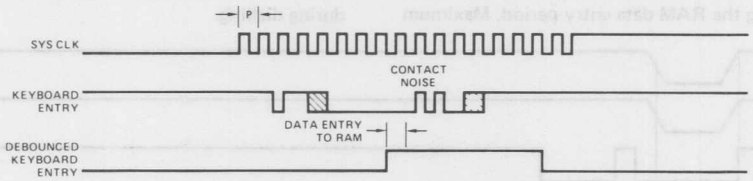
internal and external control of CE. (See Figures 7 and 8).

The basic impulsing pulse train is derived from the TIMING COUNTER AND DECODE. The IDP is timed by forcing a code on the OUTPUT COUNTER and inhibiting DP for the duration of IDP. The READ ADDRESS COUNTER then addresses the RAM and the first digit is used to program the ADDRESS COUNTER is incremented. The sequence continues until coincidence is recognized between the READ ADDRESS COUNTER contents and the WRITE ADDRSSS COUNTER contents. The post-impulsing pause POIP, is then generated. The circuit then enters the dynamic standby condition if CE is maintained at logic "1" by external control, or the static standby condition if CE INTERNAL CONTROL MODE is used.



NOTE:
(1) $t_i = t_{ON} + t_d$ where t_{ON} = Clock Start Up Time

Loop Disconnect Dialler Timing Diagram CE—Internal Control
Figure 8



Keyboard Input Debounce Timing Diagram
Figure 9

APPLICATIONS

The circuit of Figure 10 uses a minimum number of components and provides very low current operation.

When the handset is lifted, power is applied through the diode bridge to the dialer circuit. Current flows through D_1, CR_1 and Z_2, establishing V_{DD} for the DF328 and charging C_1. When the minimum operating voltage (V_{DD}) is reached, power on reset occurs via the CE network of C_2 and R_1. Initially, both DP and M_1 are LOW, giving a LOW at the gate of Q_1 to hold it off, while the HIGH at the gate of Q_2 turns it on, connecting the telephone network. The current limiting diode, CR_1 serves two purposes. First, it limits the total dialer circuit current drawn from the loop to less than 1mA, and secondly, maintains a high dialer circuit shunting impedance across the telephone set network. Z_1 is a high voltage, high surge capability device which provides protection against loop transients and office inductance spikes. The device should limit all transients to less than the breakdown voltages of CR1, Q_1 and Q_2 (100 volts).

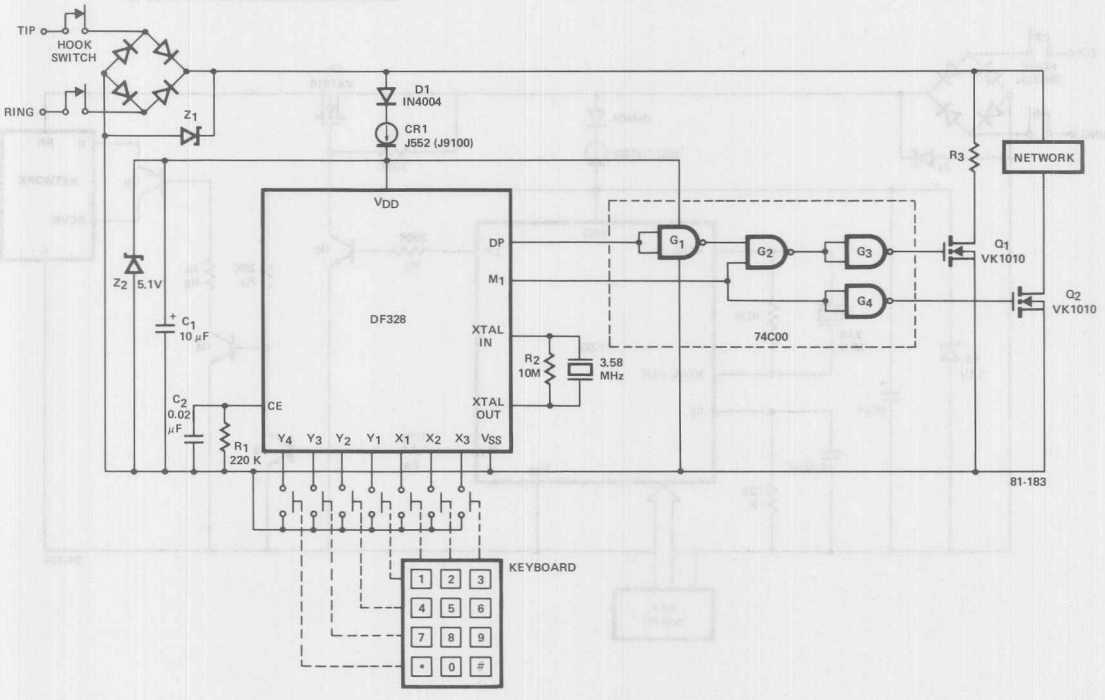
On recognition of the first keyed digit, the DF328 clock is started. M1 then goes HIGH, causing Q_2 to turn off and Q_1 to turn on. This mutes the receiver in the network and allows loop current flow to continue through R_3 and Q_1. When dial pulse breaks occur, DP will go HIGH, causing G_3 output to go LOW and turning off Q_1. Loop current flow during breaks is controlled by CR1.

When dialing is complete, M1 goes LOW causing Q_1 to open and the telephone network to be reconnected. The DF328 then returns to the static standby condition and the oscillator is turned off.

The diode bridge protects the dialer circuit from line polarity reversal. D1 prevents rapid discharge of C_1 during makes in dialing if the voltage across R_3 and Q_1 is lower than the voltage across C_1.

The VMOS devices combine low ON resistance and high breakdown voltage with very high input impedance. The high input impedance allows direct drive from CMOS logic and very low dialer circuit current consumption when compared to bipolar devices. This is important because of the wide variation in circuit operating conditions resulting from the need to accommodate both long and short loops.

Another approach is illustrated in Figure 11. The circuitry is similar to Figure 10 except for the dailing and muting functions. During non-dialing periods when the phone is off-hook, both DP and M1 will be LOW. Q_2 will be held OFF by DP, allowing Q_1 gate voltage to equal the drain voltage. A bias voltage will exist from gate to source, keeping it ON and allowing current flow through the telephone network. Q_3 is also held OFF by M1. This in turn allows Q_4 and Q_5 to be ON. Since Q_5 is in series with the receiver, no muting occurs.



DF328 Dialer Circuit Connection
Figure 10

APPLICATIONS (Cont'd)

When a key is depressed for dialing, M1 goes HIGH, turning ON Q_3 and turning OFF Q_4 and Q_5, thus muting the receiver. DP goes HIGH during dial pulse breaks, turning ON Q_2 and turning OFF Q_1. After dial pulsing is complete, DP and M1 return LOW, reconnecting the network and receiver for speech transmission. Q_1 and Q_2 should both be high voltage devices.

If a requirement exists that no semiconductor components should appear in the telephone loop during normal speech, the circuit of Figure 12 is required.

While the circuits of Figures 10 and 11 did not require a common keyboard contact, it is necessary to have a common changeover switch in this case operating in conjunction with a bistable relay. In this application external control of CE is provided by the R_1, C_2 network. If, when the handset is lifted, the relay contact is such that the DF328 network is connected in circuit, it is necessary to initialize this relay to reconnect the telephone network. This is achieved by the single pulse which occurs on M1 if CE goes to logic "1" in the absence of a keyboard input (Figure 7).

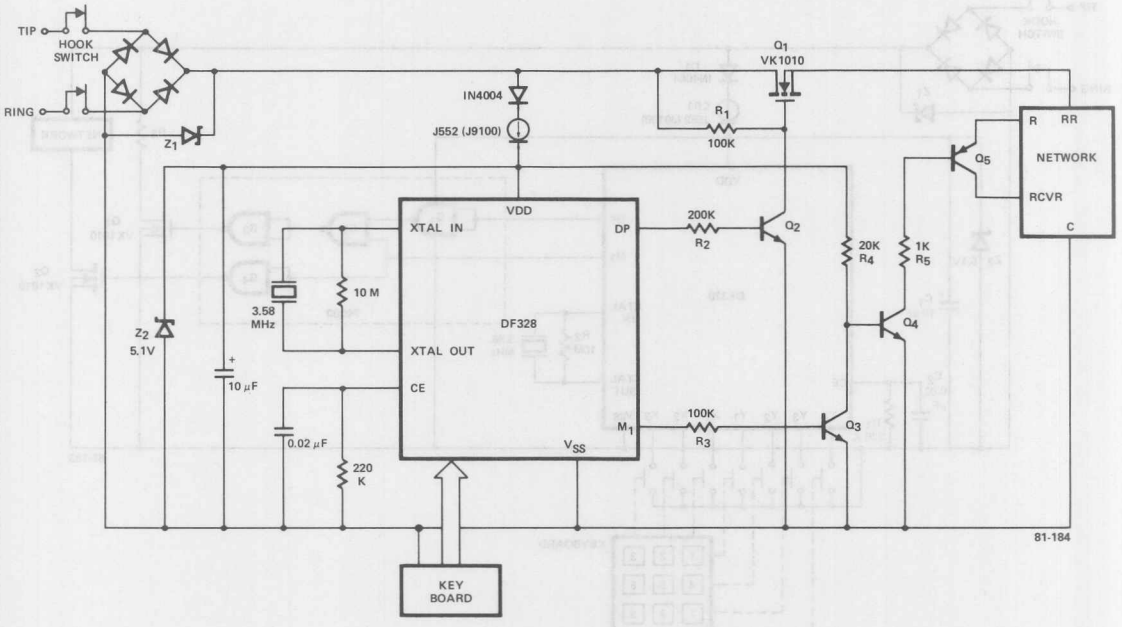
When the first digit is keyed, the DF328 circuit is connected into the telephone loop and the telephone network short circuited by the keyboard common switch. M1 then goes to logic "1" switching the bistable relay, hence maintaining the DF328 network in circuit. Impulsing occurs through DP switching Q_1 OFF which in turn switches Q_2. When dialing is complete the bistable relay is pulsed, switching the telephone network back in circuit and short circuiting the DF328 network.

Figure 13 shows a simple method of interfacing a single contact matrix-type keyboard to the DF328. Operation of a key causes the on-chip pull-up transistor of the Y input to provide base driver current to the corresponding X input external bipolar transistor, which sinks the X input pull-up current through its collector. Hence, a valid code is presented.

As an alternative to the crystal oscillator it is possible to operate the DF328 from an LC combination connected as shown in Figure 14. F01 is connected to V_{DD} selecting the 932 Hz impulsing condition. An oscillator frequency of 38.4 kHz will give a 10 Hz impulsing rate. High values of inductance and Q should be used to ensure that the loop gain does not fall below unity. Typical values are given in Table 3 for F = 38.4 kHz.

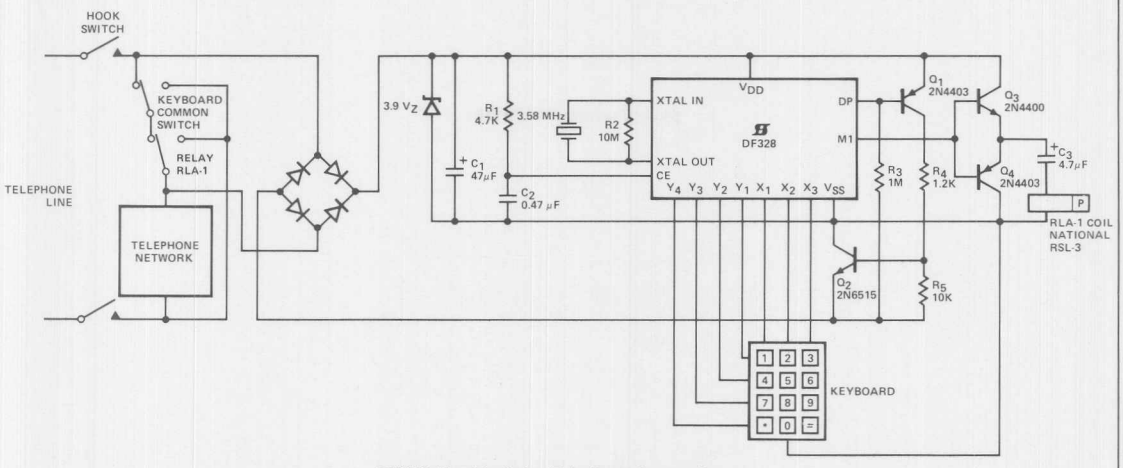
Table 3

L	1.718	mH
Q	100	
C_1	0.02	μF
C_2	0.02	μF

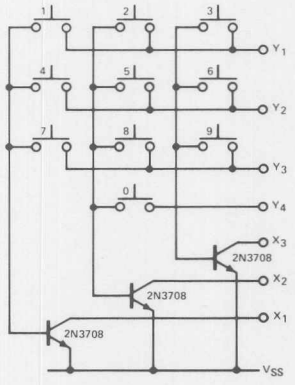


DF328 Parallel Telephone Connection
Figure 11

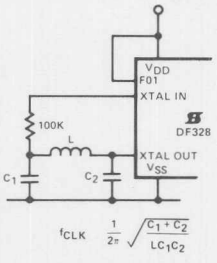
APPLICATIONS (Cont'd)



DF328 Bistable Relay Telephone Connection
Figure 12



Single Contact Keyboard Interface
Figure 13



LC Oscillator
Figure 14

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Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Analog Switches

Basic Part No. (Note 1)	Switch Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$ (nA)	Switching Time (μsec) t_{ON}	Switching Time (μsec) t_{OFF}	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Opt. Supply Voltage (V) (+) Sup. V+	Opt. Supply Voltage (V) (−) Sup. V−	Opt. Supply Voltage (V) Logic Sup. V_L	Opt. Supply Voltage (V) Ref. Sup. V_R	Comments	Switch Configuration
TWO CHANNEL SPDT														
DG189	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	10	10	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies	
DG190	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make JAN/11107	
	N-JFET	+15 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG191	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make JAN/11108	**2 SPDT Switches per Package**
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG243	Plus 40 CMOS	+15 to −15	50	1	0.5	1.0	0.8	2.0	15	−15	5	–	Make-Before-Break (DG191 Pin Out)	
DG290	N-JFET	+15 to −7.5	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Break-Before-Make	
DG303	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, TTL In JAN/11604	
DG303A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, TTL In	
DG307	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	–	–	Low Power, CMOS In JAN/11608	
DG307A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	–	–	Low Power, CMOS In	
DG390	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG190 Pin Out	
DG390A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG190 Pin Out	
DG5043	CMOS	+15 to −15	50	1	1.0	0.5	0.8	2.0	15	−15	5	–		
ONE CHANNEL DPST														
DG5044	CMOS	+15 to −15	50	1	1.0	0.5	0.8	2	15	−15	5	–	TTL Compatible	1 DPST Switch per Package
TWO CHANNEL DPST														
DG183	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	10	10	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies	
DG184	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG185	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	**2 DPST Switches per Package**
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG284	N-JFET	+15 to −7.5	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Break-Before-Make	
DG302	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, TTL In	
DG302A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, TTL In	
DG306	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	–	–	Low Power, CMOS In	
DG306A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	–	–	Low Power, CMOS In	
DG384	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG184 Pin Out	
DG384A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG184 Pin Out	
DG5045	CMOS	+15 to −15	50	1	1.0	0.5	0.8	2.0	15	−15	5	–		

NOTES:

1. The devices shown in **boldface** are recommended parts for new designs.
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. $V_{REF} = 1.5$ V is used when supply voltages $< \pm 15$ V are used. Not needed when supply voltages of ± 15 are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to +10 V.

Analog Switches (Cont'd)

Basic Part No. (Note 1)	Switch Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$ (nA)	Switching Time (μsec) t_{ON}	Switching Time (μsec) t_{OFF}	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Opt. Supply Voltage (V) (+) Sup. V+	Opt. Supply Voltage (V) (−) Sup. V−	Opt. Supply Voltage (V) Logic Sup. V_L	Opt. Supply Voltage (V) Ref. Sup. V_R	Comments	Switch Configurati
SINGLE CHANNEL SPST														
DG5040	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2	15	−15	5	—	TTL Compatible	1 SPST Switch per Pa
TWO CHANNEL SPST														
DG180	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
		+10 to −7.5	10	10	0.3	0.26	0.8	2.0	15	−15	5	0	15 V Supplies	
DG181	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
		+10 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies JAN/11101	
DG182	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
		+10 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies JAN/11102	2 SPST Switches per P
DG200	CMOS	+15 to −15	70	2	1.0	0.5	0.8	2.4	15	−15	—	(Note 3)	JAN/12303	
DG200A	Plus 40 CMOS	+15 to −15	70	2	1.0	0.5	0.8	2.4	15	−15	—	—	TTL In	
DG281	N-JFET	+15 to −15	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Low Charge Injection	
DG300	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In JAN/11601	
DG300A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In	
DG304	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In JAN/11605	
DG304A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In	
DG381	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG181 Pin Out	
DG381A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG181 Pin Out	
DG5041	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2.0	15	−15	5	—	TTL Compatible	
FOUR CHANNEL SPST														
DG201	CMOS	+15 to −15	175	1	1.0	0.5	0.8	2.4	15	−15	—	(Note 3)	JAN/12304	4 SPST Switches per P
DG201A	Plus 40 CMOS	+15 to −15	175	1	1.0	0.5	0.8	2.4	15	−15	—	—	TTL In	
DG202	Plus 40 CMOS	+15 to −15	175	1	1.0	0.5	0.8	2.4	15	−15	—	—	TTL In	
DG211	Plus 40 CMOS	+15 to −15	175	5	0.5	0.4	0.8	2.4	15	−15	5	—	Low Cost, TTL In	
DG212	Plus 40 CMOS	+15 to −15	175	5	0.6	0.45	0.8	2.4	15	−15	5	—	Low Cost, TTL In	
DG308	CMOS	+15 to −15	100	1	0.2	0.15	3.5	11.0	15	−15	—	—	Low Cost CMOS In	
DG309	Plus 40 CMOS	+15 to −15	100	5	0.2	0.15	3.5	11.0	15	−15	—	—	Low Cost CMOS In	
ONE CHANNEL SPDT														
DG186	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	10	10	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies	
DG187	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies JAN/11105	
DG188	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	1 SPST Switch per Pac
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies JAN/11106	
DG287	N-JFET	+15 to −7.5	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Break-Before-Make	
DG301	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In JAN/11602	
DG301A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In	
DG305	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In JAN/11605	
DG305A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In	
DG387	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG187 Pin Out	
DG387A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG187 Pin Out	
DG5042	CMOS	+15 to −15	50	1	1.0	0.5	0.8	4.0	15	−15	5	—	TTL Compatible	

NOTES:

1. The devices shown in **boldface** are recommended parts for new designs.
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. $V_{REF} = 1.5$ V is used when supply voltages < ±15 V are used. Not needed when supply voltages of ±15 are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to +10 V.

5-Channel SPST PMOS Switches with Drivers

Siliconix

designed for . . .

- **Communication Systems**
- **Portable, Battery Operated Units**
- **Make-Before-Break Switching i.e. Feedback Resistor Switching in Variable Gain Op-Amps**

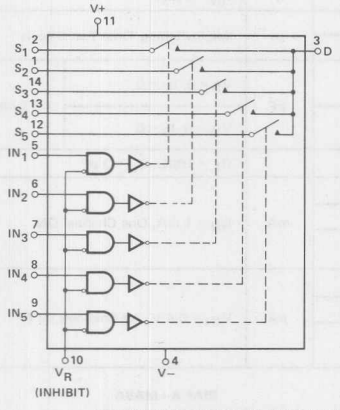
BENEFITS

- **Minimizes Standby Power Requirements**
 - 550 μW
- **Low Leakage**
 - $\leqslant$ 1 nA
- **Reduces External Component Requirements**
 - Internal Zener Diodes Protect All MOS Gates

DESCRIPTION

The DG123 contains five MOS field-effect transistors designed to function as electronic switches. Level-shifting drivers enable a low-level input (0.4 to 1.3 V) to control the ON-OFF condition of each switch. In the ON state each switch conducts current equally well in either direction, and in the OFF state the switches will block voltages up to 20 V peak-to-peak. In the OFF state, total circuit power dissipation is $<$ 0.5 mW. Positive logic "1" at the input turns the switch ON. Switch action is make-before-break. Not recommended for new designs.

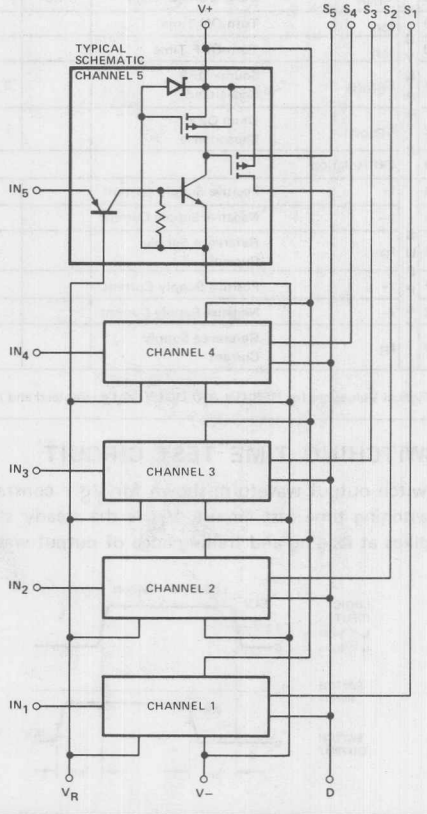
FUNCTIONAL DIAGRAM



LOGIC	SWITCH
0	ON
1	OFF

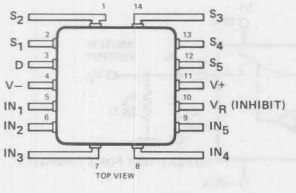
SWITCHES CLOSED FOR LOGIC "1" INPUT
(POSITIVE LOGIC)

SCHEMATIC DIAGRAM



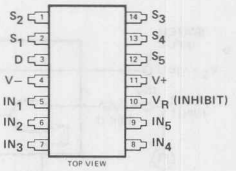
PIN CONFIGURATIONS

Flat Package



ORDER NUMBER:
DG123AL
SEE PACKAGE 5

Dual-In-Line Package



ORDER NUMBERS:
DG123AP OR DG123BP
SEE PACKAGE 11

ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V_D to V−	36 V
V_S to V−	36 V
V_D to V_S	25 V
V_S to V_D	25 V
V_R to V−	30 V
V_{IN} to V−	30 V
V_R to V_{IN}	6 V
V_{IN} to V_R	2 V

Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads soldered or welded to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

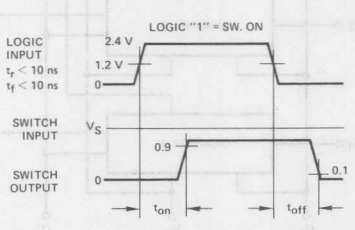
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX −20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 10 V, V− = −20 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_D = 10 V	I_S = −1 mA, I_{IN} = 1 mA
2				200	200	250	225	225	300		V_D = 0	
3				450	450	600	500	500	600		V_D = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current		−1	−1000		−5	−100	nA	V_S = −10 V, V_D = 10 V	V_{IN} = 0.4 V
5		$I_{D(off)}$	Drain OFF Leakage Current		−1	4000		−10	−300		V_D = −10 V, V_S = 10 V	
6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		4	4000		10	300		$V_D = V_S$ = 10 V	I_{IN} = 1 mA
7	INPUT	I_{INL}	Logic Input Current, Input Voltage Low	1	1	100	5	5	100	μA	V_{IN} = 0.4 V	
8		V_{INH}	Input Voltage, High	1.3	1	0.8	1.3	1	1	V	I_{IN} = 1 mA	
9	DYNAMIC	t_{on}	Turn-ON Time		0.3			0.5		μs	See Switching Time Test Circuit	
10		t_{off}	Turn-OFF Time		2			2				
11		$C_{S(off)}$	Source OFF Capacitance		3 Typ*			3 Typ*		pF	V_S = 0, I_D = 0	f = 1 MHz
12		$C_{D(off)}$	Drain OFF Capacitance		7 Typ*			7 Typ*			V_D = 0, I_S = 0	
13		Off Isolation		Typ > −50 dB at 5 MHz*							R_L = 100Ω, C_L = 3 pF	
14	SUPPLY	I+	Positive Supply Current		3			3		mA	I_{IN} = 1 mA, One Channel ON	
15		I−	Negative Supply Current		−6			−6				
16		I_R	Reference Supply Current		−0.5			−0.5				
17		I+	Positive Supply Current		15			25		μA	V_{IN} = 0.4 V, All Channels OFF	
18		I−	Negative Supply Current		−20			−40				
19		I_R	Reference Supply Current		−10			−20				

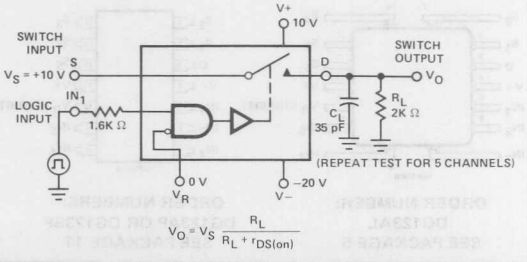
*Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

IBAF-A+MABA

SWITCHING TIME TEST CIRCUIT

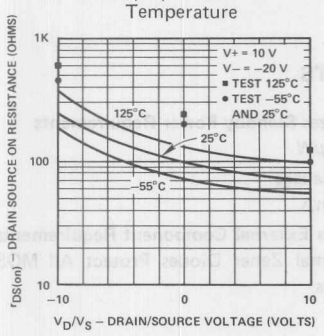
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



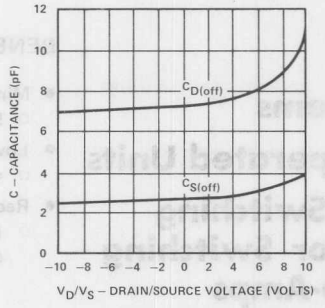


TYPICAL CHARACTERISTICS

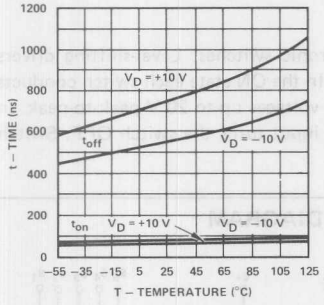
$r_{DS(on)}$ vs V_D and Temperature



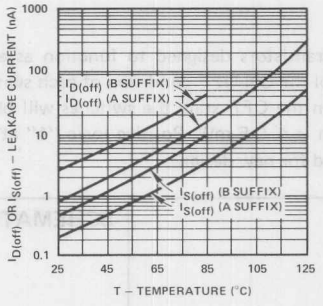
Capacitance vs V_D



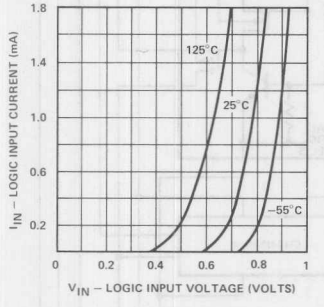
Switching Time vs V_D and Temperature



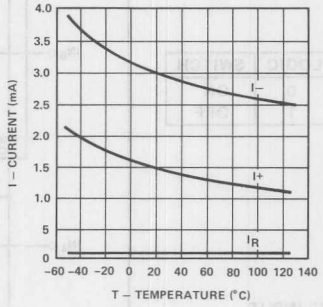
$I_{D(off)}/I_{S(off)}$ vs Temperature



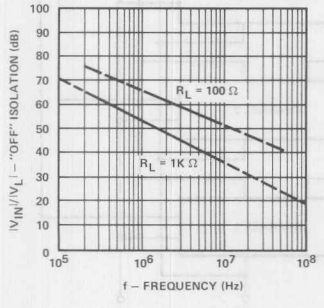
I_{IN} vs V_{IN} and Temperature

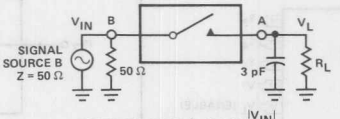


Supply Current vs Temperature



"OFF" Isolation vs R_L and Frequency

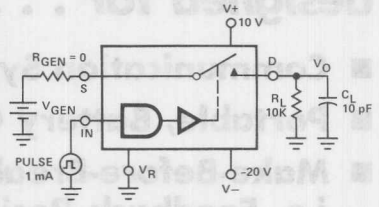




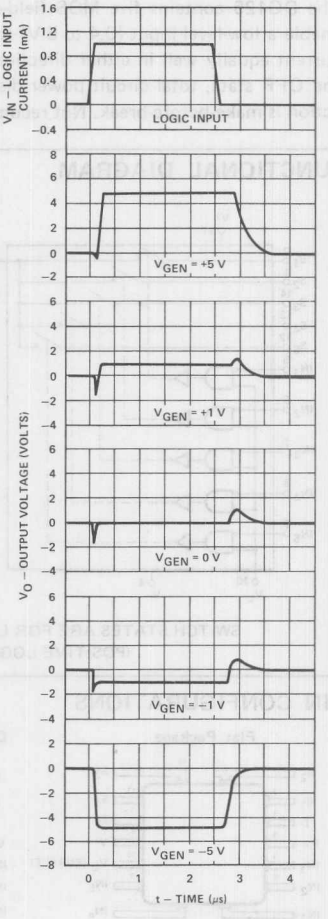
"OFF" ISOLATION $\triangleq$ 20 LOG $\frac{|V_{IN}|}{|V_L|}$

A - DRAIN OF "OFF" SWITCH
B - SOURCE OF "OFF" SWITCH

Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



designed for . . .

- **Communication Systems**
- **Portable, Battery Operated Units**
- **Make-Before-Break Switching i.e. Feedback Resistor Switching in Variable Gain Op-Amps**

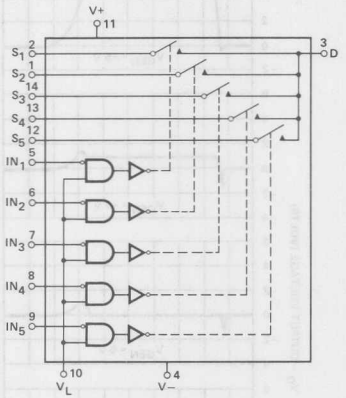
BENEFITS

- **Minimizes Standby Power Requirements**
 - 550 μW
- **Low Leakage**
 - $\leqslant$ 1 nA
- **Reduces External Component Requirements**
 - Internal Zener Diodes Protect All MOS Gates

DESCRIPTION

The DG125 contains five MOS field-effect transistors designed to function as electronic switches. Level-shifting drivers enable a low-level input (0.4 to 5 V) to control the ON-OFF condition of each switch. In the ON state each switch conducts current equally well in either direction, and in the OFF state the switches will block voltages up to 20 V peak-to-peak. In the OFF state, total circuit power dissipation is < 0.5 mW. Positive logic "1" at the input turns the switch OFF. Switch action is make-before-break. Not recommended for new designs.

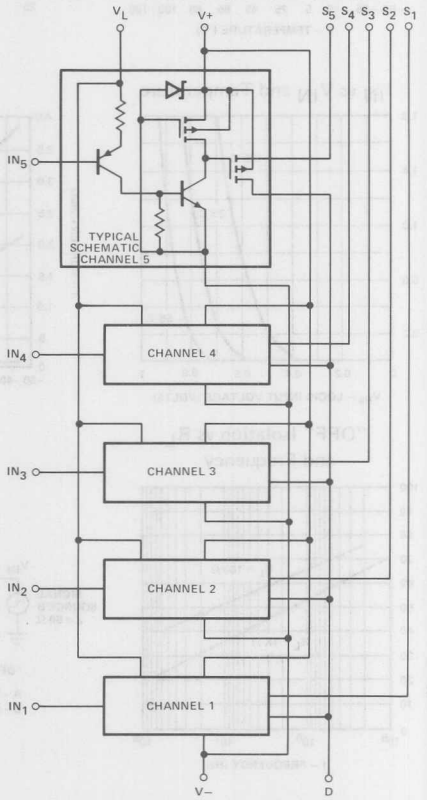
FUNCTIONAL DIAGRAM



LOGIC	SWITCH
0	ON
1	OFF

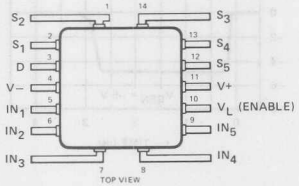
SWITCH STATES ARE FOR LOGIC "1" INPUT
(POSITIVE LOGIC)

SCHEMATIC DIAGRAM



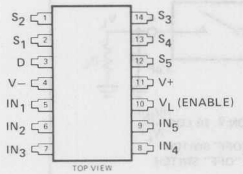
PIN CONFIGURATIONS

Flat Package



ORDER NUMBER: DG125AL
SEE PACKAGE 5

Dual-In-Line Package



ORDER NUMBERS:
DG125AP OR DG125BP
SEE PACKAGE 11

ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V_D to V−	36 V
V_S to V−	36 V
V_D to V_S	25 V
V_S to V_D	25 V
V_L to V−	30 V
V_{IN} to V−	30 V
V_L to V_{IN}	6 V
Current (Any Terminal)	30 mA

Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads soldered or welded to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

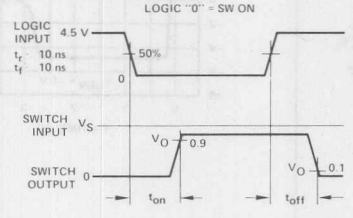
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX −20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 10 V, V− = −20 V, V_L = 4.5 V	
1	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	100	100	125	125	125	150	Ω	V_D = 10 V	I_S = −1 mA, V_{IN} = 0.5 V
2				200	200	250	225	225	300		V_D = 0	
3				450	450	600	500	500	600		V_D = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current		−1	−1000		−5	−100	nA	V_S = −10 V, V_D = 10 V	V_{IN} = 4.1 V
5		$I_{D(off)}$	Drain OFF Leakage Current		−1	−4000		−10	−300		V_D = −10 V, V_S = 10 V	
6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		4	4000		10	300		V_D = 10 V, I_S = 0	V_{IN} = 0.5 V
7	IN	I_{INL}	Logic Input Current, Input Voltage Low	-0.7	−0.7	−0.7	−1	−1	−1	mA	V_{IN} = 0.5 V	
8		I_{INH}	Logic Input Current, Input Voltage High	±1	±1	±10	±10	±10	±10	μA	V_{IN} = 4.1 V	
9	DYNAMIC	t_{on}	Turn-ON Time		0.3			0.5		μs	See Switching Time Test Circuit	
10		t_{off}	Turn-OFF Time		2			2				
11		$C_{S(off)}$	Source OFF Capacitance		3 Typ*			3 Typ*		pF	V_S = 0, I_D = 0	f = 1 MHz
12		$C_{D(off)}$	Drain OFF Capacitance		7 Typ*			7 Typ*			V_D = 0, I_S = 0	
13		Off Isolation		Typ > -50 dB at 5 MHz*							R_L = 100Ω, C_L = 3 pF	
14	SUPPLY	I+	Positive Supply Current		3			3		mA	V_{IN} = 0.5 V, One Channel ON	
15		I−	Negative Supply Current		−6			−6				
16		I_L	Logic Supply Current		3			3				
17		I+	Positive Supply Current		15			25		μA	V_{IN} = 4.1 V, All Channels OFF	
18		I−	Negative Supply Current		−20			−40				
19		I_L	Logic Supply Current		10			20				

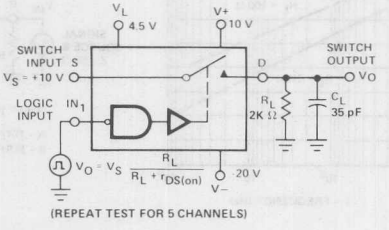
*Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

IBAF-B + MABA

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

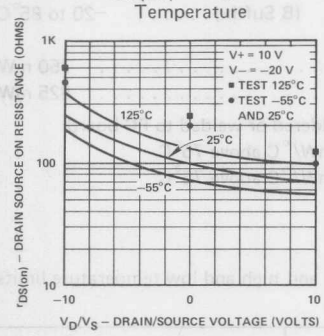




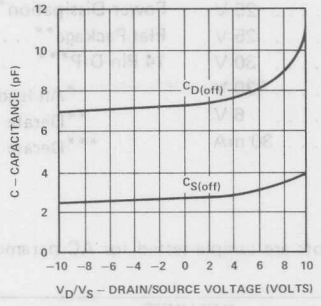
(REPEAT TEST FOR 5 CHANNELS)

TYPICAL CHARACTERISTICS

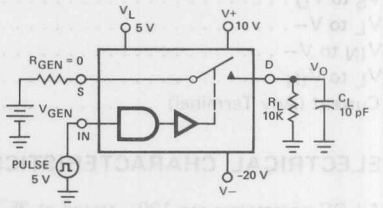
$r_{DS(on)}$ vs V_D and Temperature



Capacitance vs V_D

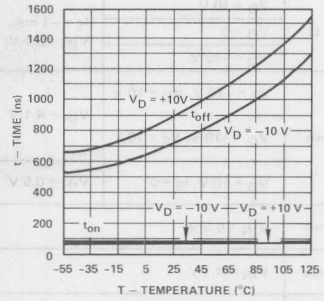


Typical delay, rise, fall, settling times, and switching transients in this circuit.

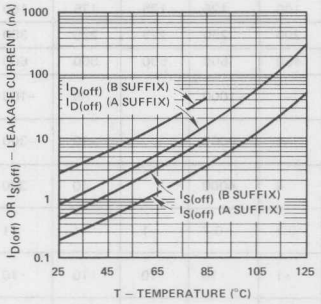


If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

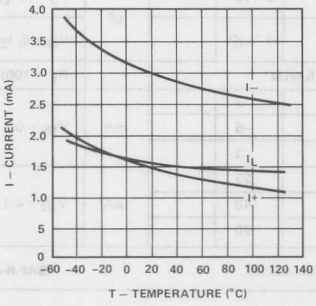
Switching Time vs V_D and Temperature



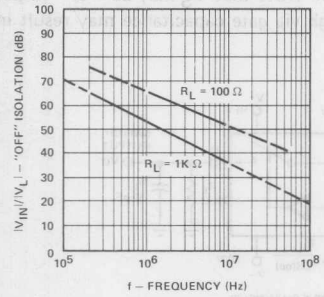
$I_{D(off)}/I_{S(off)}$ vs Temperature

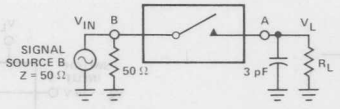


Supply Current vs Temperature



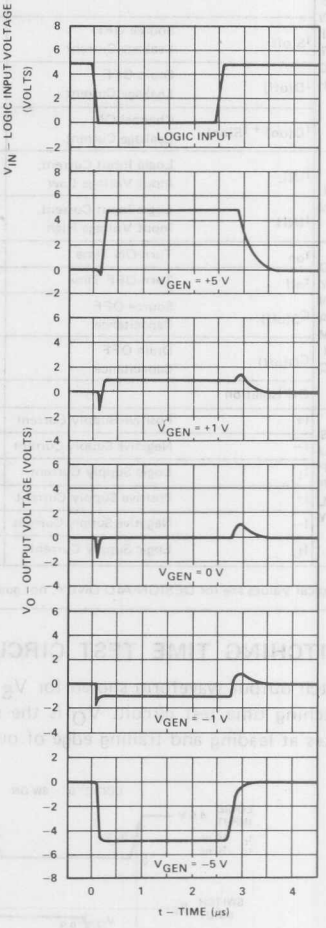
"OFF" Isolation vs R_L and Frequency





"OFF" ISOLATION ≙ 20 LOG $\frac{|V_{IN}|}{|V_L|}$

A - DRAIN OF "OFF" SWITCH
B - SOURCE OF "OFF" SWITCH



2-Channel Drivers with SPST and DPST FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

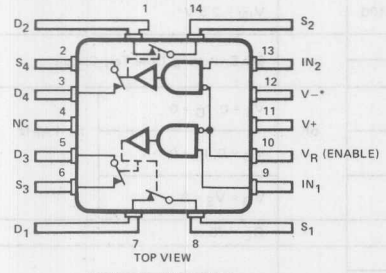
- **Higher Signal Bandwidth Switching Capabilities**
 - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
 - Bipolar Drivers
- **Minimizes Standby Power Requirements**
 - <1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
 - Constant ON Resistance

DESCRIPTION

These switching circuits contain two channels in one package; each channel consists of a driver circuit controlling SPST or DPST junction FET switches. The driver interfaces with DTL, TTL or RTL logic signals for multiplexing, commutating, and D/A converter applications. Logic "1" at the input turns the FET switch ON, and logic "0" turns it OFF. Switches have make-before-break action. It is recommended that the DG185 and DG182 be used for new designs.

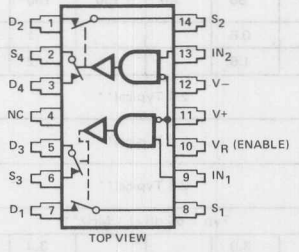
PIN CONFIGURATIONS

Flat Package



ORDER NUMBER:
DG126AL
SEE PACKAGE 5

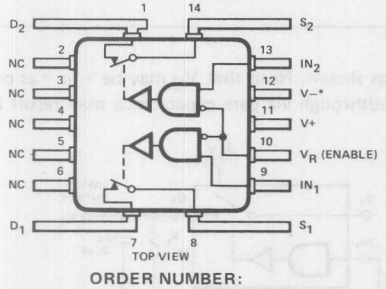
Dual-In-Line Package



ORDER NUMBERS:
DG126AP OR DG126BP
SEE PACKAGE 11

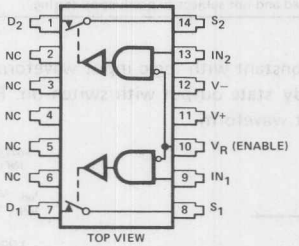
LOGIC	SWITCH
0	OFF
1	ON

Flat Package



ORDER NUMBER:
DG134AL
SEE PACKAGE 5

Dual-In-Line Package

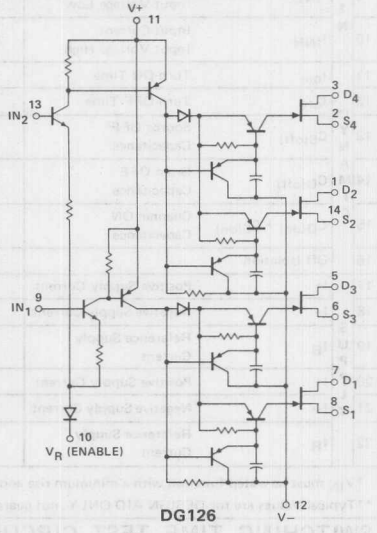


ORDER NUMBERS:
DG134AP OR DG134BP
SEE PACKAGE 11

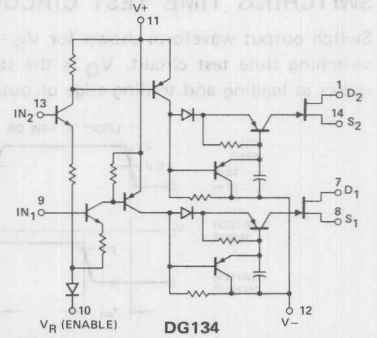
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR LOGIC "1" INPUT

SCHEMATIC DIAGRAMS



DG126



DG134

ABSOLUTE MAXIMUM RATINGS

V_R to V−	25 V	Flat Package**	750 mW
V_{IN} to V−	30 V	14 Pin DIP***	825 mW
V+ to V_{IN}	25 V		
V_{IN} to V_R	±6 V		

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

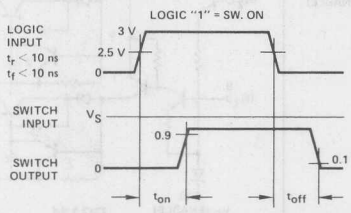
		CHARACTERISTIC		MAX LIMITS DG126A, DG134A −55°C	25°C	125°C	MAX LIMITS DG126B, DG134B −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 12 V, V− = −18 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	80	80	150				Ω	V_D = 10 V	I_S = −10 mA, V_{IN} = 2.5 V*
2							100	100	150		V_D = 8 V	
3		$I_{S(off)}$	Source OFF Leakage Current		1	100				nA	V_S = 10 V, V_D = −10 V	V_{IN} = 0.8 V*
4								5	100		V_S = 8 V, V_D = −8 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		1	100					V_D = 10 V, V_S = −10 V	
6								5	100		V_D = 8 V, V_S = −8 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −10 V	V_{IN} = 2.5 V*
8								−5	−100		V_D = V_S = −8 V	
9	IN	I_{INL}	Input Current, Input Voltage Low	0.1	0.1	2	4	4	4	μA	V_{IN} = 0.8 V*	
10		I_{INH}	Input Current, Input Voltage High	120	60	60	150	100	100		V_{IN} = 2.5 V*	
11	DYNAMIC	t_{on}	Turn-ON Time		0.6			1		μs	See Switching Time Test Circuit	
12		t_{off}	Turn-OFF Time		1.6			2				
13		$C_{S(off)}$	Source OFF Capacitance	2.4 Typical**						pF	V_S = 0, I_D = 0	f = 1 MHz
14		$C_{D(off)}$	Drain OFF Capacitance	2.4 Typical**							V_D = 0, I_S = 0	
15		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	2.8 Typical**							V_D = V_S = 0	
16		Off Isolation		Typ > 60 dB at 1 MHz**							R_L = 75 Ω	
17	SUPPLY	I+	Positive Supply Current		3.0			3.3		mA	V_{IN} = 2.5 V, One Channel ON	
18		I−	Negative Supply Current		−1.8			−2.0				
19		I_R	Reference Supply Current		−1.4			−1.5				
20		I+	Positive Supply Current		25			25		μA	Both V_{IN} = 0*, All Channels OFF	
21		I−	Negative Supply Current		−25			−25				
22		I_R	Reference Supply Current		−25			−25				

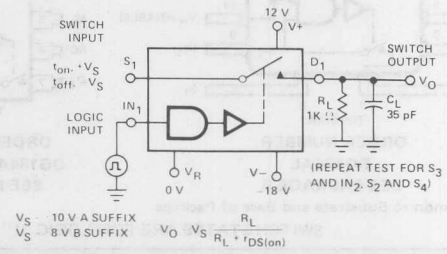
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.
**Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODC + NC

SWITCHING TIME TEST CIRCUIT

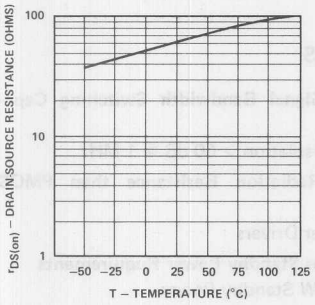
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



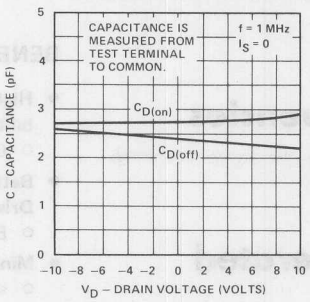


TYPICAL CHARACTERISTICS

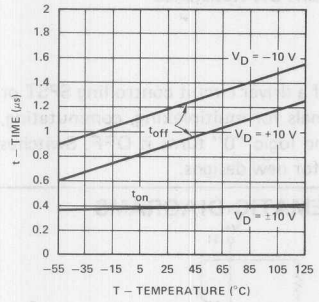
$r_{DS(on)}$ vs Temperature



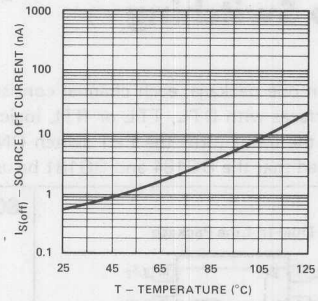
Capacitance vs V_D



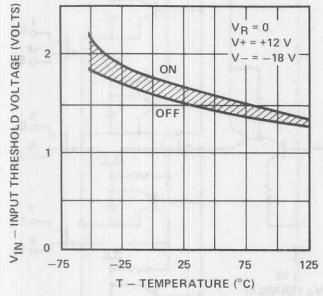
Switching Time vs V_D and Temperature



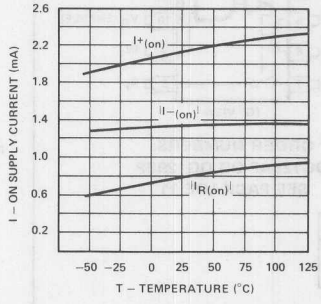
$I_{S(off)}$ vs Temperature



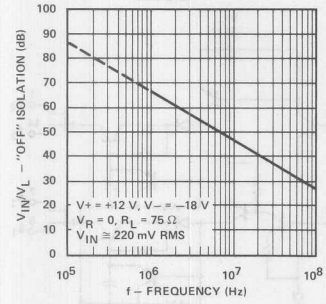
V_{IN} vs Temperature



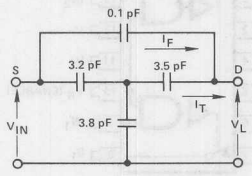
Supply Current vs Temperature



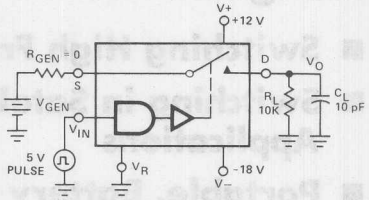
"OFF" Isolation vs R_L and Frequency



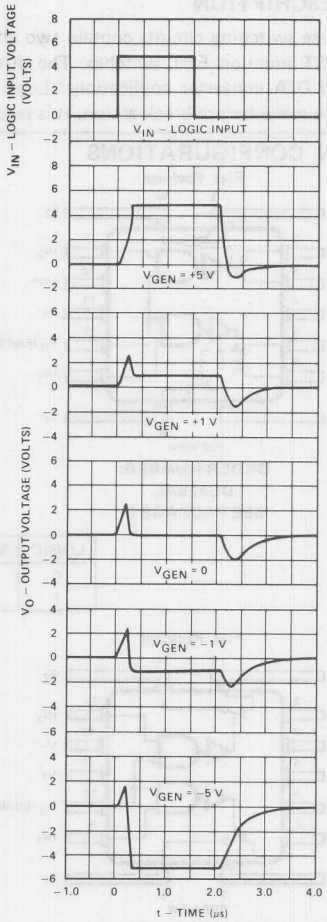
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



2-Channel Drivers with SPST and DPST FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

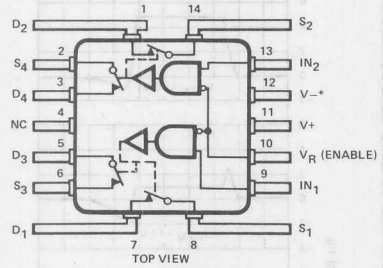
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 - <1 mW Standby Power
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DESCRIPTION

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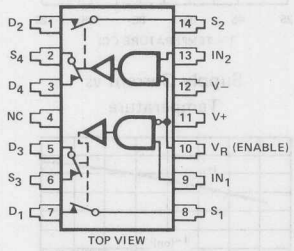
PIN CONFIGURATIONS

Flat Package



ORDER NUMBER:
DG129AL
SEE PACKAGE 5

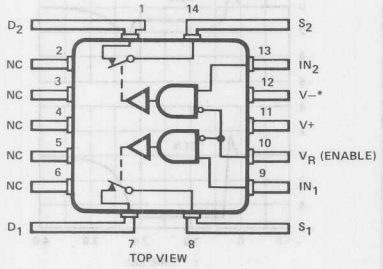
Dual-In-Line Package



ORDER NUMBERS:
DG129AP OR DG129BP
SEE PACKAGE 11

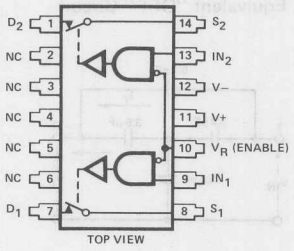
LOGIC	SWITCH
0	OFF
1	ON

Flat Package



ORDER NUMBER:
DG133AL
SEE PACKAGE 5

Dual-In-Line Package

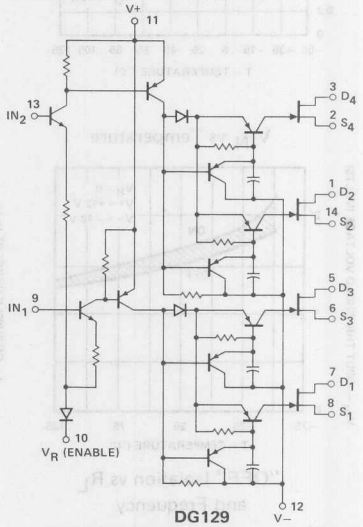


ORDER NUMBERS:
DG133AP OR DG133BP
SEE PACKAGE 11

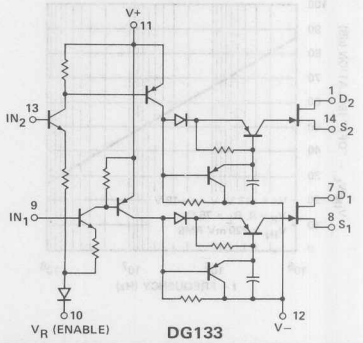
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR LOGIC "1" INPUT

SCHEMATIC DIAGRAMS



DG129



DG133

ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_D	36 V
V_D or V_S to V−	36 V
V_D to V_S	±22 V
V+ to V_R	25 V
V_R to V−	25 V
V_{IN} to V−	30 V
V+ to V_{IN}	25 V
V_{IN} to V_R	±6 V

Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

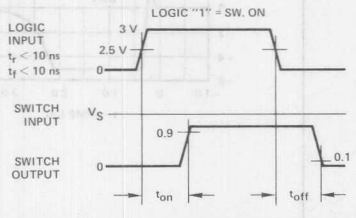
		CHARACTERISTIC		MAX LIMITS DG129A, DG133A −55°C	25°C	125°C	DG129B, DG133B −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 12 V, V− = −18 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	30	30	60				Ω	V_D = 10 V	I_S = −10 mA, V_{IN} = 2.5 V*
2							50	50	75		V_D = 8 V	
3		$I_{S(off)}$	Source OFF Leakage Current		1	100				nA	V_S = 10 V, V_D = −10 V	V_{IN} = 0.8 V*
4								5	100		V_S = 8 V, V_D = −8 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		1	100					V_D = 10 V, V_S = −10 V	
6								5	100		V_D = 8 V, V_S = −8 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −10 V	V_{IN} = 2.5 V*
8								−5	−100		V_D = V_S = −8 V	
9	IN	I_{INL}	Input Current, Input Voltage Low	0.1	0.1	2	4	4	4	μA	V_{IN} = 0.8 V*	
10		I_{INH}	Input Current, Input Voltage High	120	60	60	150	100	100		V_{IN} = 2.5 V*	
11	DYNAMIC	t_{on}	Turn-ON Time		0.6			1		μs	See Switching Time Test Circuit	
12		t_{off}	Turn-OFF Time		1.6			2				
13		$C_{S(off)}$	Source OFF Capacitance	2.4 Typical**						pF	V_S = 0, I_D = 0	f = 1 MHz
14		$C_{D(off)}$	Drain OFF Capacitance	2.4 Typical**							V_D = 0, I_S = 0	
15		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	2.8 Typical**							V_D = V_S = 0	
16		Off Isolation		Typ > 60 dB at 1 MHz**							R_L = 75 Ω	
17	SUPPLY	I+	Positive Supply Current		3.0			3.3		mA	V_{IN} = 2.5V*, One Channel ON	
18		I−	Negative Supply Current		−1.8			−2.0				
19		I_R	Reference Supply Current		−1.4			−1.5				
20		I+	Positive Supply Current		25			25		μA	Both V_{IN} = 0*, All Channels OFF	
21		I−	Negative Supply Current		−25			−25				
22		I_R	Reference Supply Current		−25			−25				

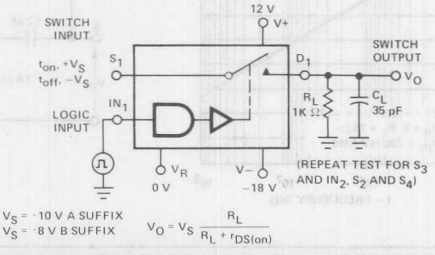
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.
**Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

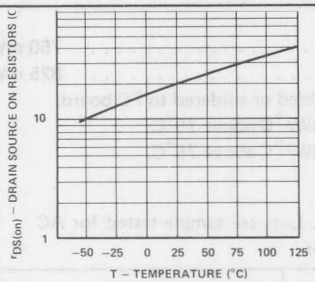
LODC + NC

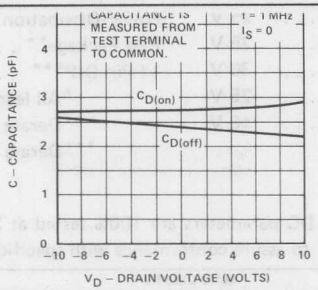
SWITCHING TIME TEST CIRCUIT

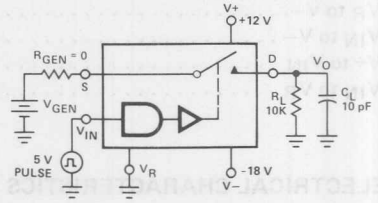
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





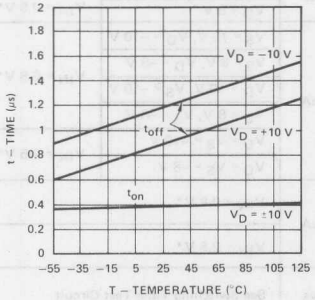




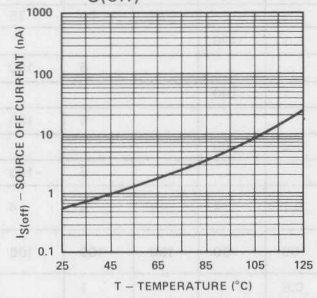


If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

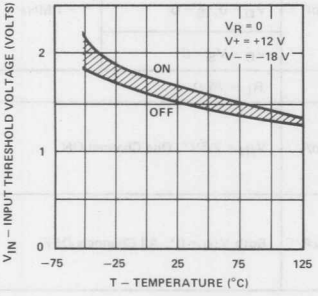
Switching Time vs V_D and Temperature



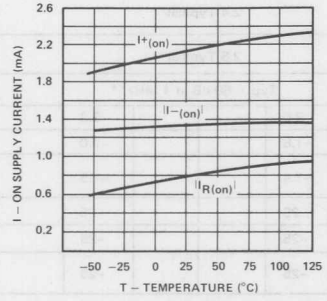
$I_{S(off)}$ vs Temperature



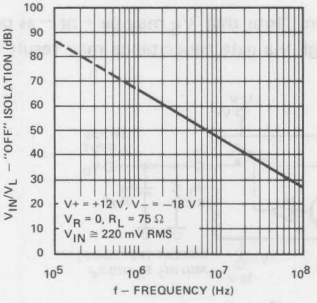
V_{IN} vs Temperature



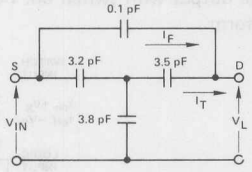
Supply Current vs Temperature

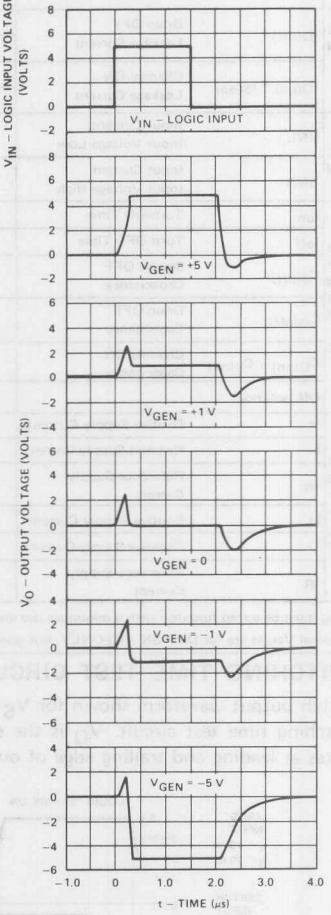


"OFF" Isolation vs R_L and Frequency



Equivalent "OFF" Circuit





Drivers with Normally Open & Normally Closed FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

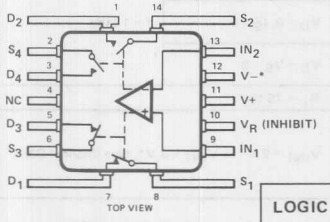
- **Higher Signal Bandwidth Switching Capabilities**
 - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
 - Bipolar Drivers
- **Minimizes Standby Power Requirements**
 - <1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
 - Constant ON Resistance

DESCRIPTION

The DG139 contains four junction-type field-effect transistors designed to function as electronic switches. Level-shifting drivers enable low-level inputs (2 to 3 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN_2 connected to a 2.5 voltage reference, a positive logic "0" at input IN_1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN_1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally-grounded V_R terminal may be used as an "Inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to V_R. In the ON state, each switch conducts equally well in either direction, has a series resistance of < 30 ohms, and a shunt leakage of < 2 nA. In the OFF state the switches will hold off voltages up to 20 V peak-to-peak. Switches have make-before-break action. The DG144 is similar to the DG139, except that it contains two FET switches instead of four. It is recommended that the DG190 and DG187 be used for new designs.

PIN CONFIGURATIONS

Flat Package

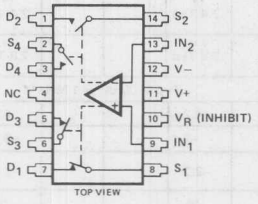


DPDT

LOGIC	SW 1 SW 3	SW 2 SW 4
0	OFF	ON
1	ON	OFF

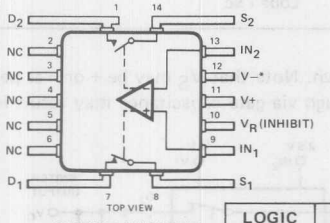
ORDER NUMBER:
DG139AL
SEE PACKAGE 5

Dual-In-Line Package



ORDER NUMBERS:
DG139AP OR DG139BP
SEE PACKAGE 11

Flat Package

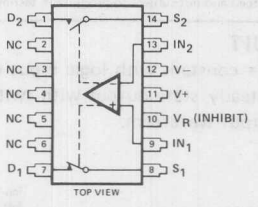


SPDT

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

ORDER NUMBER:
DG144AL
SEE PACKAGE 5

Dual-In-Line Package

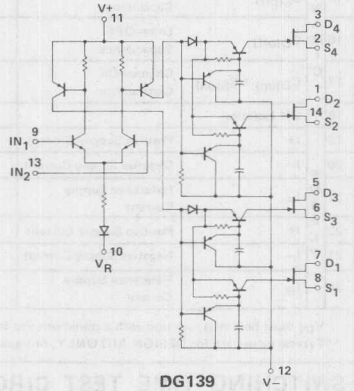


ORDER NUMBERS:
DG144AP OR DG144BP
SEE PACKAGE 11

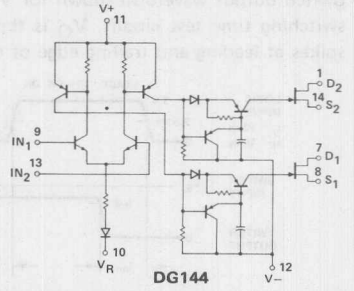
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR
V_{IN1} = LOGIC "1" INPUT AND V_{IN2} = 2.5 V BIAS
(POSITIVE LOGIC)

SCHEMATIC DIAGRAMS



DG139



DG144

ABSOLUTE MAXIMUM RATINGS

V+ to V–, V_D or V_S	36 V
V_D or V_S to V–	36 V
V_D to V_S	±22 V
V+ to V_R	25 V
V+ to V_{IN1} or V_{IN2}	25 V
V_R to V–	25 V
V_{IN1} to V_{IN2}	±6 V
V_{IN1} or V_{IN2} to V_R	±6 V
V_{IN1} or V_{IN2} to V–	30 V
Current (Any Terminal)	30 mA

Storage Temperature	–65 to 150°C
Operating Temperature (A Suffix)	–55 to 125°C
(B Suffix)	–20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

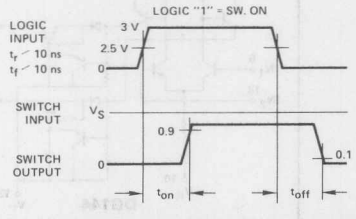
		CHARACTERISTIC		MAX LIMITS A SUFFIX –55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX –20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 12 V, V– = –18 V, V_R = 0, V_{IN2} = 2.5 V*	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	30	30	60				Ω	V_D = 10 V	I_S = –10 mA, V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
2							50	50	75		V_D = 8 V	
3		$I_{S(off)}$	Source OFF Leakage Current		1	100				nA	V_S = 10 V, V_D = –10 V	V_{IN1} = 2 V* ($SW_{1,3}$ OFF), V_{IN1} = 3 V* ($SW_{2,4}$ OFF)
4								5	100		V_S = 8 V, V_D = –8 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		1	100					V_D = 10 V, V_S = –10 V	
6								5	100		V_D = 8 V, V_S = –8 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		–2	–100					V_D = V_S = –10 V	V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
8								–5	–100		V_D = V_S = –8 V	
9	IN	I_{IN1L}	Input 1 Current, Input 1 Voltage Low	0.1	0.1	2	4	4	4	µA	V_{IN1} = 2 V*	
10		I_{IN2L}	Input 2 Current, Input 2 Voltage Low	0.1	0.1	2	4	4	4		V_{IN2} = 2 V*, V_{IN1} = 2.5 V*	
11		I_{IN1H}	Input 1 Current, Input 1 Voltage High	120	60	60	150	100	100		V_{IN1} = 3 V*	
12		I_{IN2H}	Input 2 Current, Input 2 Voltage High	120	60	60	150	100	100		V_{IN2} = 3 V*, V_{IN1} = 2.5 V*	
13	DYNAMIC	t_{on}	Turn-ON Time		0.8			1		µs	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time		1.6			2				
15		$C_{S(off)}$	Source OFF Capacitance		** 2.4 Typ			** 2.4 Typ		pF	V_S = 0, I_D = 0	f = 1 MHz
16		$C_{D(off)}$	Drain OFF Capacitance		** 2.4 Typ			** 2.4 Typ			V_D = 0, I_S = 0	
17		$C_{D(on)} + C_{S(on)}$	Channel On Capacitance		** 2.8 Typ			** 2.8 Typ			V_D = V_S = 0	
18		Off Isolation		Typ > 60 dB at 1 MHz**							R_L = 75 Ω	
19	SUPPLY	I+	Positive Supply Current		4.2			4.5		mA	V_{IN1} = 2 V* or V_{IN1} = 3 V*, One Channel ON	
20		I–	Negative Supply Current		–2			–2.2				
21		I_R	Reference Supply Current		–2.2			–2.4				
22		I+	Positive Supply Current		25			25		µA	V_{IN1} = V_{IN2} = 0.8 V*, All Channels OFF	
23		I–	Negative Supply Current		–25			–25				
24		I_R	Reference Supply Current		–25			–25				

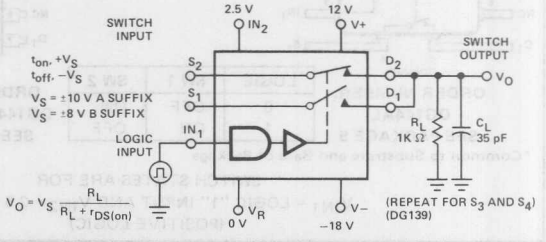
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/µs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODF + NC

SWITCHING TIME TEST CIRCUIT

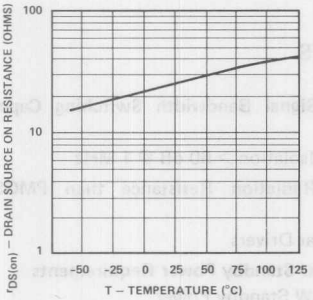
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



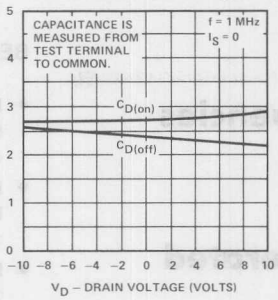


TYPICAL CHARACTERISTICS

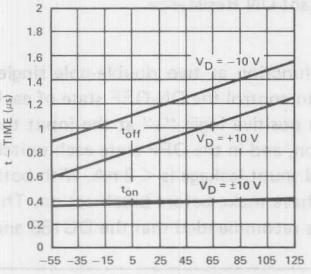
$r_{DS(on)}$ vs Temperature



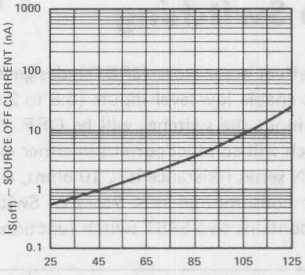
Capacitance vs V_D



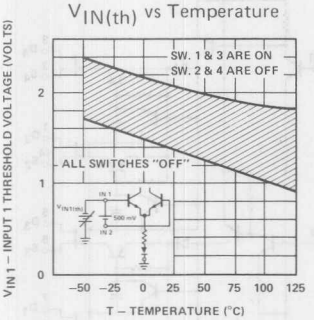
Switching Time vs V_D and Temperature



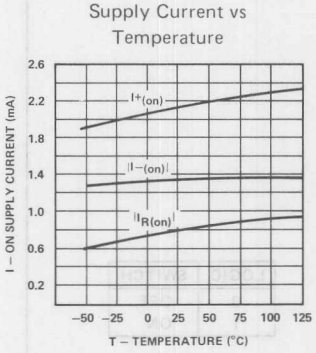
$I_{S(off)}$ vs Temperature



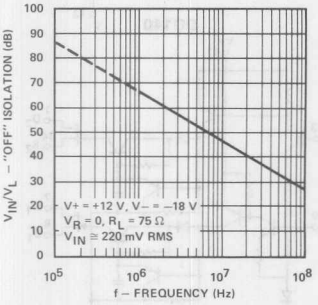
$V_{IN(th)}$ vs Temperature



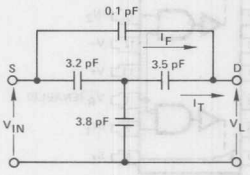
Supply Current vs Temperature



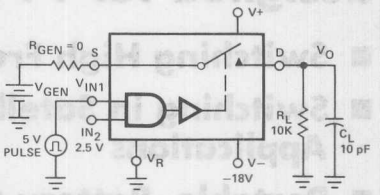
"OFF" Isolation vs R_L and Frequency



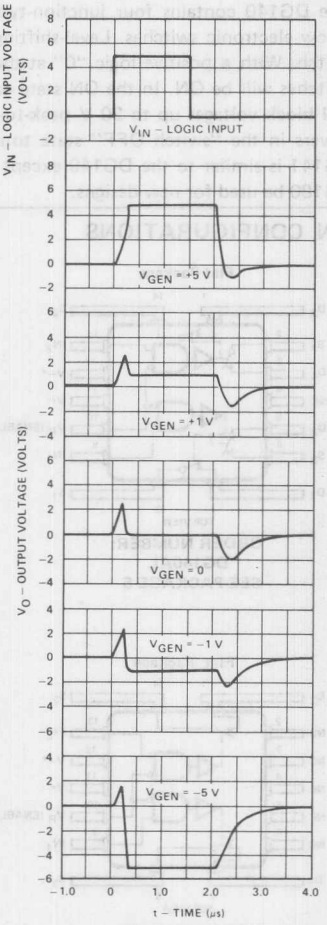
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

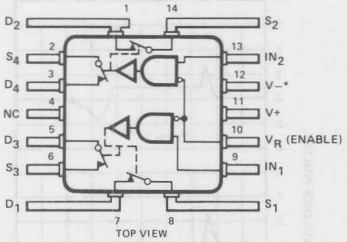
- **Higher Signal Bandwidth Switching Capabilities**
 - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
 - Bipolar Drivers
- **Minimizes Standby Power Requirements**
 - <1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
 - Constant ON Resistance

DESCRIPTION

The DG140 contains four junction-type field-effect transistors (JFETs) designed to function as two double-pole single-throw electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2.5 V) to control the ON-OFF state of each switch. With a positive logic "0" at the driver input the switches will be OFF. With a positive logic "1" at the input the switches will be ON. In the ON state each switch will conduct current in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. ON series resistance is < 10 ohms, and ON shunt leakage is < 2 nA. With both drivers in the "switch OFF" state total power consumption is < 750 μW. Switches have make-before-break action. The DG141 is similar to the DG140 except that it contains two SPST switch functions. It is recommended that the DG183 and DG180 be used for new designs.

PIN CONFIGURATIONS

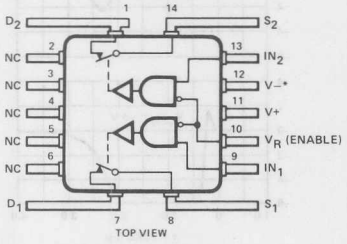
Flat Package



ORDER NUMBER:
DG140AL
SEE PACKAGE 5

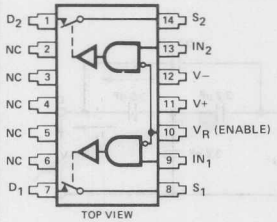
LOGIC	SWITCH
0	OFF
1	ON

Flat Package



ORDER NUMBER:
DG141AL
SEE PACKAGE 5

Dual-In-Line Package

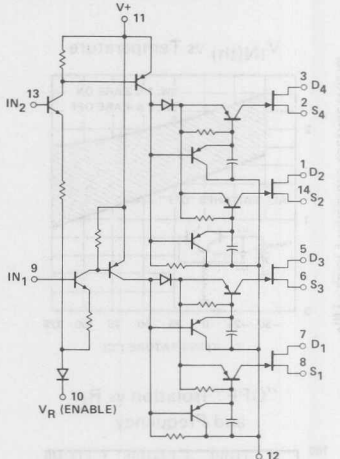


ORDER NUMBERS:
DG141AP OR DG141BP
SEE PACKAGE 11

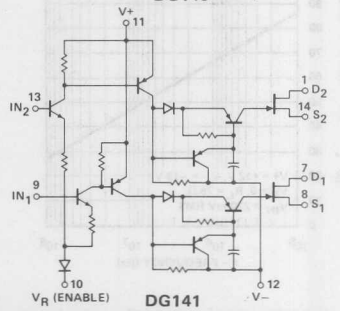
*Common to Substrate and Base of Package

SWITCH STATES ARE LOGIC "1" INPUT

SCHEMATIC DIAGRAMS



DG140



DG141

ABSOLUTE MAXIMUM RATINGS

$V+$ to $V-$	36 V	Storage Temperature	−65 to 150°C
$V+$ to V_D or V_S	36 V	Operating Temperature (A Suffix)	−55 to 125°C
V_D or V_S to $V-$	32 V	(B Suffix)	−20 to 85°C
V_D to V_S	±22 V	Power Dissipation*	
$V+$ to V_R	25 V	Flat Package**	750 mW
V_R to $V-$	25 V	14 Pin DIP***	825 mW
V_{IN} to $V-$	30 V		
$V+$ to V_{IN}	25 V		
V_{IN} to V_R	±6 V		
Current (Any Terminal)	30 mA		

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

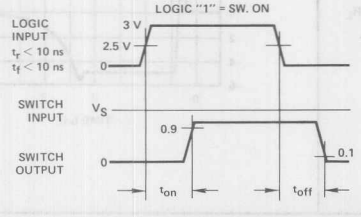
		CHARACTERISTIC		MAX LIMITS DG140A, DG141A −55°C	DG140A, DG141A 25°C	DG140A, DG141A 125°C	DG140B, DG141B −20°C	DG140B, DG141B 25°C	DG140B, DG141B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: $V+ = 12$ V, $V- = -18$ V, $V_R = 0$	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	10	10	20				Ω	$V_D = 10$ V	$I_S = -10$ mA, $V_{IN} = 2.5$ V*
2							15	15	25		$V_D = 8$ V	
3		$I_{S(off)}$	Source OFF Leakage Current		10	1000				nA	$V_S = 10$ V, $V_D = -10$ V	$V_{IN} = 0.8$ V*
4								15	300		$V_S = 8$ V, $V_D = -8$ V	
5		$I_{D(off)}$	Drain OFF Leakage Current		10	1000					$V_D = 10$ V, $V_S = -10$ V	
6								15	300		$V_D = 8$ V, $V_S = -8$ V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					$V_D = V_S = -10$ V	$V_{IN} = 2.5$ V*
8								−5	−100		$V_D = V_S = -8$ V	
9	IN	I_{INL}	Input Current, Input Voltage Low	0.1	0.1	2	4	4	4	μA	$V_{IN} = 0.8$ V*	
10		I_{INH}	Input Current, Input Voltage High	120	60	60	150	100	100		$V_{IN} = 2.5$ V*	
11	DYNAMIC	t_{on}	Turn-ON Time		1			1.5		μs	See Switching Time Test Circuit	
12		t_{off}	Turn-OFF Time		2.5			2.5				
13		$C_{S(off)}$	Source OFF Capacitance		**3 Typ			**3 Typ		pF	$V_S = 0$, $I_D = 0$	f = 1 MHz
14		$C_{D(off)}$	Drain OFF Capacitance		**3 Typ			**3 Typ			$V_D = 0$, $I_S = 0$	
15		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		**2.8 Typ			**2.8 Typ			$V_D = V_S = 0$	
16		Off Isolation		Typ > 50 dB at 1 MHz**							$R_L = 100$ Ω, $C_L = 3$ pF	
17	SUPPLY	I+	Positive Supply Current		3			3.3		mA	$V_{IN} = 2.5$ V*, One Channel ON	
18		I−	Negative Supply Current		−1.8			−2				
19		I_R	Reference Supply Current		−1.4			−1.5				
20		I+	Positive Supply Current		25			25		μA	Both $V_{IN} = 0$*, All Channels OFF	
21		I−	Negative Supply Current		−25			−25				
22		I_R	Reference Supply Current		−25			−25				

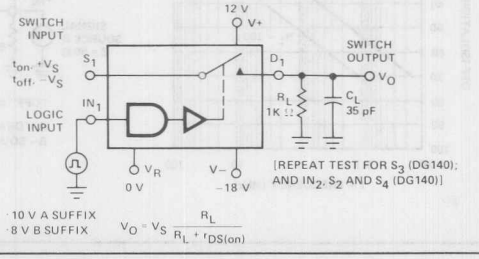
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.
**Typical values are for DESIGN AID only, not guaranteed and not subject to production testing.

LODC + NIP

SWITCHING TIME TEST CIRCUIT

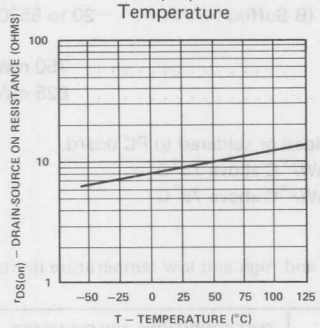
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



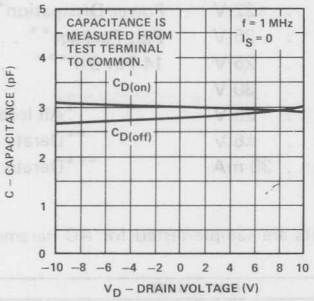


TYPICAL CHARACTERISTICS

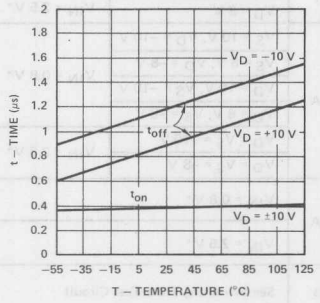
$r_{DS(on)}$ vs Temperature



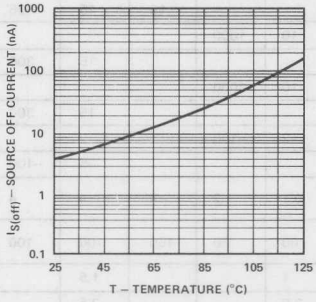
Capacitance vs V_D



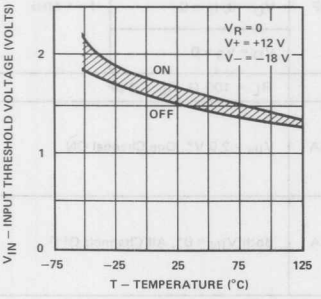
Switching Time vs V_D and Temperature



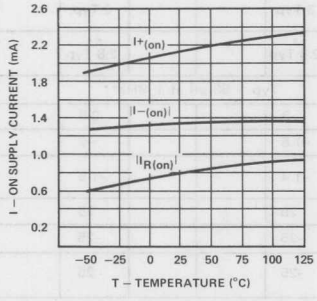
$I_{S(off)}$ vs Temperature



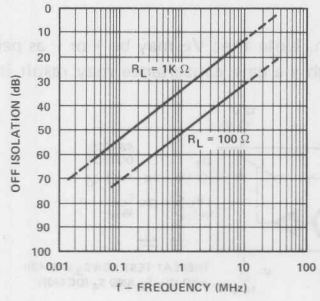
$V_{IN(th)}$ vs Temperature

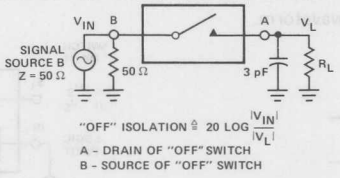


Supply Current vs Temperature

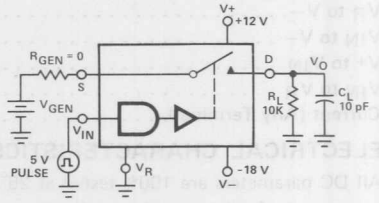


"OFF" Isolation vs R_L and Frequency

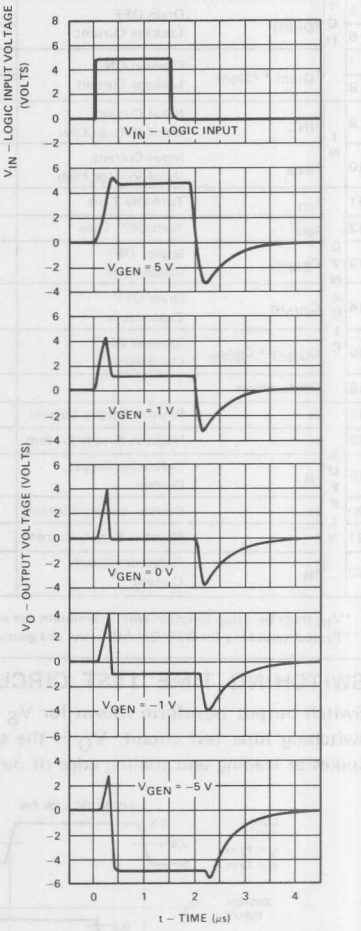




Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



Drivers with Normally Open & Normally Closed Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

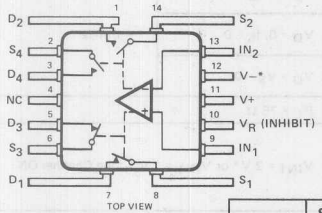
- **Higher Signal Bandwidth Switching Capabilities**
 - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
 - Bipolar Drivers
- **Minimizes Standby Power Requirements**
 - <1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
 - Constant ON Resistance

DESCRIPTION

The DG142 contains four junction-type field-effect transistors designed to function as electronic switches. Level-shifting drivers enable low-level inputs (2 to 3 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN_2 connected to a 2.5 voltage reference, a positive logic "0" at input IN_1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN_1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally-grounded V_R terminal may be used as an "Inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to V_R. In the ON state, each switch conducts equally well in either direction, has a series resistance of < 80 ohms, and a shunt leakage of < 2 nA. In the OFF state the switches will hold off voltages up to 20 V peak-to-peak. Switches have make-before-break action. The DG143 is similar to the DG142, except that it contains two FET switches instead of four. It is recommended that the DG191 and DG188 be used for new designs.

PIN CONFIGURATIONS

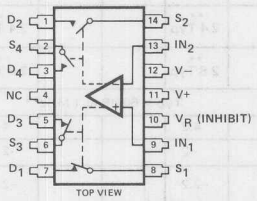
Flat Package



ORDER NUMBER:
DG142AL
SEE PACKAGE 5

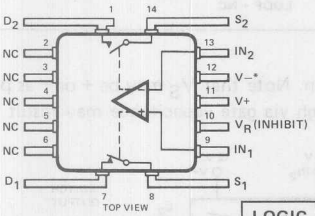
LOGIC	SW 1 SW 3	SW 2 SW 4
0	OFF	ON
1	ON	OFF

Dual-In-Line Package



ORDER NUMBERS:
DG142AP OR DG142BP
SEE PACKAGE 11

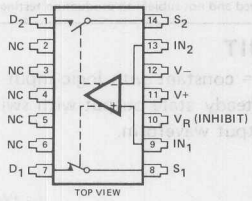
Flat Package



ORDER NUMBER:
DG143AL
SEE PACKAGE 5

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

Dual-In-Line Package

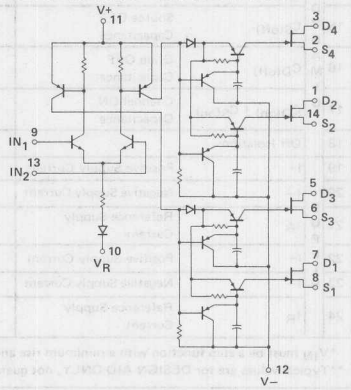


ORDER NUMBERS:
DG143AP OR DG143BP
SEE PACKAGE 11

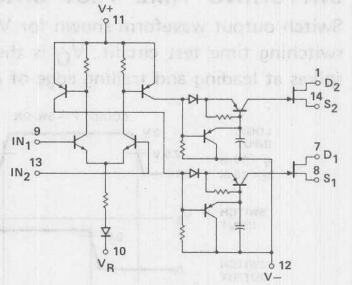
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR
V_{IN1} = LOGIC "1" INPUT AND V_{IN2} = 2.5 V BIAS
(POSITIVE LOGIC)

SCHEMATIC DIAGRAMS



DG142



DG143

$V+$ to V_R	25 V
$V+$ to V_{IN1} or V_{IN2}	25 V
V_R to $V-$	25 V
V_{IN1} to V_{IN2}	±6 V
V_{IN1} or V_{IN2} to V_R	±6 V
V_{IN1} or V_{IN2} to $V-$	30 V
Current (Any Terminal)	30 mA

Power Dissipation*

Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

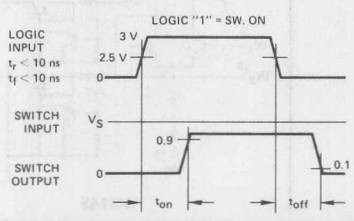
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	25°C	125°C	MAX LIMITS B SUFFIX −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 12 V, V− = −18 V, V_R = 0, V_{IN2} = 2.5V*	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	80	80	150				Ω	V_D = 10 V	I_S = −10 mA, V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
2							100	100	150		V_D = 8 V	
3		$I_{S(off)}$	Source OFF Leakage Current		1	100				nA	V_S = 10 V, V_D = −10 V	V_{IN1} = 2 V* ($SW_{1,3}$ OFF), V_{IN1} = 3 V* ($SW_{2,4}$ OFF)
4								5	100		V_S = 8 V, V_D = −8 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		1	100					V_D = 10 V, V_S = −10 V	
6								5	100		V_D = 8 V, V_S = −8 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −10 V	V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
8								−5	−100		V_D = V_S = −8 V	
9	IN	I_{IN1L}	Input 1 Current, Input 1 Voltage Low	0.1	0.1	2	4	4	4	µA	V_{IN1} = 2 V*	
10		I_{IN2L}	Input 2 Current, Input 2 Voltage Low	0.1	0.1	2	4	4	4		V_{IN2} = 2 V*, V_{IN1} = 2.5 V*	
11		I_{IN1H}	Input 1 Current, Input 1 Voltage High	120	60	60	150	100	100		V_{IN1} = 3 V*	
12		I_{IN2H}	Input 2 Current, Input 2 Voltage High	120	60	60	150	100	100		V_{IN2} = 3 V*, V_{IN1} = 2.5 V*	
13	DYNAMIC	t_{on}	Turn-ON Time		0.8			1		µs	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time		1.6			2				
15		$C_{S(off)}$	Source OFF Capacitance		** 2.4 Typ			** 2.4 Typ		pF	V_S = 0, I_D = 0	f = 1 MHz
16		$C_{D(off)}$	Drain OFF Capacitance		** 2.4 Typ			** 2.4 Typ			V_D = 0, I_S = 0	
17		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		** 2.8 Typ			** 2.8 Typ			V_D = V_S = 0	
18		Off Isolation		Typ > 60 dB at 1 MHz**							R_L = 75 Ω	
19	SUPPLY	I+	Positive Supply Current		4.2			4.5		mA	V_{IN1} = 2 V* or V_{IN1} = 3 V*, One Channel ON	
20		I−	Negative Supply Current		−2			−2.2				
21		I_R	Reference Supply Current		−2.2			−2.4				
22		I+	Positive Supply Current		25			25		µA	V_{IN1} = V_{IN2} = 0.8 V*, All Channels OFF	
23		I−	Negative Supply Current		−25			−25				
24		I_R	Reference Supply Current		−25			−25				

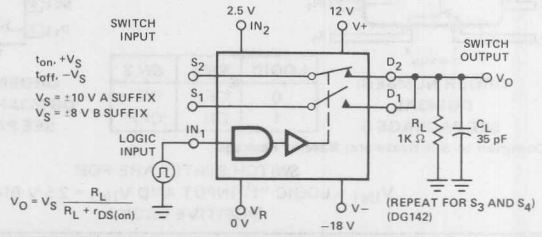
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/µs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

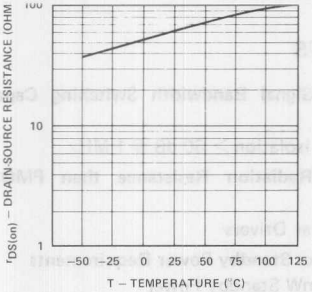
LODF + NC

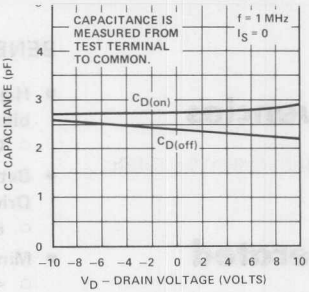
SWITCHING TIME TEST CIRCUIT

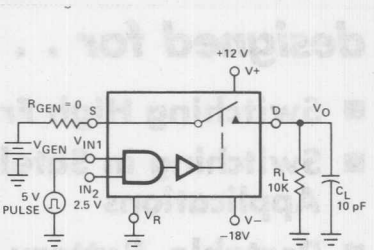
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





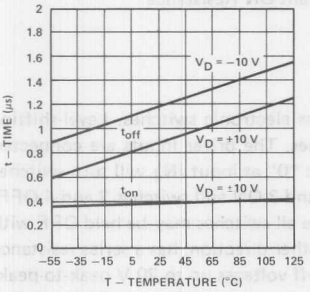




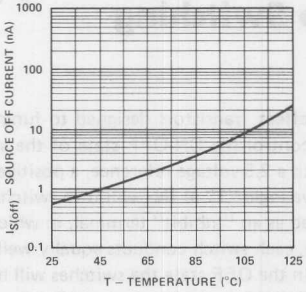


If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

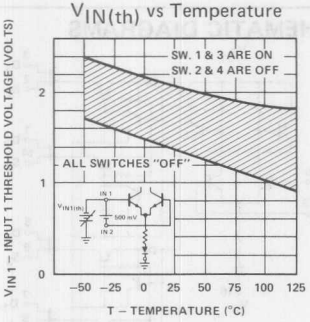
Switching Time vs V_D and Temperature



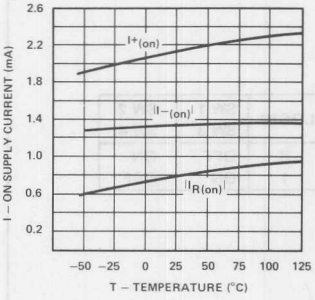
$I_{S(off)}$ vs Temperature



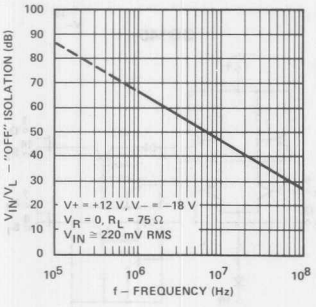
$V_{IN(th)}$ vs Temperature



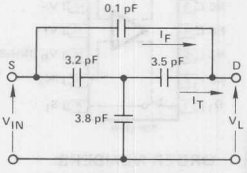
Supply Current vs Temperature

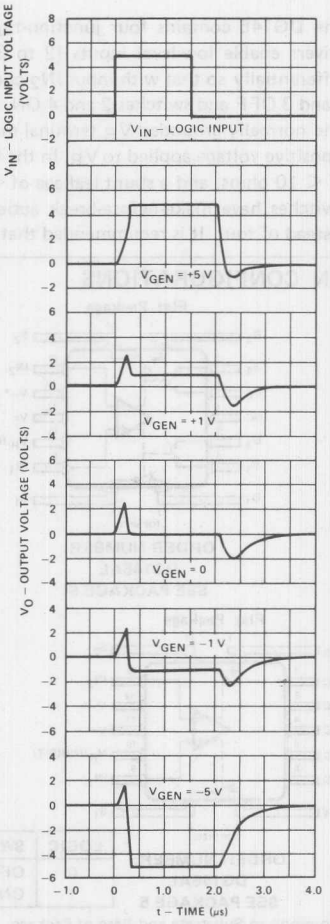


"OFF" Isolation vs R_L and Frequency



Equivalent "OFF" Circuit





Drivers with Normally Open & Normally Closed FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

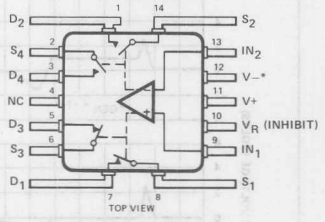
- **Higher Signal Bandwidth Switching Capabilities**
 - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
 - Bipolar Drivers
- **Minimizes Standby Power Requirements**
 - <1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
 - Constant ON Resistance

DESCRIPTION

The DG145 contains four junction-type field-effect transistors designed to function as electronic switches. Level-shifting drivers enable low-level inputs (2 to 3 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN_2 connected to a 2.5 voltage reference, a positive logic "0" at input IN_1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN_1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally-grounded V_R terminal may be used as an "Inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to V_R. In the ON state, each switch conducts equally well in either direction, has a series resistance of < 10 ohms, and a shunt leakage of < 2 nA. In the OFF state the switches will hold off voltages up to 20 V peak-to-peak. Switches have make-before-break action. The DG146 is similar to the DG145 except that it contains two FET switches instead of four. It is recommended that the DG189 and DG186 be used for new designs.

PIN CONFIGURATIONS

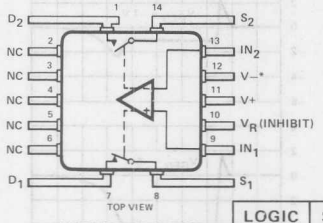
Flat Package



LOGIC	SW 1 SW 3	SW 2 SW 4
0	OFF	ON
1	ON	OFF

ORDER NUMBER:
DG145AL
SEE PACKAGE 5

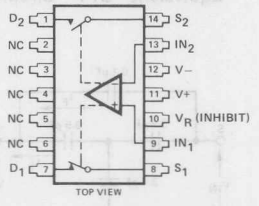
Flat Package



ORDER NUMBER:
DG146AL
SEE PACKAGE 5

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

Dual-In-Line Package

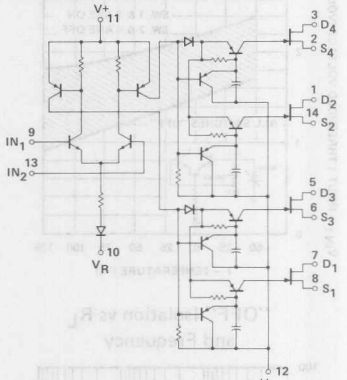


ORDER NUMBERS:
DG146AP OR DG146BP
SEE PACKAGE 11

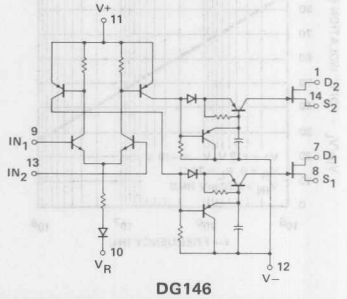
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR
V_{IN1} = LOGIC "1" INPUT AND V_{IN2} = 2.5 V BIAS
(POSITIVE LOGIC)

SCHEMATIC DIAGRAMS



DG145



DG146

ABSOLUTE MAXIMUM RATINGS

V+ to V−, V_D or V_S	36 V
V_D or V_S to V−	32 V
V_D to V_S	±22 V
V+ to V_R	25 V
V+ to V_{IN1} or V_{IN2}	25 V
V_R to V−	25 V
V_{IN1} to V_{IN2}	±6 V
V_{IN1} or V_{IN2} to V_R	±6 V
V_{IN1} or V_{IN2} to V−	30 V

Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

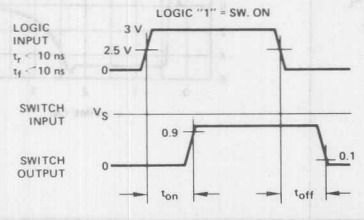
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	25°C	125°C	MAX LIMITS B SUFFIX −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 12 V, V− = −18 V, V_R = 0, V_{IN2} = 2.5 V*	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	10	10	20				Ω	V_D = 10 V	I_S = −10 mA, V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
2							15	15	25		V_D = 8 V	
3		$I_{S(off)}$	Source OFF Leakage Current		10	1000				nA	V_S = 10 V, V_D = −10 V	V_{IN1} = 2 V* ($SW_{1,3}$ OFF), V_{IN1} = 3 V* ($SW_{2,4}$ OFF)
4								15	300		V_S = 8 V, V_D = −8 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		10	1000					V_D = 10 V, V_S = −10 V	
6								15	300		V_D = 8 V, V_S = −8 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −10 V	V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
8								−5	−100		V_D = V_S = −8 V	
9	IN	I_{IN1L}	Input 1 Current, Input 1 Voltage Low	0.1	0.1	2	4	4	4	μA	V_{IN1} = 2 V*	
10		I_{IN2L}	Input 2 Current, Input 2 Voltage Low	0.1	0.1	2	4	4	4		V_{IN2} = 2 V*, V_{IN1} = 2.5 V*	
11		I_{IN1H}	Input 1 Current, Input 1 Voltage High	120	60	60	150	100	100		V_{IN1} = 3 V*	
12		I_{IN2H}	Input 2 Current, Input 2 Voltage High	120	60	60	150	100	100		V_{IN2} = 3 V*, V_{IN1} = 2.5 V*	
13	DYNAMIC	t_{on}	Turn-ON Time		1			1.5		μs	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time		2.5			2.5				
15		$C_{S(off)}$	Source OFF Capacitance		3 Typ**			3 Typ**		pF	V_S = 0, I_D = 0	f = 1 MHz
16		$C_{D(off)}$	Drain OFF Capacitance		3 Typ**			3 Typ**			V_D = 0, I_S = 0	
17		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		2.8 Typ**			2.8 Typ**			V_D = V_S = 0	
18		Off Isolation		Typ > 50 dB at f = 1 MHz**							R_L = 100 Ω, C_L = 3 pF	
19	SUPPLY	I+	Positive Supply Current		4.2			4.5		mA	V_{IN1} = 2 V* or V_{IN1} = 3 V*, One Channel ON	
20		I−	Negative Supply Current		−2			−2.2				
21		I_R	Reference Supply Current		−2.2			−2.4				
22		I+	Positive Supply Current		25			25		μA	V_{IN1} = V_{IN2} = 0.8 V*, All Channels OFF	
23		I−	Negative Supply Current		−25			−25				
24		I_R	Reference Supply Current		−25			−25				

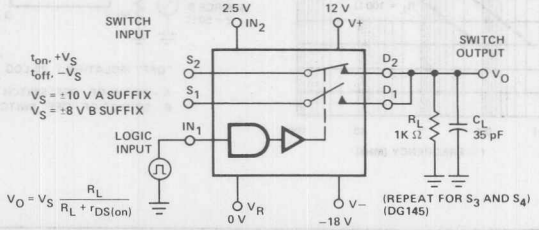
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODF + NIP

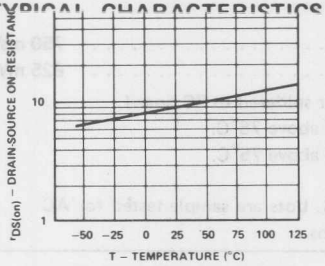
SWITCHING TIME TEST CIRCUIT

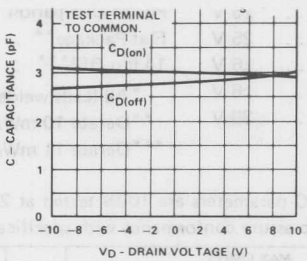
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



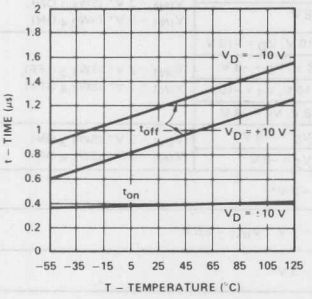


TYPICAL CHARACTERISTICS

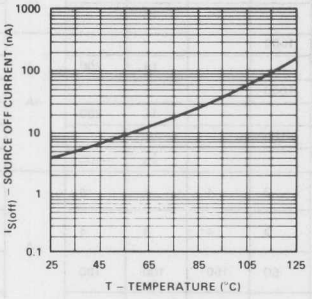




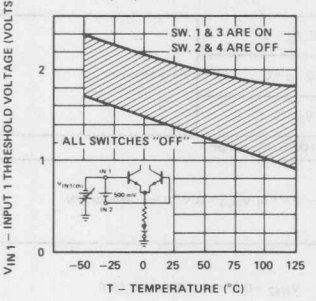
Switching Time vs V_D and Temperature



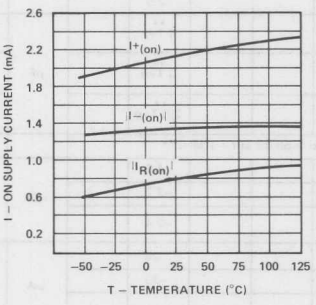
$I_{S(off)}$ vs Temperature



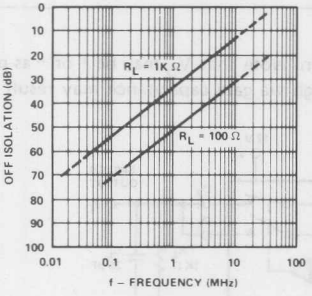
$V_{IN(th)}$ vs Temperature

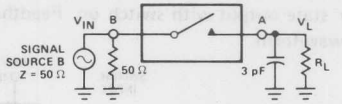


Supply Current vs Temperature



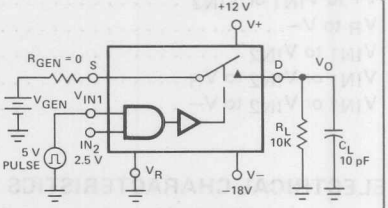
"OFF" Isolation vs R_L and Frequency



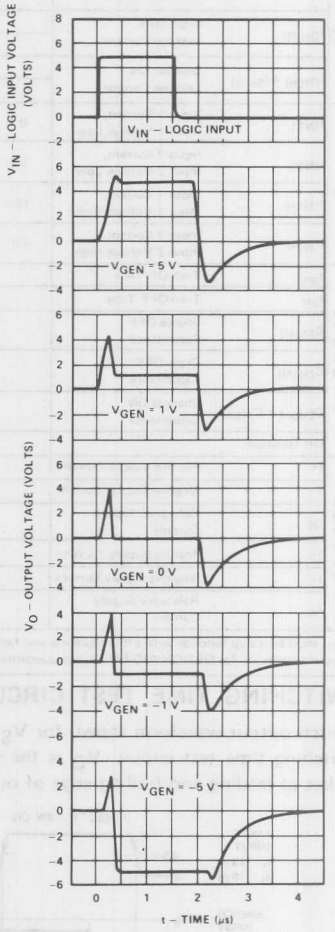


"OFF" ISOLATION ≙ 20 LOG $\frac{|V_{IN}|}{|V_L|}$

A - DRAIN OF "OFF" SWITCH
B - SOURCE OF "OFF" SWITCH



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



2-Channel Drivers with SPST and DPST FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

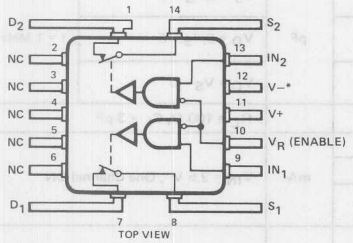
- **Higher Signal Bandwidth Switching Capabilities**
 - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
 - Bipolar Drivers
- **Minimizes Standby Power Requirements**
 - < 1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
 - Constant ON Resistance

DESCRIPTION

The DG153 contains four junction-type field-effect transistors (JFETs) designed to function as two double-pole single-throw electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2.5 V) to control the ON-OFF state of each switch. With a positive logic "0" at the driver input the switches will be OFF. With a positive logic "1" at the input the switches will be ON. In the ON state each switch will conduct current in either direction, and in the OFF state each switch will block voltages up to 15 V peak-to-peak. ON series resistance is < 15 ohms, and ON shunt leakage is < 2 nA. With both drivers in the "switch OFF" state total power consumption is < 750 μW. Switches have make-before-break action. The DG151 is similar to the DG153 except that it contains two SPST switch functions. It is recommended that the DG180 and DG183 be used for new designs.

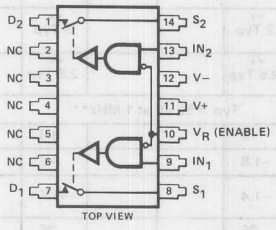
PIN CONFIGURATIONS

Flat Package



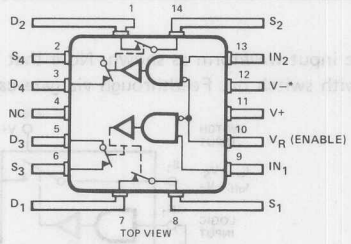
ORDER NUMBER:
DG151AL
SEE PACKAGE 5

Dual-In-Line Package



ORDER NUMBERS:
DG151AP OR DG151BP
SEE PACKAGE 11

Flat Package



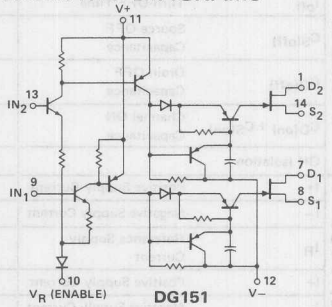
LOGIC	SWITCH
0	OFF
1	ON

ORDER NUMBER:
DG153AL
SEE PACKAGE 5

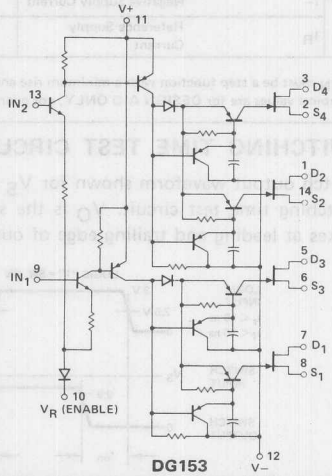
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR LOGIC "1" INPUT

SCHEMATIC DIAGRAMS



DG151



DG153

ABSOLUTE MAXIMUM RATINGS

V+ to V− or V_D	36 V	Current (Any Terminal)	30 mA
V_D to V−	32 V	Storage Temperature	−65 to 150°C
V_D to V_S	±22 V	Operating Temperature (A Suffix)	−55 to 125°C
V+ to V_R	25 V	(B Suffix)	−20 to 85°C
V+ to V_{IN1} or V_{IN2}	25 V	Power Dissipation*	
V_R to V−	25 V	Flat Package**	750 mW
V_{IN1} to V_{IN2}	±6 V	14 Pin DIP***	825 mW
V_{IN1} or V_{IN2} to V_R	±6 V		
V_{IN1} or V_{IN2} to V−	30 V		

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

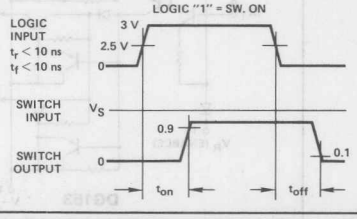
		CHARACTERISTIC		MAX LIMITS DG151A, DG153A −55°C	25°C	125°C	DG151B, DG153B −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	15	15	30				Ω	V_D = 7.5 V	I_S = −10 mA, V_{IN} = 2.5 V*
2							20	20	35		V_D = 5.5 V	
3		$I_{S(off)}$	Source OFF Leakage Current		10	1000				nA	V_S = 7.5 V, V_D = −7.5 V	V_{IN} = 0.8 V*
4								15	300		V_S = 5.5 V, V_D = −5.5 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		10	1000					V_D = 7.5 V, V_S = −7.5 V	
6								15	300		V_D = 5.5 V, V_S = −5.5 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −7.5 V	V_{IN} = 2.5 V*
8								−5	−100		V_D = V_S = −5.5 V	
9	IN	I_{INL}	Input Current, Input Voltage Low	0.1	0.1	2	4	4	4	μA	V_{IN} = 0.8 V*	
10		I_{INH}	Input Current, Input Voltage High	120	60	60	150	100	100		V_{IN} = 2.5 V*	
11	DYNAMIC	t_{on}	Turn-ON Time		1			1.5		μs	See Switching Time Test Circuit	
12		t_{off}	Turn-OFF Time		2.5			2.5				
13		$C_{S(off)}$	Source OFF Capacitance		** 3 Typ			** 3 Typ		pF	V_S = 0, I_D = 0	f = 1 MHz
14		$C_{D(off)}$	Drain OFF Capacitance		** 3 Typ			** 3 Typ			V_D = 0, I_S = 0	
15		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		** 2.8 Typ			** 2.8 Typ			V_D = V_S = 0	
16		Off Isolation		Typ > 50 dB at 1 MHz**							R_L = 100 Ω, C_L = 3 pF	
17	SUPPLY	I+	Positive Supply Current		3			3.3		mA	V_{IN} = 2.5 V*, One Channel ON	
18		I−	Negative Supply Current		−1.8			−2				
19		I_R	Reference Supply Current		−1.4			−1.5				
20		I+	Positive Supply Current		25			25		μA	V_{IN} = 0*, All Channels OFF	
21		I−	Negative Supply Current		−25			−25				
22		I_R	Reference Supply Current		−25			−25				

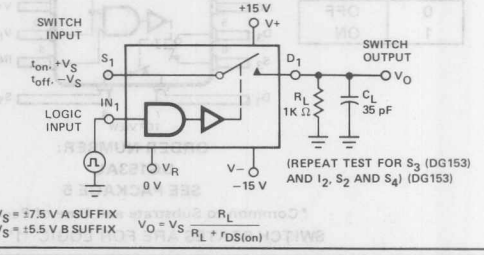
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODC + NIP

SWITCHING TIME TEST CIRCUIT

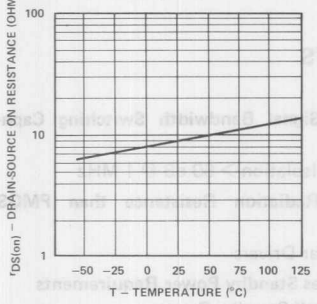
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



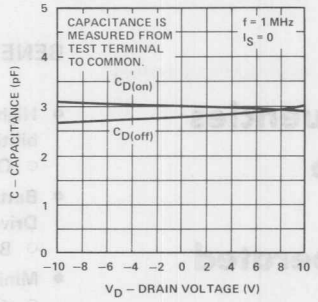


TYPICAL CHARACTERISTICS

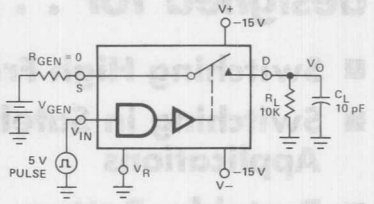
$r_{DS(on)}$ vs Temperature



Capacitance vs V_D

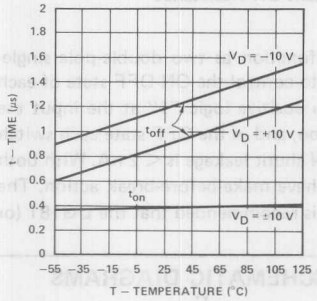


Typical delay, rise, fall, settling times, and switching transients in this circuit.

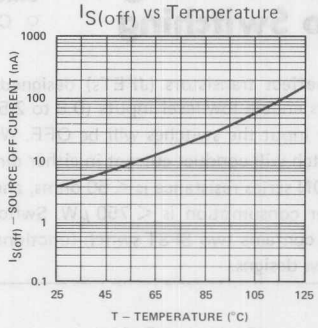


If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

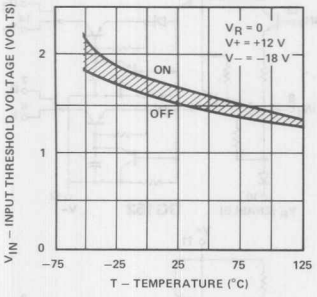
Switching Time vs V_D and Temperature



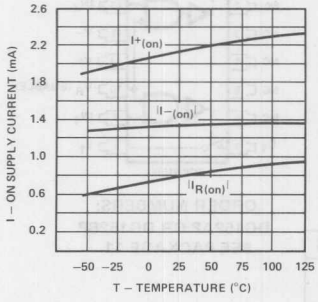
$I_{S(off)}$ vs Temperature



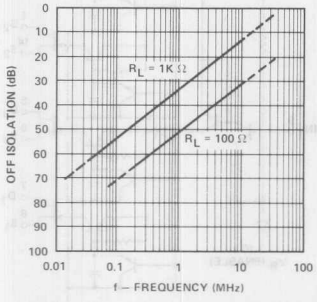
V_{IN} vs Temperature

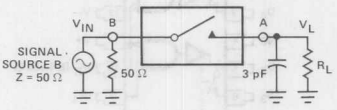


Supply Current vs Temperature



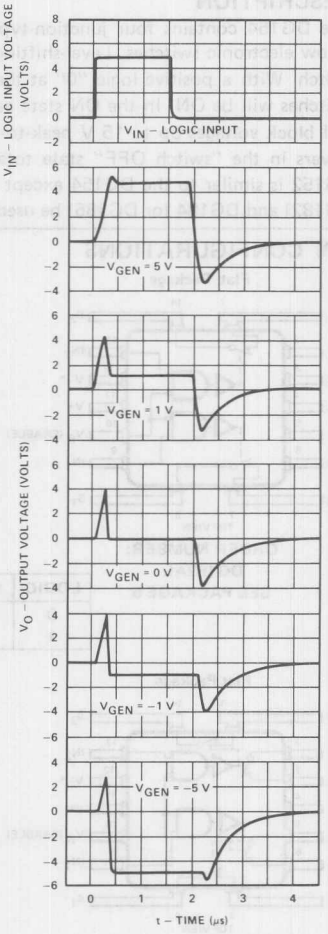
"OFF" Isolation vs R_L and Frequency





"OFF" ISOLATION ≙ 20 LOG $\frac{|V_{IN}|}{|V_L|}$

A - DRAIN OF "OFF" SWITCH
B - SOURCE OF "OFF" SWITCH



designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

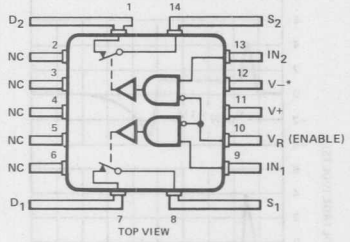
- **Higher Signal Bandwidth Switching Capabilities**
 - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
 - Bipolar Drivers
- **Minimizes Standby Power Requirements**
 - < 1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
 - Constant ON Resistance

DESCRIPTION

The DG154 contains four junction-type field-effect transistors (JFETs) designed to function as two double-pole single-throw electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2.5 V) to control the ON-OFF state of each switch. With a positive logic "0" at the driver input the switches will be OFF. With a positive logic "1" at the input the switches will be ON. In the ON state each switch will conduct current in either direction, and in the OFF state each switch will block voltages up to 15 V peak-to-peak. ON series resistance is < 50 ohms, and ON shunt leakage is < 2 nA. With both drivers in the "switch OFF" state total power consumption is < 750 μW. Switches have make-before-break action. The DG152 is similar to the DG154 except that it contains two SPST switch functions. It is recommended that the DG181 (or DG182) and DG184 (or DG185) be used for new designs.

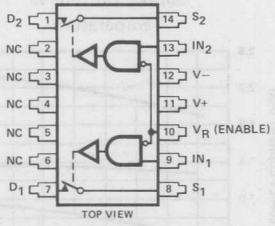
PIN CONFIGURATIONS

Flat Package



ORDER NUMBER:
DG152AL
SEE PACKAGE 5

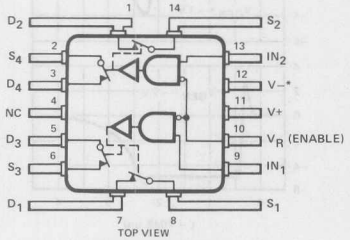
Dual-In-Line Package



ORDER NUMBERS:
DG152AP OR DG152BP
SEE PACKAGE 11

LOGIC	SWITCH
0	OFF
1	ON

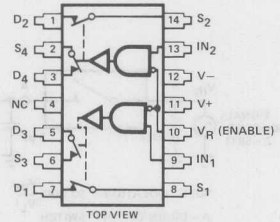
Flat Package



ORDER NUMBER:
DG154AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

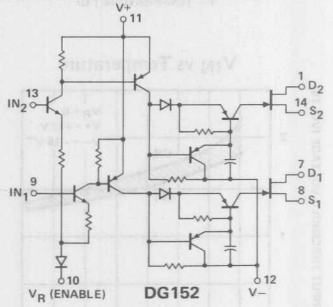
Dual-In-Line Package



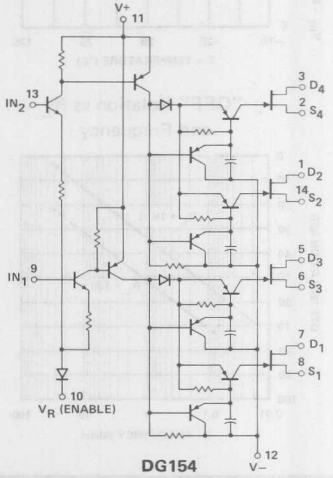
ORDER NUMBERS:
DG154AP OR DG154BP
SEE PACKAGE 11

SWITCH STATES ARE FOR LOGIC "1" INPUT

SCHEMATIC DIAGRAMS



DG152



DG154

ABSOLUTE MAXIMUM RATINGS

V+ to V− or V_D	36 V
V_D to V−	36 V
V_D to V_S	±22 V
V+ to V_R	25 V
V+ to V_{IN1} or V_{IN2}	25 V
V_R to V−	25 V
V_{IN1} to V_{IN2}	±6 V
V_{IN1} or V_{IN2} to V_R	±6 V
V_{IN1} or V_{IN2} to V−	30 V

Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

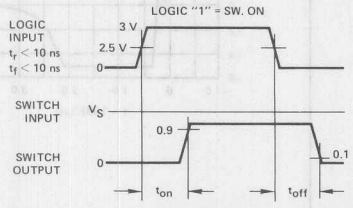
		CHARACTERISTIC		MAX LIMITS DG152A, DG154A −55°C	25°C	125°C	MAX LIMITS DG152B, DG154B −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	50	50	100				Ω	V_D = 7.5 V	I_S = −10 mA, V_{IN} = 2.5 V*
2							100	100	150		V_D = 5.5 V	
3		$I_{S(off)}$	Source OFF Leakage Current		1	100				nA	V_S = 7.5 V, V_D = −7.5 V	V_{IN} = 0.8 V*
4								5	100		V_S = 5.5 V, V_D = −5.5 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		1	100					V_D = 7.5 V, V_S = −7.5 V	
6								5	100		V_D = 5.5 V, V_S = −5.5 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −7.5 V	V_{IN} = 2.5 V*
8								−5	−100		V_D = V_S = −5.5 V	
9	IN	I_{INL}	Input Current, Input Voltage Low	0.1	0.1	2	4	4	4	μA	V_{IN} = 0.8 V*	
10		I_{INH}	Input Current, Input Voltage High	120	60	60	150	100	100		V_{IN} = 2.5 V*	
11	DYNAMIC	t_{on}	Turn-ON Time		0.6			1		μs	See Switching Time Test Circuit	
12		t_{off}	Turn-OFF Time		1.6			2				
13		$C_{S(off)}$	Source OFF Capacitance		**2.4 Typ			**2.4 Typ		pF	V_S = 0, I_D = 0	f = 1 MHz
14		$C_{D(off)}$	Drain OFF Capacitance		**2.4 Typ			**2.4 Typ			V_D = 0, I_S = 0	
15		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		**2.8 Typ			**2.8 Typ			V_D = V_S = 0	
16		Off Isolation		Typ > 60 dB at 1 MHz**							R_L = 75 Ω	
17	SUPPLY	I+	Positive Supply Current		3			3.3		mA	V_{IN} = 2.5 V*, One Channel ON	
18		I−	Negative Supply Current		−1.8			−2				
19		I_R	Reference Supply Current		−1.4			−1.5				
20		I+	Positive Supply Current		25			25		μA	V_{IN} = 0*, All Channels OFF	
21		I−	Negative Supply Current		−25			−25				
22		I_R	Reference Supply Current		−25			−25				

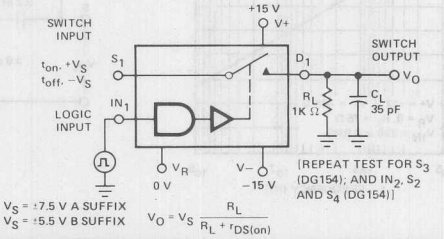
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODC + NC

SWITCHING TIME TEST CIRCUIT

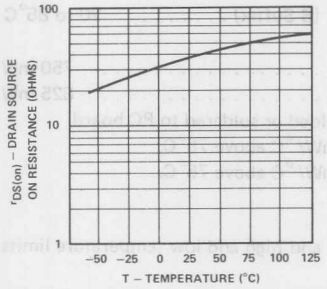
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



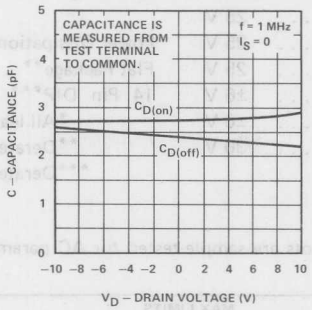


TYPICAL CHARACTERISTICS

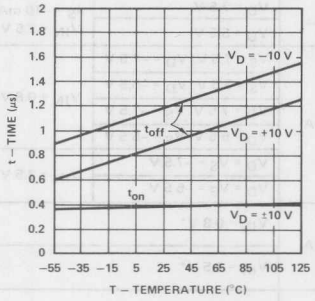
$r_{DS(on)}$ vs Temperature



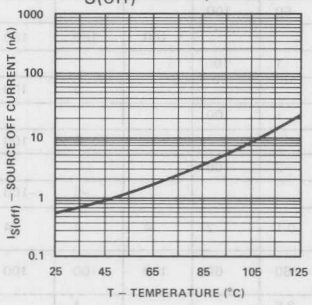
Capacitance vs V_D



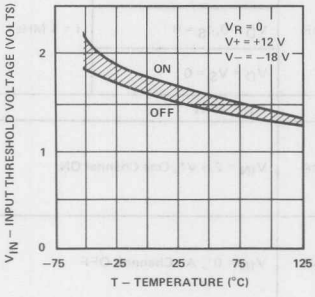
Switching Time vs V_D and Temperature



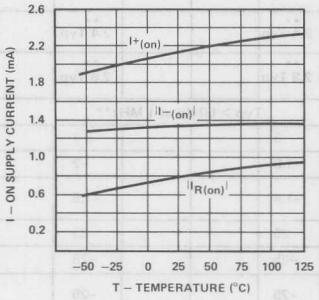
$I_{S(off)}$ vs Temperature



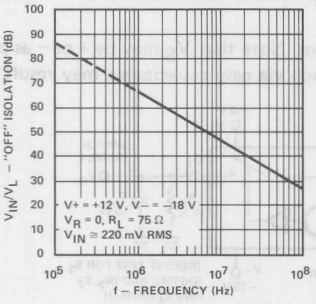
V_{IN} vs Temperature



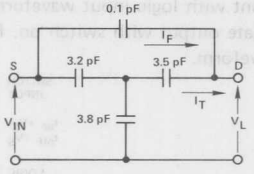
Supply Current vs Temperature



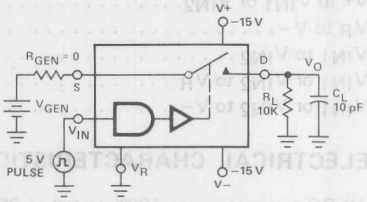
"OFF" Isolation vs R_L and Frequency



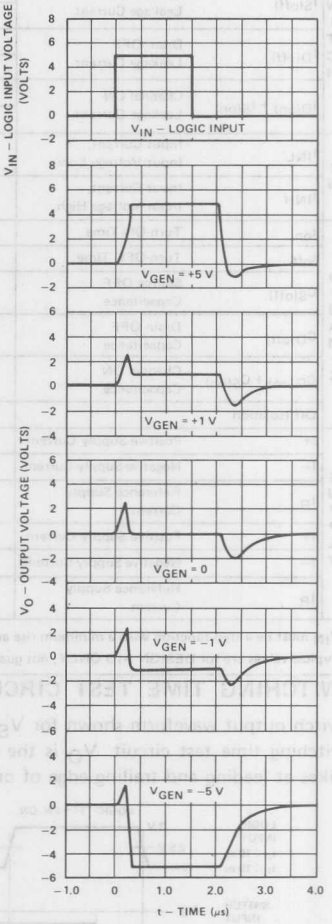
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



Drivers with Differentially Driven Normally Open and Normally Closed FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

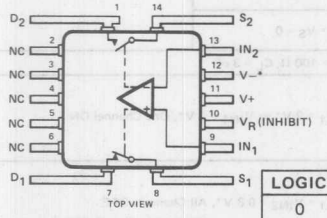
- **Higher Signal Bandwidth Switching Capabilities**
 - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
 - Bipolar Drivers
- **Minimizes Standby Power Requirements**
 - < 1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
 - Constant ON Resistance

DESCRIPTION

The DG163 contains four junction-type field-effect transistors designed to function as electronic switches. Level-shifting drivers enable low-level inputs (2 to 3 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN_2 connected to a 2.5 voltage reference, a positive logic "0" at input IN_1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN_1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally-grounded V_R terminal may be used as an "Inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to V_R. In the ON state, each switch conducts equally well in either direction, has a series resistance of < 15 ohms, and a shunt leakage of < 2 nA. In the OFF state the switches will hold off voltages up to 15 V peak-to-peak. Switches have make-before-break action. The DG161 is similar to the DG163, except that it contains two FET switches instead of four. It is recommended that the DG186 and DG189 be used for new designs.

PIN CONFIGURATIONS

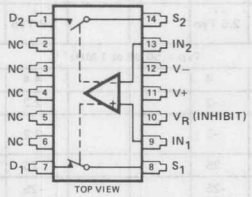
Flat Package



ORDER NUMBERS:
DG161AL
SEE PACKAGE 5

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

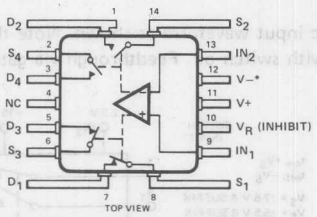
Dual-In-Line Package



ORDER NUMBERS:
DG161AP OR DG161BP
SEE PACKAGE 11

Flat Package

LOGIC	SW 1 SW 3	SW 2 SW 4
0	OFF	ON
1	ON	OFF

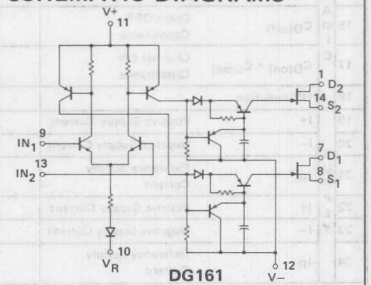


ORDER NUMBER: DG163AL
SEE PACKAGE 5

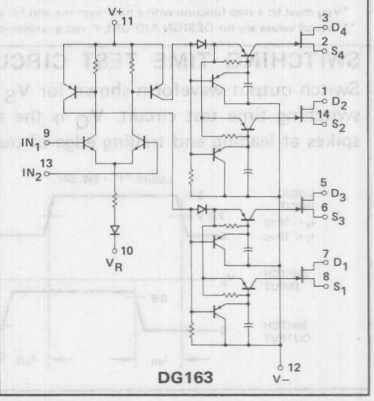
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR V_{IN1} = LOGIC "1" INPUT AND V_{IN2} = 2.5 V BIAS (POSITIVE LOGIC)

SCHEMATIC DIAGRAMS



DG161



DG163

V+ to V_R	25 V
V+ to V_{IN1} or V_{IN2}	25 V
V_R to V−	25 V
V_{IN1} to V_{IN2}	±6 V
V_{IN1} or V_{IN2} to V_R	±6 V
V_{IN1} or V_{IN2} to V−	30 V

Power Dissipation*

Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

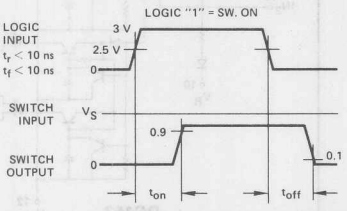
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX −20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, V_R = 0, V_{IN2} = 2.5 V*	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	15	15	30				Ω	V_D = 7.5 V	I_S = −10 mA, V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
2							20	20	35		V_D = 5.5 V	
3		$I_{S(off)}$	Source OFF Leakage Current		10	1000				nA	V_S = 7.5 V, V_D = −7.5 V	V_{IN1} = 2 V* ($SW_{1,3}$ OFF), V_{IN1} = 3 V* ($SW_{2,4}$ OFF)
4								15	300		V_S = 5.5 V, V_D = −5.5 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		10	1000					V_D = 7.5 V, V_S = −7.5 V	
6								15	300		V_D = 5.5 V, V_S = −5.5 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −7.5 V	V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
8								−5	−100		V_D = V_S = −5.5 V	
9	IN	I_{IN1L}	Input 1 Current, Input 1 Voltage Low	0.1	0.1	2	4	4	4	μA	V_{IN1} = 2 V*	
10		I_{IN2L}	Input 2 Current, Input 2 Voltage Low	0.1	0.1	2	4	4	4		V_{IN2} = 2 V*, V_{IN1} = 2.5 V*	
11		I_{IN1H}	Input 1 Current, Input 1 Voltage High	120	60	60	150	100	100		V_{IN1} = 3 V*	
12		I_{IN2H}	Input 2 Current, Input 2 Voltage High	120	60	60	150	100	100		V_{IN2} = 3 V*, V_{IN1} = 2.5 V*	
13	DYNAMIC	t_{on}	Turn-ON Time		1			1.5		μs	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time		2.5			2.5				
15		$C_{S(off)}$	Source OFF Capacitance		** 3 Typ			** 3 Typ		pF	V_S = 0, I_D = 0	f = 1 MHz
16		$C_{D(off)}$	Drain OFF Capacitance		** 3 Typ			** 3 Typ			V_D = 0, I_S = 0	
17		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		** 2.8 Typ			** 2.8 Typ			V_D = V_S = 0	
18		Off Isolation		Typ > 50 dB at 1 MHz**							R_L = 100 Ω, C_L = 3 pF	
19	SUPPLY	I+	Positive Supply Current		4			4.4		mA	V_{IN1} = 2 V* or V_{IN1} = 3 V*, One Channel ON	
20		I−	Negative Supply Current		−2			−2.2				
21		I_R	Reference Supply Current		−2			−2.2				
22		I+	Positive Supply Current		25			25		μA	V_{IN1} = V_{IN2} = 0.8 V*, All Channels OFF	
23		I−	Negative Supply Current		−25			−25				
24		I_R	Reference Supply Current		−25			−25				

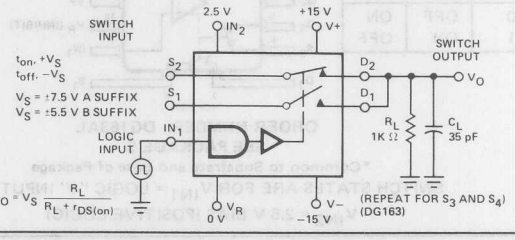
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODF + NIP

SWITCHING TIME TEST CIRCUIT

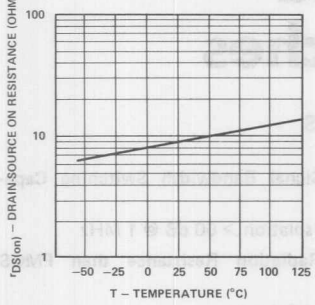
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



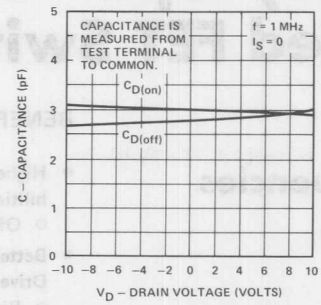


TYPICAL CHARACTERISTICS

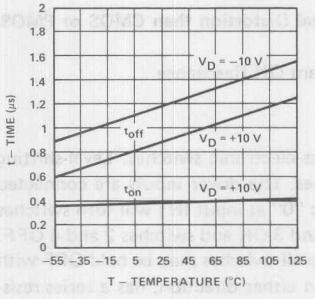
$r_{DS(on)}$ vs Temperature



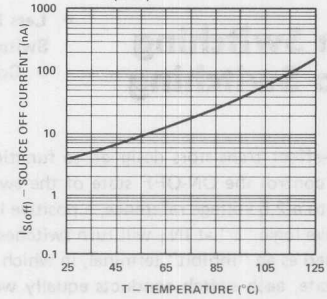
Capacitance vs V_D



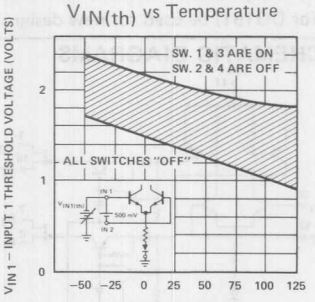
Switching Time vs V_D and Temperature



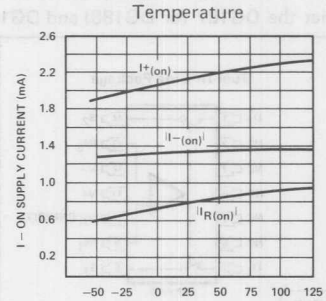
$I_{S(off)}$ vs Temperature



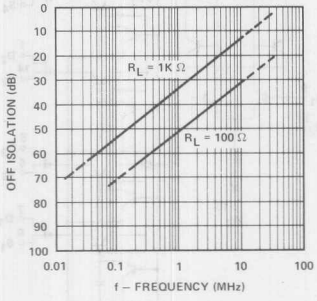
$V_{IN(th)}$ vs Temperature

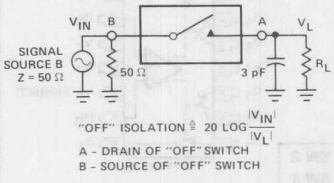


Supply Current vs Temperature

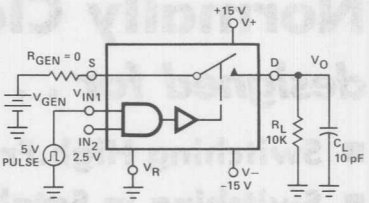


"OFF" Isolation vs R_L and Frequency

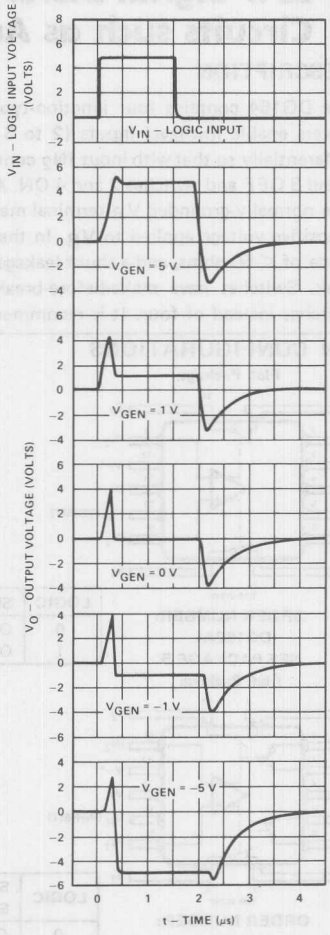




Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



Drivers with Differentially Driven Normally Open and Normally Closed FET Switches

Siliconix

designed for . . .

- **Switching High.Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

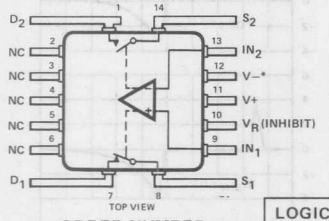
- **Higher Signal Bandwidth Switching Capabilities**
 - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
 - Bipolar Drivers
- **Minimizes Standby Power Requirements**
 - < 1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
 - Constant ON Resistance

DESCRIPTION

The DG164 contains four junction-type field-effect transistors designed to function as electronic switches. Level-shifting drivers enable low-level inputs (2 to 3 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN_2 connected to a 2.5 voltage reference, a positive logic "0" at input IN_1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN_1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally-grounded V_R terminal may be used as an "Inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to V_R. In the ON state, each switch conducts equally well in either direction, has a series resistance of < 50 ohms, and a shunt leakage of < 2 nA. In the OFF state the switches will hold off voltages up to 15 V peak-to-peak. Switches have make-before-break action. The DG162 is similar to the DG164, except that it contains two FET switches instead of four. It is recommended that the DG187 (or DG188) and DG190 (or DG191) be used for new designs.

PIN CONFIGURATIONS

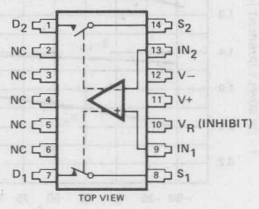
Flat Package



ORDER NUMBER:
DG162AL
SEE PACKAGE 5

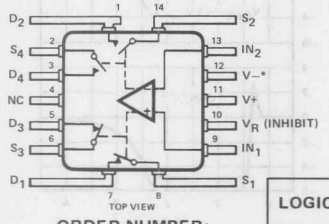
LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

Dual-In-Line Package



ORDER NUMBERS:
DG162AP OR DG162BP
SEE PACKAGE 11

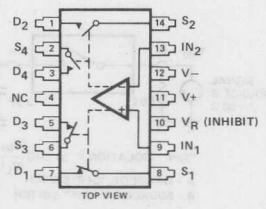
Flat Package



ORDER NUMBER:
DG164AL
SEE PACKAGE 5

LOGIC	SW 1 SW 3	SW 2 SW 4
0	OFF	ON
1	ON	OFF

Dual-In-Line Package

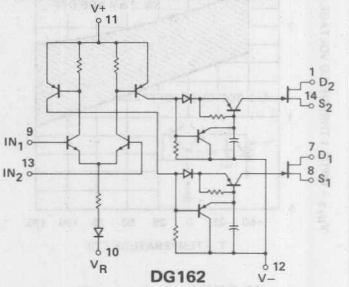


ORDER NUMBERS:
DG164AP OR DG164BP
SEE PACKAGE 11

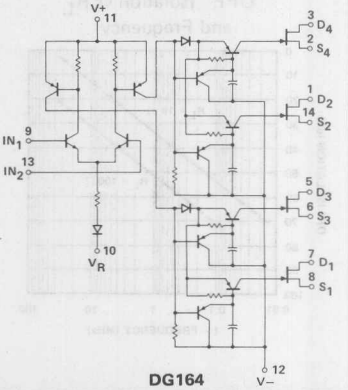
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR V_{IN1} = LOGIC "1" INPUT AND
V_{IN2} = 2.5 V BIAS (POSITIVE LOGIC)

SCHEMATIC DIAGRAMS



DG162



DG164

ABSOLUTE MAXIMUM RATINGS

$V+$ to $V-$	36 V	Current (Any Terminal)	30 mA
$V+$ to V_D or V_S	36 V	Storage Temperature	−65 to 150°C
V_D or V_S to $V-$	36 V	Operating Temperature (A Suffix)	−55 to 125°C
V_D to V_S	±22 V	(B Suffix)	−20 to 85°C
$V+$ to V_R	25 V	Power Dissipation*	
$V+$ to V_{IN1} or V_{IN2}	25 V	Flat Package**	750 mW
V_R to $V-$	25 V	14 Pin DIP***	825 mW
V_{IN1} to V_{IN2}	±6 V		
V_{IN1} or V_{IN2} to V_R	±6 V		
V_{IN1} or V_{IN2} to $V-$	30 V		

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

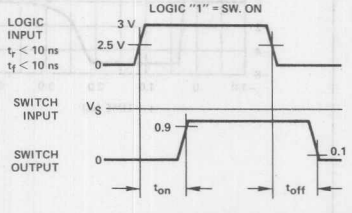
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX −20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: $V+ = 15$ V, $V- = -15$ V, $V_R = 0$, $V_{IN2} = 2.5$ V*	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	50	50	100				Ω	$V_D = 7.5$ V	$I_S = -10$ mA, $V_{IN1} = 3$ V* ($SW_{1,3}$ ON), $V_{IN1} = 2$ V* ($SW_{2,4}$ ON)
2	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance				100	100	150	Ω	$V_D = 5.5$ V	$I_S = -10$ mA, $V_{IN1} = 3$ V* ($SW_{1,3}$ ON), $V_{IN1} = 2$ V* ($SW_{2,4}$ ON)
3	SWITCH	$I_{S(off)}$	Source OFF Leakage Current		2	100				nA	$V_S = 7.5$ V, $V_D = -7.5$ V	$V_{IN1} = 2$ V* ($SW_{1,3}$ OFF), $V_{IN1} = 3$ V* ($SW_{2,4}$ OFF)
4	SWITCH	$I_{S(off)}$	Source OFF Leakage Current					5	100	nA	$V_S = 5.5$ V, $V_D = -5.5$ V	$V_{IN1} = 2$ V* ($SW_{1,3}$ OFF), $V_{IN1} = 3$ V* ($SW_{2,4}$ OFF)
5	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current		2	100				nA	$V_D = 7.5$ V, $V_S = -7.5$ V	$V_{IN1} = 2$ V* ($SW_{1,3}$ OFF), $V_{IN1} = 3$ V* ($SW_{2,4}$ OFF)
6	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current					5	100	nA	$V_D = 5.5$ V, $V_S = -5.5$ V	$V_{IN1} = 2$ V* ($SW_{1,3}$ OFF), $V_{IN1} = 3$ V* ($SW_{2,4}$ OFF)
7	SWITCH	$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	100				nA	$V_D = V_S = -7.5$ V	$V_{IN1} = 3$ V* ($SW_{1,3}$ ON), $V_{IN1} = 2$ V* ($SW_{2,4}$ ON)
8	SWITCH	$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current					−5	100	nA	$V_D = V_S = -5.5$ V	$V_{IN1} = 3$ V* ($SW_{1,3}$ ON), $V_{IN1} = 2$ V* ($SW_{2,4}$ ON)
9	IN	I_{IN1L}	Input 1 Current, Input 1 Voltage Low	0.1	0.1	2	4	4	4	µA	$V_{IN1} = 2$ V*	
10	IN	I_{IN2L}	Input 2 Current, Input 2 Voltage Low	0.1	0.1	2	4	4	4	µA	$V_{IN2} = 2$ V*, $V_{IN1} = 2.5$ V*	
11	IN	I_{IN1H}	Input 1 Current, Input 1 Voltage High	120	60	60	150	100	100	µA	$V_{IN1} = 3$ V*	
12	IN	I_{IN2H}	Input 2 Current, Input 2 Voltage High	120	60	60	150	100	100	µA	$V_{IN2} = 3$ V*, $V_{IN1} = 2.5$ V*	
13	DYNAMIC	t_{on}	Turn-ON Time		0.8			1		µs	See Switching Time Test Circuit	
14	DYNAMIC	t_{off}	Turn-OFF Time		1.6			2		µs	See Switching Time Test Circuit	
15	DYNAMIC	$C_{S(off)}$	Source OFF Capacitance		** 2.4 Typ			** 2.4 Typ		pF	$V_S = 0$, $I_D = 0$	f = 1 MHz
16	DYNAMIC	$C_{D(off)}$	Drain OFF Capacitance		** 2.4 Typ			** 2.4 Typ		pF	$V_D = 0$, $I_S = 0$	f = 1 MHz
17	DYNAMIC	$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		** 2.8 Typ			** 2.8 Typ		pF	$V_D = V_S = 0$	f = 1 MHz
18		Off Isolation		Typ > 60 dB at 1 MHz**							$R_L = 75$ Ω	
19	SUPPLY	I+	Positive Supply Current		4			4.4		mA	$V_{IN1} = 2$ V* or $V_{IN1} = 3$ V*, One Channel ON	
20	SUPPLY	I−	Negative Supply Current		−2			−2.2		mA	$V_{IN1} = 2$ V* or $V_{IN1} = 3$ V*, One Channel ON	
21	SUPPLY	I_R	Reference Supply Current		−2			−2.2		mA	$V_{IN1} = 2$ V* or $V_{IN1} = 3$ V*, One Channel ON	
22	SUPPLY	I+	Positive Supply Current		25			25		µA	$V_{IN1} = V_{IN2} = 0.8$ V*, All Channels OFF	
23	SUPPLY	I−	Negative Supply Current		−25			−25		µA	$V_{IN1} = V_{IN2} = 0.8$ V*, All Channels OFF	
24	SUPPLY	I_R	Reference Supply Current		−25			−25		µA	$V_{IN1} = V_{IN2} = 0.8$ V*, All Channels OFF	

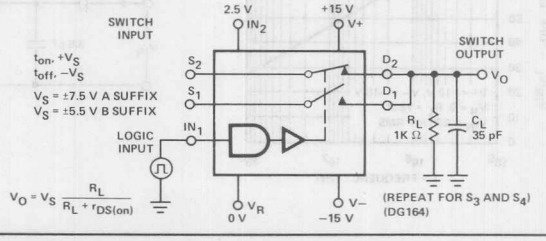
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/µs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

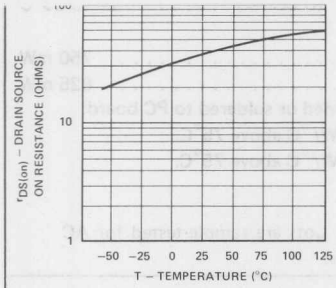
LODF + NC

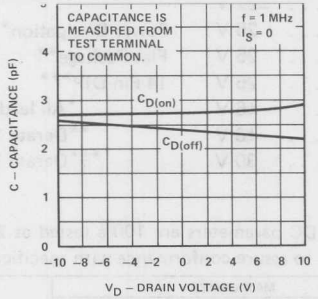
SWITCHING TIME TEST CIRCUIT

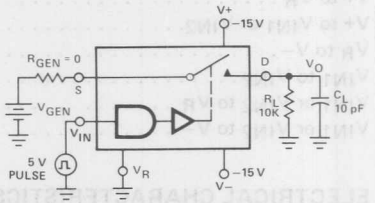
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





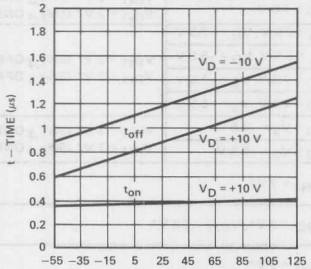




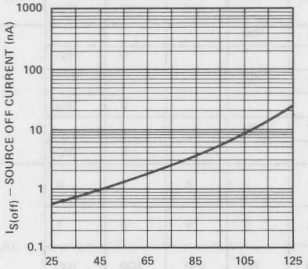


If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

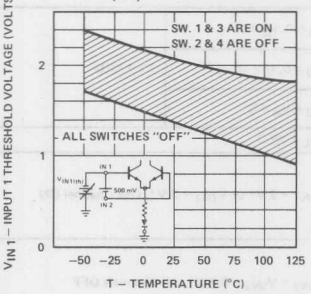
Switching Time vs V_D and Temperature



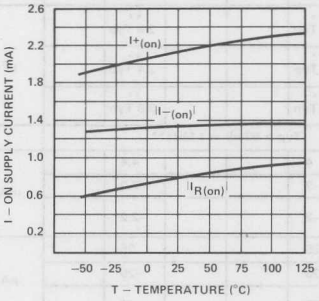
$I_{S(off)}$ vs Temperature



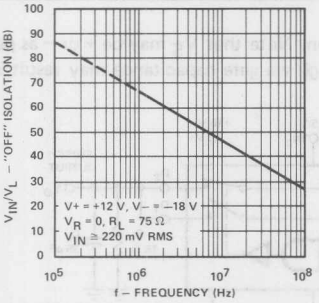
$V_{IN(th)}$ vs Temperature



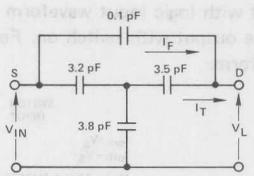
Supply Current vs Temperature

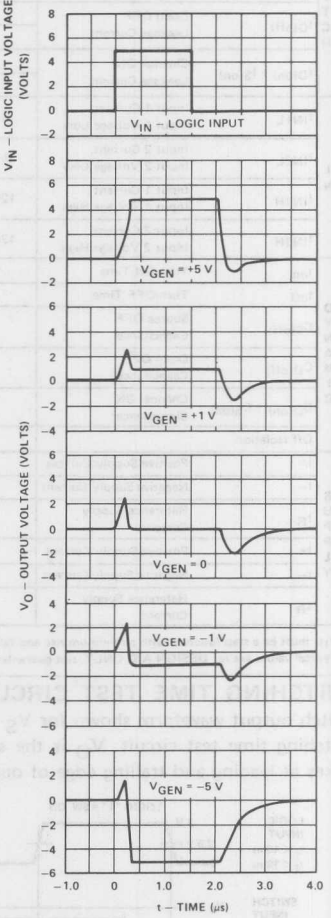


"OFF" Isolation vs R_L and Frequency



Equivalent "OFF" Circuit





Monolithic 4-Channel Driver with PMOS Switches

Siliconix

designed for . . .

- **Make-Before-Break Switching i.e. Feedback Resistor Switching in Variable Gain Op-Amps**
- **Low Leakage Switching such as Sample and Hold Circuits**

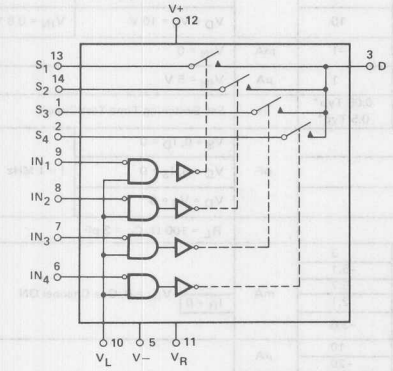
BENEFITS

- **Easily Interfaced**
 - TTL, CMOS, DTL Direct Drive Compatibility
- **Reduces External Component Requirements**
 - No Interface Components Required
 - Voltage–Limiting Diodes Protect PMOS Gates

DESCRIPTION

The DG172 contains four MOS field-effect transistors designed to function as electronic switches. Level-shifting drivers enable a low-level input (0.8 to 2.0 V) to control the ON-OFF condition of each switch. In the ON state, each switch will conduct current equally well in either direction. In the OFF state, the switches will block voltages up to 20 V peak-to-peak. Positive logic "0" at the driver input will turn each switch ON. A common driver terminal V_L may be used to clock all four switches by switching the device from the ENABLE mode ($\geq$ 4 V) to the INHIBIT mode ($\leq$ 0.4 V).

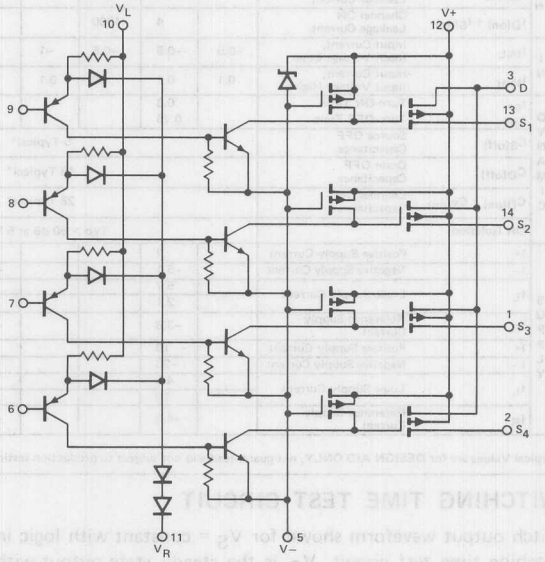
FUNCTIONAL DIAGRAM



LOGIC	SWITCH
0	ON
1	OFF

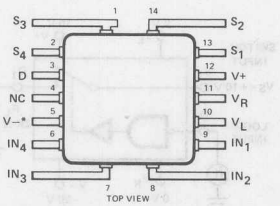
SWITCH STATES ARE FOR LOGIC "1" INPUT.
(POSITIVE LOGIC)

SCHEMATIC DIAGRAM



PIN CONFIGURATIONS

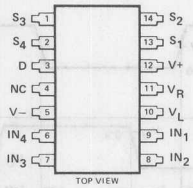
Flat Package



ORDER NUMBER: DG172AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

Dual-In-Line Package



ORDER NUMBERS: DG172AP OR DG172BP
SEE PACKAGE 11

DG172CJ
SEE PACKAGE 7

ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_D	25 V
V+ to V_S	25 V
V_S to V−	36 V
V_D to V−	36 V
V_S to V_D	25 V
V_L to V−	30 V
V_L to V_{IN}	±6 V
V_L to V_R	±6 V
V_{IN} to V_R	±6 V
Current (Any Terminal)	20 mA
Storage Temperature (A & B Suffix)	−65 to 150°C
(C Suffix)	-65 to 125°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
(C Suffix)	0 to 70°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP (ceramic)***	825 mW
14 Pin Plastic DIP****	470 mW

*All leads welded or soldered to PC board
**Derate 10 mW/°C above 75°C
***Derate 11 mW/°C above 75°C
****Derate 6.3 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

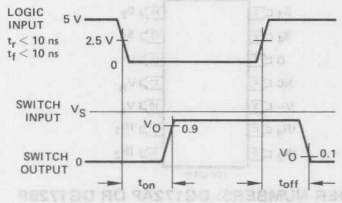
		CHARACTERISTIC		MAX LIMITS DG172A −55°C	DG172A 25°C	DG172A 125°C	DG172B −20°C	DG172B 25°C	DG172B 85°C	DG172C 25°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 10 V, V− = −20 V, V_L = 5 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	150	150	250	150	150	200	200	Ω	V_D = 10 V	I_S = −1 mA, V_{IN} = 0.8 V
2				200	200	350	225	225	300	300		V_D = 0	
3				450	450	600	500	500	600	600		V_D = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current		−1	−1000		−5	−100	−10	nA	V_S = −10 V, V_D = 10 V	V_{IN} = 2 V
5		$I_{D(off)}$	Drain OFF Leakage Current		−4	−4000		−10	−300	−10		V_D = −10 V, V_S = 10 V	
6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		4	4000		10	300	10		$V_D = V_S$ = 10 V	V_{IN} = 0.8 V
7	IN	I_{INL}	Input Current, Input Voltage Low	−0.5	−0.5	−0.5	−1	−1	−1	−1	mA	V_{IN} = 0	
8		I_{INH}	Input Current, Input Voltage High	0.1	0.1	10	0.1	1	10	1	μA	V_{IN} = 5 V	
9	DYNAMIC	t_{on}	Turn-ON Time		0.3			0.5		0.08 Typ*	μs	See Switching Time Test Circuit	
10		t_{off}	Turn-OFF Time		0.75			1		0.5 Typ*			
11		$C_{S(off)}$	Source OFF Capacitance	5 Typical*							pF	V_S = 0, I_D = 0	f = 1 MHz
12		$C_{D(off)}$	Drain OFF Capacitance	18 Typical*								V_D = 0, I_S = 0	
13		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	28 Typical*								$V_D = V_S$ = 0	
14		Off Isolation		Typ > 50 dB at 5 MHz*								R_L = 100 Ω, C_L = 3 pF	
15	SUPPLY	I+	Positive Supply Current		3			3		3	mA	V_{IN} = 0, One Channel ON	
16		I−	Negative Supply Current		−5.1			−5.1		−5.1			
17		I_L	Logic Supply Current		5.7			5.7		5.7			
18					2.1			2.1		2.1		I_R = 0	
19		I_R	Reference Supply Current		−3.6			−3.6		−3.6			
20		I+	Positive Supply Current		10			10		10	μA	V_{IN} = 5 V, All Channels OFF	
21		I−	Negative Supply Current		−20			−20		−20			
22		I_L	Logic Supply Current		4.5			4.5		4.5	mA		
23					10			10		10	μA	I_R = 0	
24		I_R	Reference Supply Current		−4.5			−4.5		−4.5	mA		

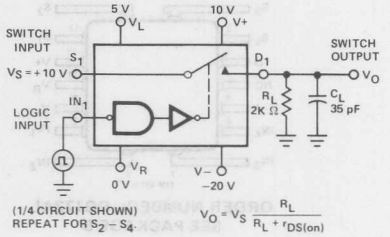
*Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing

CMD

SWITCHING TIME TEST CIRCUIT

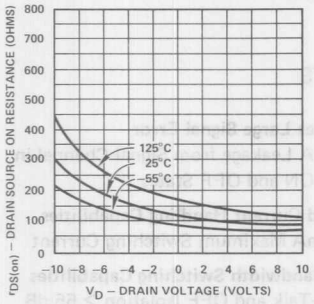
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



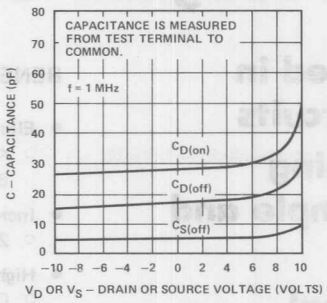


TYPICAL CHARACTERISTICS

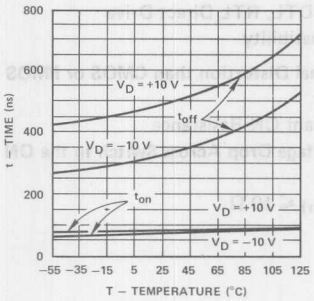
$r_{DS(on)}$ vs V_D and Temperature



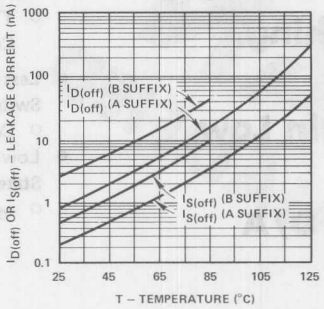
Capacitance vs V_D or V_S



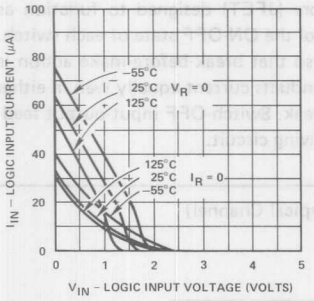
Switching Time vs V_D and Temperature



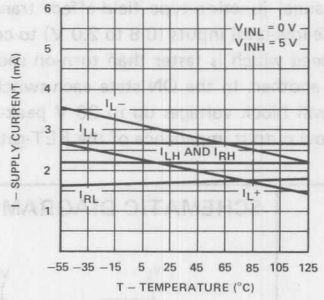
$I_{D(off)}/I_{S(off)}$ vs Temperature



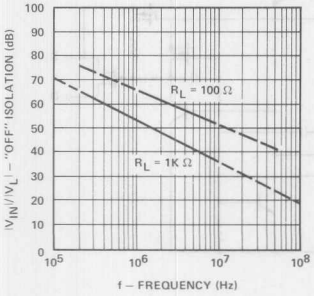
I_{IN} vs V_{IN} and Temperature

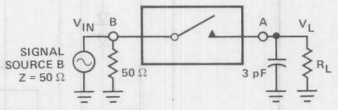


Supply Current vs Temperature



"OFF" Isolation vs R_L and Frequency

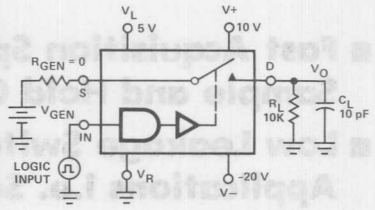




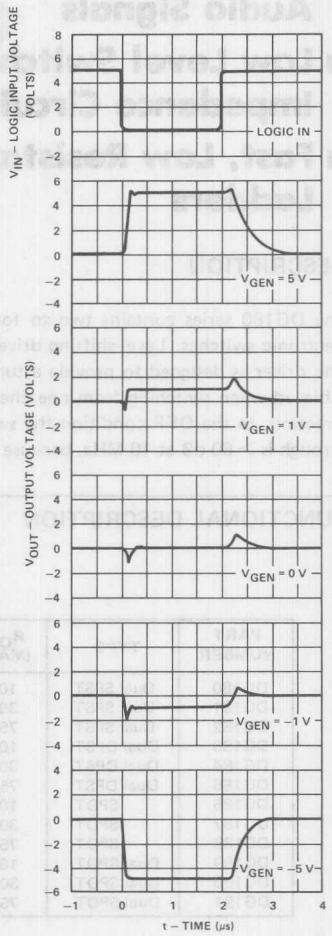
"OFF" ISOLATION ≙ 20 LOG $\frac{|V_{IN}|}{|V_L|}$

A - DRAIN OF "OFF" SWITCH
B - SOURCE OF "OFF" SWITCH

Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



High-Speed Driver with JFET Switches *designed for...*

Siliconix

- **Fast Acquisition Speed in Sample and Hold Circuits**
- **Low Leakage Switching Applications i.e. Sample and Hold Circuits**
- **High Frequency Signal Switching such as Video Signals**
- **Low Distortion Switching, Audio Signals**
- **Low Level Switching in Low Impedance Circuits**
- **Fast, Low Resistance D/A Ladders**

BENEFITS

- **Eliminates Large Signal Error**
 - < 2 nA Leakage from Signal Channel in Both ON and OFF States
- **Increased Current Handling Capabilities**
 - 200 mA Maximum Switching Current
- **Higher Bandwidth Switching Capabilities**
 - Cross-Talk and OFF Isolation > 55 dB at 1 MHz (75 Ω Load)
- **Easily Interfaced**
 - TTL, DTL, RTL Direct Drive Compatibility
- **Less Signal Distortion than CMOS or PMOS Switches**
 - Constant ON Resistance
- **Low Voltage Drop Across Switch in the ON State**
 - $r_{ds(on)} \leq 10\ \Omega$

JAN QUALIFIED

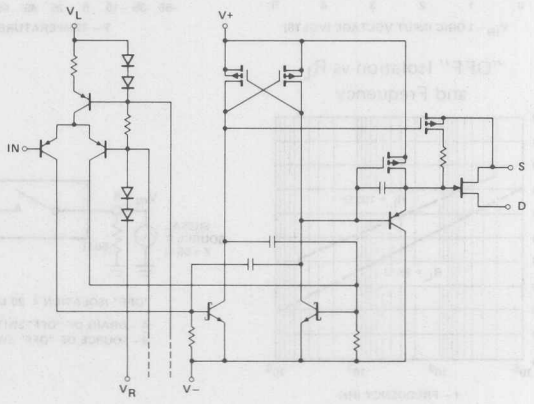
DESCRIPTION

The DG180 series contains two to four N-channel junction-type field-effect transistors (JFET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2.0 V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block voltages up to 20 V peak-to-peak. Switch-OFF input-output feed-through is > 60 dB at 10 MHz, because of the low output impedance of the FET-gate driving circuit.

FUNCTIONAL DESCRIPTION

PART NUMBER	TYPE	R_{ON} (MAX)
DG180	Dual SPST	10
DG181	Dual SPST	30
DG182	Dual SPST	75
DG183	Dual DPST	10
DG184	Dual DPST	30
DG185	Dual DPST	75
DG186	SPDT	10
DG187	SPDT	30
DG188	SPDT	75
DG189	Dual SPDT	10
DG190	Dual SPDT	30
DG191	Dual SPDT	75

SCHEMATIC DIAGRAM (Typical Channel)



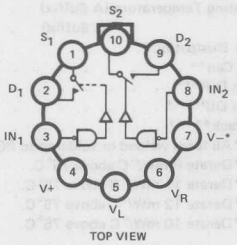
PIN CONFIGURATIONS

DUAL SPST

LOGIC	SWITCH
0	ON
1	OFF

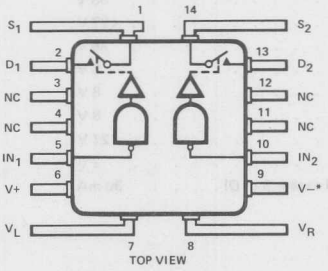
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

Metal Can Package



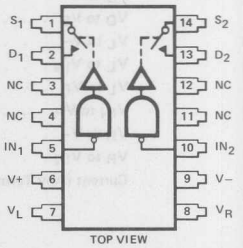
ORDER NUMBERS:
DG180AA OR DG180BA
DG181AA OR DG181BA
DG182AA OR DG182BA
SEE PACKAGE 2
*Common to Substrate and Case

Flat Package



ORDER NUMBER:
DG181AL
SEE PACKAGE 5
*Common to Substrate and Base of Package

Dual-In-Line Package



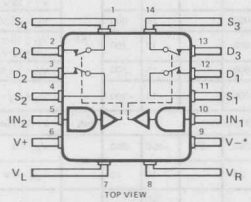
ORDER NUMBERS:
DG180AP OR DG180BP
DG181AP OR DG181BP
DG182AP OR DG182BP
SEE PACKAGE 11

DUAL DPST

LOGIC	SWITCH
0	OFF
1	ON

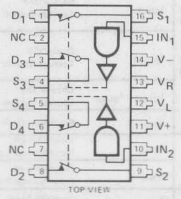
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

Flat Package



ORDER NUMBERS:
DG184AL OR DG185AL
SEE PACKAGE 5
*Common to Substrate and Base of Package

Dual-In-Line Package



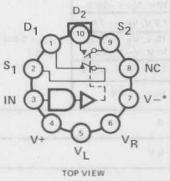
ORDER NUMBERS:
DG183AP OR DG183BP
DG184AP OR DG184BP
DG185AP OR DG185BP
SEE PACKAGE 12

SPDT

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

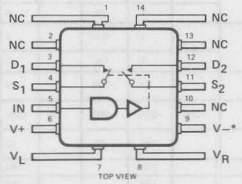
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

Metal Can Package



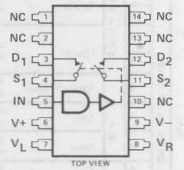
ORDER NUMBERS:
DG186AA OR DG186BA
DG187AA OR DG187BA
DG188AA OR DG188BA
SEE PACKAGE 2
*Common to Substrate and Case

Flat Package



ORDER NUMBERS:
DG187AL OR DG188AL
SEE PACKAGE 5
*Common to Substrate and Base of Package

Dual-In-Line Package



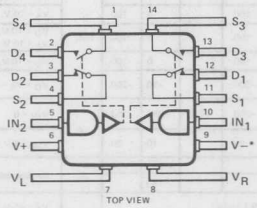
ORDER NUMBERS:
DG186AP OR DG186BP
DG187AP OR DG187BP
DG188AP OR DG188BP
SEE PACKAGE 11

DUAL SPDT

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

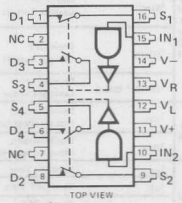
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

Flat Package



ORDER NUMBERS:
DG190AL OR DG191AL
SEE PACKAGE 5
*Common to Substrate and Base of Package

Dual-In-Line Package



ORDER NUMBERS:
DG189AP OR DG189BP
DG190AP OR DG190BP
DG191AP OR DG191BP
SEE PACKAGE 12

ABSOLUTE MAXIMUM RATINGS

V+ to V–	36 V
V+ to V_D	33 V
V_D to V–	33 V
V_D to V_S	±22 V
V_L to V–	36 V
V_L to V_{IN}	8 V
V_L to V_R	8 V
V_{IN} to V_R	8 V
V_R to V–	27 V
V_R to V_{IN}	2 V
Current (Any Terminal except S or D)	30 mA
Currents (S or D) 30 Ω, 75 Ω	30 mA
10 Ω Only	200 mA
Storage Temperature	–65 to 150°C
Operating Temperature (A Suffix)	–55 to 125°C
(B Suffix)	–20 to 85°C

Power Dissipation*

Metal Can**	450 mW
14 Pin DIP***	825 mW
16 Pin DIP****	900 mW
Flat Pack*****	900 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.
****Derate 12 mW/°C above 75°C.
*****Derate 10 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

			CHARACTERISTIC		MAX LIMITS A SUFFIX –55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX –20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V– = –15 V, V_L = 5 V, V_R = 0	
10 Ω DG180, DG183, DG186, DG188	1		$r_{DS(on)}$	Drain Source ON Resistance	10	10	20	15	15	25	Ω	V_D = –7.5 V	I_S = –10 mA, V_{IN} = 0.8 V or 2.0 V Note 1
	2	SWITCH	$I_{S(off)}$	Source OFF Leakage Current		10	1000		15	300	nA	V_S = 10 V, V_D = –10 V, V+ = 10 V, V– = –20 V	V_{IN} = 2.0 V or 0.8 V Note 2
	3					10	1000		15	300		V_S = 7.5 V, V_D = –7.5 V	
	4		$I_{D(off)}$	Drain OFF Leakage Current		10	1000		15	300		V_D = 10 V, V_S = –10 V, V+ = 10 V, V– = –20 V	
	5					10	1000		15	300		V_D = 7.5 V, V_S = –7.5 V	
	6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		–2	–200		–10	–200		V_D = V_S = –7.5 V	
	7		I_{DSS}	Saturation Drain Current	300 Typical*						mA	2 msec Pulse Duration	
	8	IN	I_{INL}	Input Current, Input Voltage Low	–250	–250	–250	–250	–250	–250	µA	V_{IN} = 0	
	9		I_{INH}	Input Current, Input Voltage High		10	20		10	20		V_{IN} = 5 V	
	10	DYNAMIC	t_{on}	Turn-ON Time		300			350		ns	See Switching Time Test Circuit	
	11		t_{off}	Turn-OFF Time		250			300				
	12		$C_{S(off)}$	Source OFF Capacitance	21 Typical*						pF	V_S = –5 V, I_D = 0	f = 1 MHz
	13		$C_{D(off)}$	Drain OFF Capacitance	17 Typical*							V_D = 5 V, I_S = 0	
	14		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	17 Typical*							V_D = V_S = 0	
	15			OFF Isolation	Typical > 55 dB at 1 MHz *							R_L = 75 Ω	
30 Ω DG181, DG184, DG187, DG190	1		$r_{DS(on)}$	Drain-Source ON Resistance	30	30	60	50	50	75	Ω	V_D = –7.5 V	I_S = –10 mA, V_{IN} = 0.8 V or 2.0 V Note 1
	2	SWITCH	$I_{S(off)}$	Source OFF Leakage Current		1	100		5	100	nA	V_S = 10 V, V_D = –10 V, V+ = 10 V, V– = –20 V	V_{IN} = 2.0 V or 0.8 V Note 2
	3					1	100		5	100		V_S = 7.5 V, V_D = –7.5 V	
	4		$I_{D(off)}$	Drain OFF Leakage Current		1	100		5	100		V_D = 10 V, V_S = –10 V, V+ = 10 V, V– = –20 V	
	5					1	100		5	100		V_D = 7.5 V, V_S = –7.5 V	
	6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		–2	–200		–10	–200		V_D = V_S = –7.5 V	
	7	IN	I_{INL}	Input Current, Input Voltage Low	–250	–250	–250	–250	–250	–250	µA	V_{IN} = 0	
	8		I_{INH}	Input Current, Input Voltage High		10	20		10	20		V_{IN} = 5 V	
	9	DYNAMIC	t_{on}	Turn-ON Time		150			180		ns	See Switching Time Test Circuit	
	10		t_{off}	Turn-OFF Time		130			150				
	11		$C_{S(off)}$	Source OFF Capacitance	9 Typical*						pF	V_S = –5 V, I_D = 0	f = 1 MHz
	12		$C_{D(off)}$	Drain OFF Capacitance	6 Typical*							V_D = –5 V, I_S = 0	
	13		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	14 Typical*							V_D = V_S = 0	
	14			Off Isolation	Typical > 50 dB at 10 MHz							R_L = 75 Ω	
75 Ω DG182, DG185, DG188, DG191	1		$r_{DS(on)}$	Drain-Source ON Resistance	75	75	150	100	100	150		V_D = –10 V	I_S = –10 mA, V_{IN} = 0.8 V or 2.0 V Note 1
	2	SWITCH	$I_{S(off)}$	Source OFF Leakage Current		1	100		5	100	nA	V_S = 10 V, V_D = –10 V, V+ = 10 V, V– = –20 V	V_{IN} = 2.0 V or 0.8 V Note 2
	3					1	100		5	100		V_S = 10 V, V_D = –10 V	
	4		$I_{D(off)}$	Drain OFF Leakage Current		1	100		5	100		V_D = 10 V, V_S = –10 V, V+ = 10 V, V– = –20 V	
	5					1	100		5	100		V_D = 10 V, V_S = –10 V	
	6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		–2	–200		–10	–200		V_D = V_S = –10 V	
	7	IN	I_{INL}	Input Current, Input Voltage Low	–250	–250	–250	–250	–250	–250	µA	V_{IN} = 0	
	8		I_{INH}	Input Current, Input Voltage High		10	20		10	20		V_{IN} = 5 V	
	9	DYNAMIC	t_{on}	Turn-ON Time		250			300		ns	See Switching Time Test Circuit	
	10		t_{off}	Turn-OFF Time		130			150				
	11		$C_{S(off)}$	Source OFF Capacitance	9 Typical*						pF	V_S = –5 V, I_D = 0	f = 1 MHz
	12		$C_{D(off)}$	Drain OFF Capacitance	6 Typical*							V_D = –5 V, I_S = 0	
	13		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	14 Typical*							V_D = V_S = 0	
	14			Off Isolation	Typical > 50 dB at 10 MHz							R_L = 75 Ω	

NOTES: 1. V_{IN} = 0.8 V or 2.0 V to turn ON switch under test. 2. V_{IN} = 0.8 V or 2.0 V to turn OFF switch under test.

ELECTRICAL CHARACTERISTICS Power Supply Current (25°C)

CHARACTERISTIC		A OR B SUFFIX MAX LIMITS DG180, DG181 DG182, DG189 DG190, DG191	DG183 DG184 DG185	DG186 DG187 DG188	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V– = –15 V, V_L = 5 V, V_R = 0
I+	Positive Supply Current	1.5	3	0.8	mA	All V_{IN} = 0 V
I–	Negative Supply Current	–5	–5.5	–3		
I_L	Logic Supply Current	4.5	4.5	3.2		
I_R	Reference Supply Current	–2	–2	–2		
I+	Positive Supply Current	1.5	0.1	0.8		All V_{IN} = 5 V
I–	Negative Supply Current	–5	–4	–3		
I_L	Logic Supply Current	4.5	4.5	3.2		
I_R	Reference Supply Current	–2	–2	–2		

CMJA + NC – DG184,DG185
CMJA + NIP – DG183

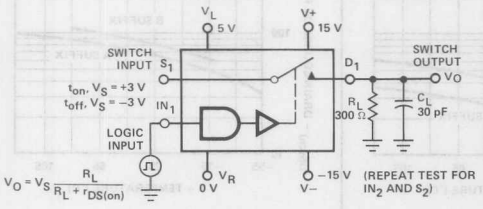
CMJB + NC – DG181, DG182, DG190, DG191
CMJB + NIP – DG180, DG189

CMJC + NC – DG187, DG188
CMJC + NIP – DG186

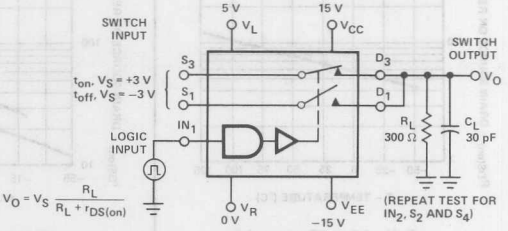
SWITCHING TIME TEST CIRCUITS

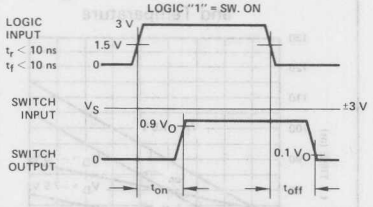
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

DG180 – DG185



DG186 – DG191





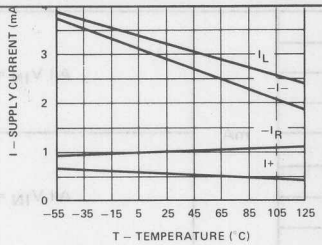
NOTE: LOGIC INPUT WAVEFORM IS INVERTED FOR SWITCHES THAT HAVE THE OPPOSITE LOGIC SENSE CONTROL

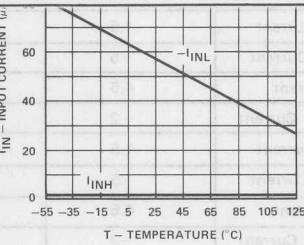
APPLICATION HINTS*

Switch Family	V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S Analog Voltage Range (V)
10 Ω	+15**	–15	+5	Gnd	2.0/0.8	–7.5 to +15
and	+10	–20	+5	Gnd	2.0/0.8	–12.5 to +10
30 Ω	+12	–12	+5	Gnd	2.0/0.8	–4.5 to +12
	+15**	–15	+5	Gnd	2.0/0.8	–10 to +15
75 Ω	+10	–20	+5	Gnd	2.0/0.8	–15 to +10
	+12	–12	+5	Gnd	2.0/0.8	–7 to +12

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Parameter Chart based on V+ = +15 V, V– = –15 V, V_L = 5 V, V_R = Gnd.



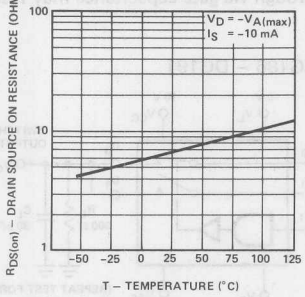


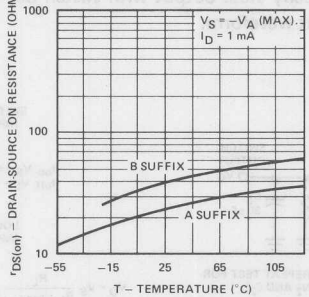
10 Ω
DG180
DG183
DG186
DG189

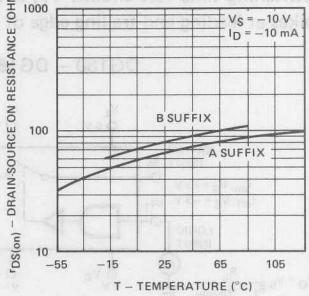
30 Ω
DG181
DG184
DG187
DG190

75 Ω
DG182
DG185
DG188
DG191

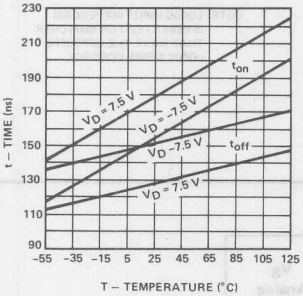
$r_{DS(on)}$ vs Temperature

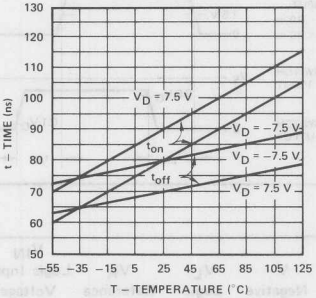


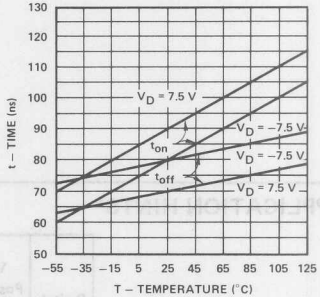




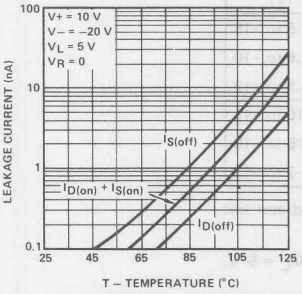
Switching Time vs V_D and Temperature



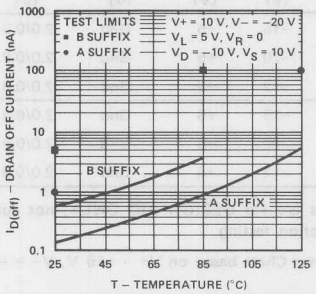




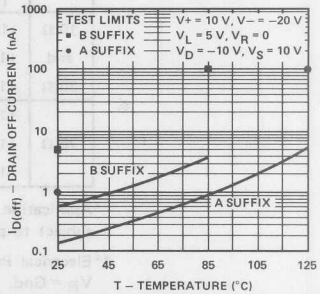
Leakage vs Temperature



$I_{D(off)}$ vs Temperature

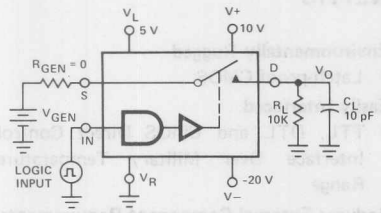


$I_{D(off)}$ vs Temperature



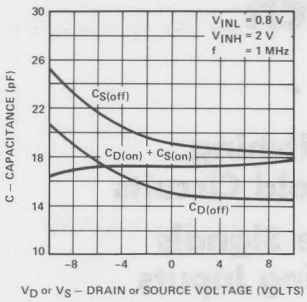
TYPICAL CHARACTERISTICS (Cont'd)

Typical delay, rise, fall, settling times, and switching transients in this circuit.

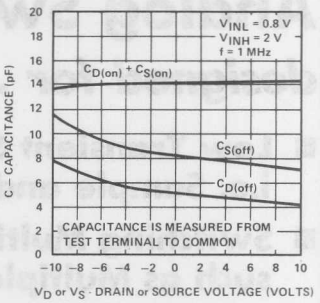


If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall times.

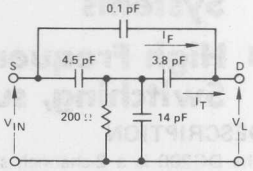
Capacitance vs V_D or V_S
10 Ω FET



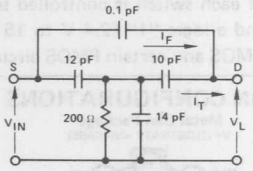
Capacitance vs V_D or V_S
30-75 Ω FET



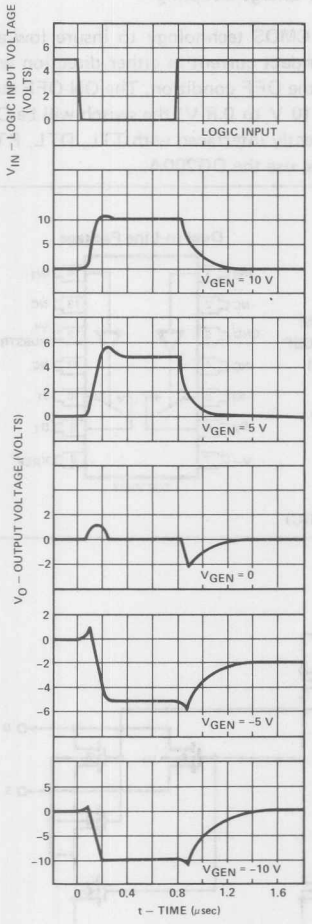
Equivalent "OFF" Circuit
30-75 Ω FET



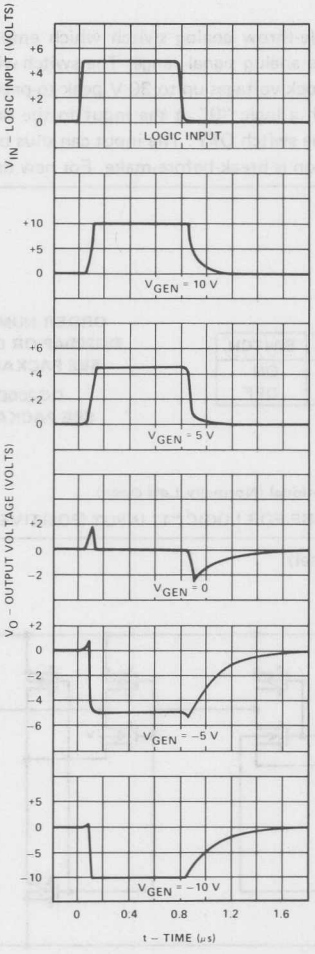
Equivalent "OFF" Circuit
10 Ω FET



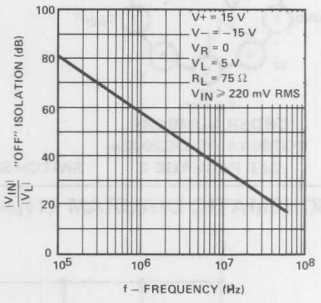
DG180, DG183, DG186
DG189



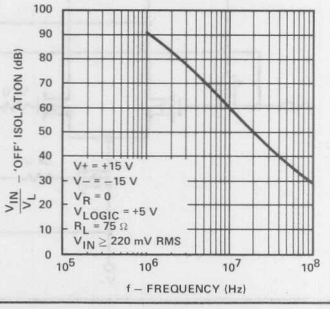
DG181, DG182, DG184,
DG185, DG187, DG188,
DG190, DG191



"OFF" Isolation vs Frequency
10 Ω FET



"OFF" Isolation vs Frequency
30-75 Ω FET



Dual Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Low Transient Switching i.e. Sample and Hold Circuits**
- **Switching Multiple Signals such as Multiplexing Inputs**
- **TTL Compatible Switching Systems**
- **High Frequency Signal Switching, such as Video Signals**

BENEFITS

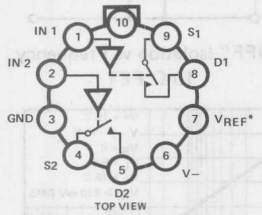
- **Environmentally Rugged**
 - Latch-proof CMOS
- **Easily Interfaced**
 - TTL, DTL and CMOS Direct Control Interface Over Military Temperature Range
- **Reduces External Component Requirements**
 - ±15 V Analog Signal Range with ±15 V Supplies
- **Reduced System Cross-Talk**
 - Break-Before-Make Switching
- **Eliminates Signal Error**
 - 10 pA Typical Leakage From Source or Drain
 - Low Charge Coupling

DESCRIPTION

The DG200 is a 2-channel, single-pole, single-throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0 V to 0.8 V) the switch will be ON, and a logic "1" (2.4 V to 15 V) will turn the switch OFF. The input can thus be directly interfaced with TTL, DTL, RTL CMOS and certain PMOS circuits. Switch action is break-before-make. For new designs, use the DG200A.

PIN CONFIGURATIONS

Metal Can Package
V+ (SUBSTRATE AND CASE)



TOP VIEW

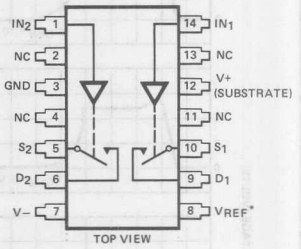
ORDER NUMBERS:
DG200AA OR DG200BA
SEE PACKAGE 2

LOGIC	SWITCH
0	ON
1	OFF

ORDER NUMBERS:
DG200AP OR DG200BP
SEE PACKAGE 11

DG200CJ
SEE PACKAGE 7

Dual-In-Line Package

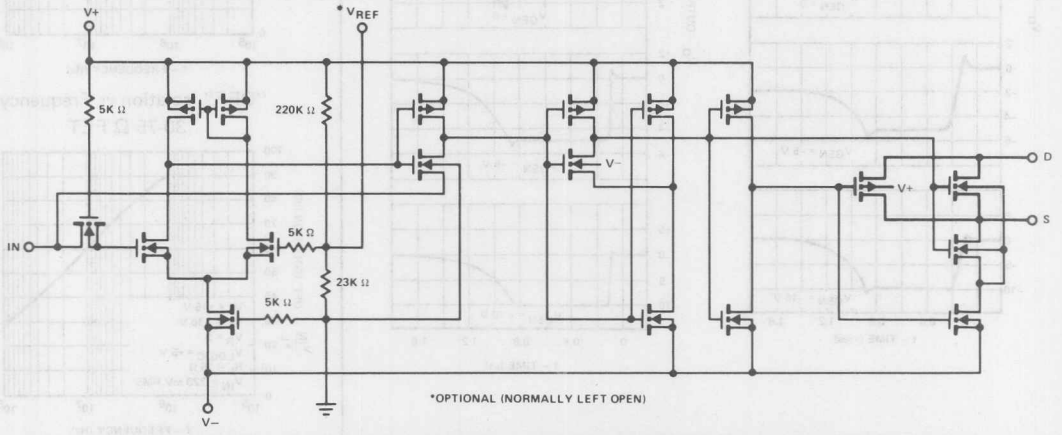


TOP VIEW

*Optional (Normally Left Open)

SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

SCHEMATIC DIAGRAM (Typical Channel)



*OPTIONAL (NORMALLY LEFT OPEN)

ABSOLUTE MAXIMUM RATINGS

V_{IN} and V_{REF} to Ground	−0.3 V, V+
V_S or V_D to V+	0, −32 V
V_S or V_D to V−	0, 32 V
V+ to Ground	16 V
V− to Ground	−16 V
Current, Any Terminal Except S or D	30 mA
Current, S or D	20 mA
Current, S or D Pulsed (1 msec, 10% Duty Cycle Max)	100 mA
Operating Temp. (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
(C Suffix)	0 to 70°C
Storage Temp. (A & B Suffix)	−65 to 150°C
(C Suffix)	−65 to +125°C
Power Dissipation (Package)*	
Metal Can**	450 mW
14 Pin DIP***	825 mW
14 Pin Plastic DIP****	470 mW

*Device mounted with all leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C
***Derate 11 mW/°C above 75°C
****Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

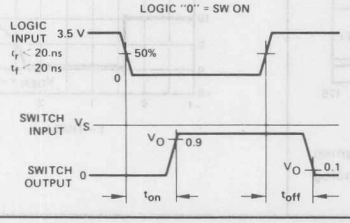
		CHARACTERISTIC		TYP† 25°C	MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX −20/0°C	B/C SUFFIX 25°C	B/C SUFFIX 85/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Gnd = 0, V_{REF} = Open***	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	45	70	70	100	80	80	100	Ω	V_D = 10 V	V_{IN} = 0.8 V, I_S = −1 mA
3				45	70	70	100	80	80	100		V_D = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current	+0.01		2	100		5	100	nA	V_S = 14 V, V_D = −14 V	V_{IN} = 2.4 V
5				−0.02		−2	−100		−5	−100		V_S = −14V, V_D = 14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	+0.01		2	100		5	100		V_D = 14 V, V_S = −14 V	
7				−0.02		−2	−100		−5	−100		V_D = −14 V, V_S = 14 V	
8		$I_{D(on)}$*	Channel ON Leakage Current	+0.1		2	200		−5	200		V_D = V_S = 14 V	V_{IN} = 0.8 V
9				−0.1		−2	−200		−5	−200		V_D = V_S = −14 V	
10	INPUT	I_{INH}	Input Current Input Voltage High	0.0009		−1	−10		−1	−10	μA	V_{IN} = 2.4 V	
11				0.005		1	10		1	10		V_{IN} = 15 V	
12		$I_{IN(peak)}$	Peak Input Current Required for Transition	−150								See Curve I_{IN} vs V_{IN}	
13		I_{INL}	Input Current, Input Voltage Low	−.0015		−1	−10		−1	−10		V_{IN} = 0 V	
14	DYNAMIC	t_{on}	Turn-ON Time	440		1000			1000		ns	See Switching Time Test Circuit	
15		t_{off}	Turn-OFF Time	370		500			500				
16		$C_{S(off)}$	Source OFF Capacitance	9.0							pF	V_S = 0, V_{IN} = 5 V	
17		$C_{D(off)}$	Drain OFF Capacitance	9.0								V_D = 0, V_{IN} = 5 V	f = 140 kHz
18		$C_{D(on)}$ + $C_{S(on)}$	Channel ON Capacitance	25								V_D = V_S = 0, V_{IN} = 0	
19		OFF Isolation		72							dB	V_{IN} = 5 V, R_L = 1K Ω, C_L = 15 pF, V_S = 7 VRMS, f = 500 kHz	
20	SUP	I+	Positive Supply Current	+2.3		4			4		mA	Both Channels "ON," V_{IN} = 0	
21		I−	Negative Supply Current	−2.3		−4			−4				
22		I+ Standby	Positive Supply Current	+0.7		2			2			Both Channels "OFF," V_{IN} = 5 V	
23		I− Standby	Negative Supply Current	−0.6		−2			−2				

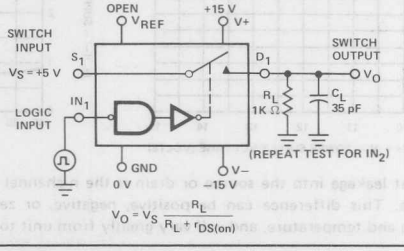
ICXE

NOTES:
†Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
*$I_{D(on)}$ is leakage from driver into "ON" switch.
**"OFF" isolation $\triangleq$ 20 log V_S/V_D, V_S = input to OFF switch, V_D = output
***Functional operation is possible for supply voltages less than 15 V, but the input logic threshold will shift. For V+ = −V− = 10 V, 1.4 V may be applied to V_{REF} terminal. The V_{REF} terminal has $R_{IN} \geq$ 21K Ω. See Applications Section.

SWITCHING TIME TEST CIRCUIT

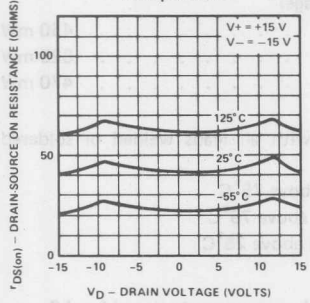
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



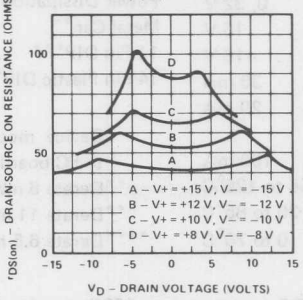


TYPICAL CHARACTERISTICS

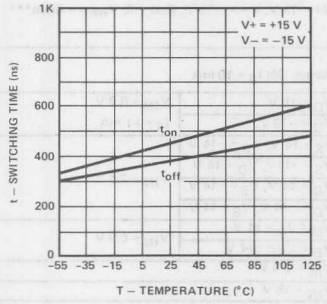
$r_{DS(on)}$ vs V_D and Temperature



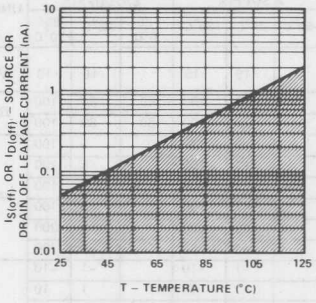
$r_{DS(on)}$ vs V_D and Power Supply Voltage



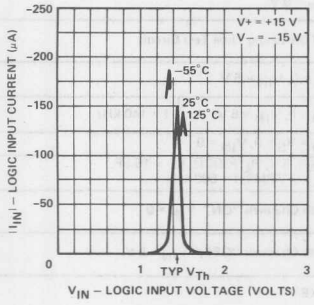
Switching Time vs Temperature



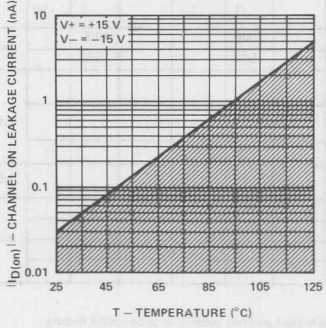
$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*



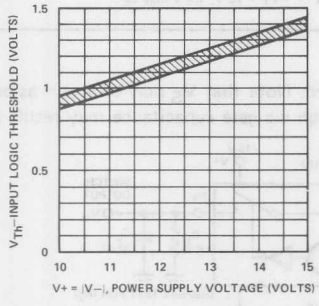
I_{IN} vs V_{IN}



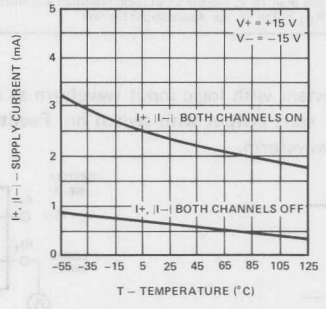
$I_{D(on)}$ vs Temperature*



V_{Th} (Input Logic Threshold) vs Power Supply Voltage

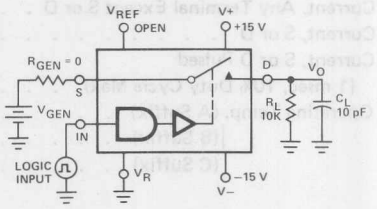


Supply Current vs Temperature

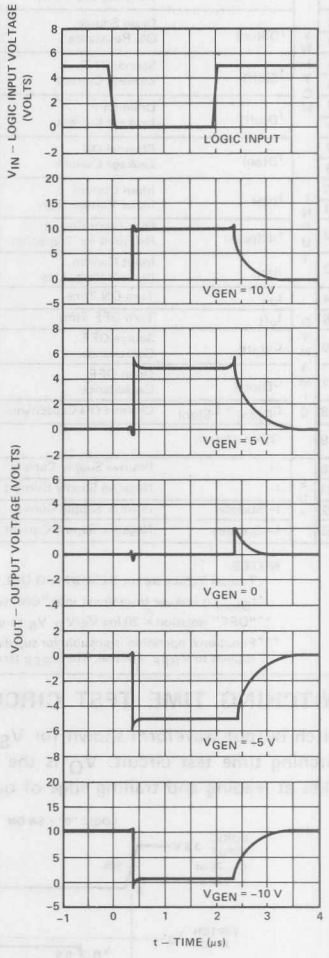


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

Typical delay, rise, fall, settling times, and switching transients in this circuit.

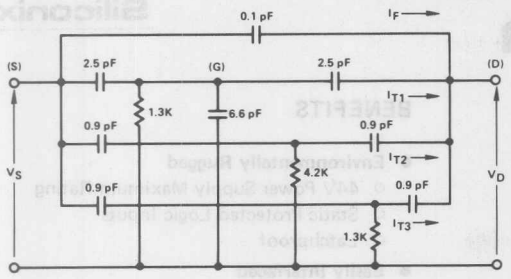


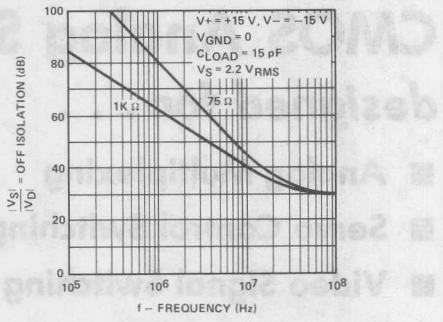
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater spikes.

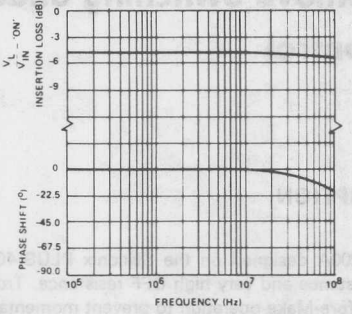


TYPICAL CHARACTERISTICS (Cont'd)

"OFF" Isolation Equivalent Circuit and Data







APPLICATIONS

Application Hints*

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{REF} Reference Pin Connection (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
+15**	−15	Open	2.4/0.8	−15 to +15
+12	−12	Open or 1.4 V	2.4/0.8	−12 to +12
+10	−10	1.4 V	2.4/0.8	−10 to +10
+8***	−8	1.4 V	2.4/0.8	−8 to +8

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics chart based on V+ = +15 V, V− = −15 V, V_{REF} = Open.

***Operation below ±8 V is not recommended.

Logic Inputs

Logic input circuitry protects the input MOS gate from static transients. A series MOS device shuts off when V_{IN} exceeds the positive power supply. Negative transients are clamped to ground by a diode clamp.

The input voltage characteristics have a current spike occurring at the transition voltage when the logic goes from V_{INH} to V_{INL}. If a series resistor is used for additional static protection, it should be limited to less than 4.7 KΩ to insure switching with worst case current spikes.

The Function of V_{REF}

V_{REF} is an internal connection which allows the user to establish the logic threshold voltage at which the switch changes state. The actual threshold voltage is equal to the voltage on the V_{REF} pin. V_{REF} is internally connected for a 1.4 V threshold at V+ = +15 V. For other thresholds and/or supply voltages, one may connect V_{REF} to a voltage source or resistive divider whose output voltage is equal to the desired threshold. The internal impedance of V_{REF} is 21 KΩ ±30%.

Additionally, to adjust V_{REF}, a single pullup resistor can be used from the V_{REF} pin to a positive supply voltage to shunt the upper internal divider resistor. The equation below shows the calculation of the shunt resistor for the desired logic threshold voltage – this calculation is based on nominal internal resistor values, which are ±30% in absolute magnitude. The adjusted trip point voltage (V_{REF}) should be limited to an upper level of 5 V to avoid input logic switching transition hysteresis.

$$R_{SHUNT} = \frac{R1 \times R2\left(\frac{V^+}{V_{tr}} - 1\right)}{\left[R1 - R2\left(\frac{V^+}{V_{tr}} - 1\right)\right]}$$

Calculation of R_{SHUNT}

Where $R1 \simeq 220$ KΩ: nominal values,
$R2 \simeq 23$ KΩ ±30% run to run

Example: for V+ = 15 V, V_{TRIP} = 5 V, using nominal R1, R2 calc R_{SHUNT} = 58 KΩ.

Dual Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Analog Multiplexing**
- **Servo Control Switching**
- **Video Signal Switching**
- **Remove Switching under TTL Logic Control**

BENEFITS

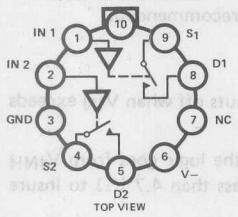
- **Environmentally Rugged**
 - 44V Power Supply Maximum Rating
 - Static Protected Logic Inputs
 - Latchproof
- **Easily Interfaced**
 - TTL and CMOS Compatible without Pull-Up Resistors
- **Pin for Pin Compatible with**
 - Analog Devices ADG200
 - Harris HI200
 - Intersil DG200
 - Siliconix DG200

DESCRIPTION

The DG200A designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 70 ohms contact (ON) resistance and very high OFF resistance. True switch action takes place over the full analog signal range of ±15 V, with Break-Before-Make operation to prevent momentary shorting of signal inputs.

PIN CONFIGURATIONS

Metal Can Package
V+ (SUBSTRATE AND CASE)

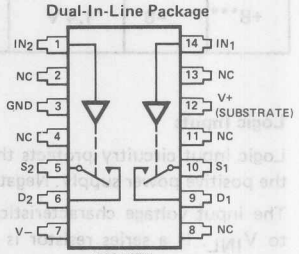


TOP VIEW

LOGIC	SWITCH
0	ON
1	OFF

ORDER NUMBERS:
DG200AAA OR DG200ABA
SEE PACKAGE 2

Dual-In-Line Package



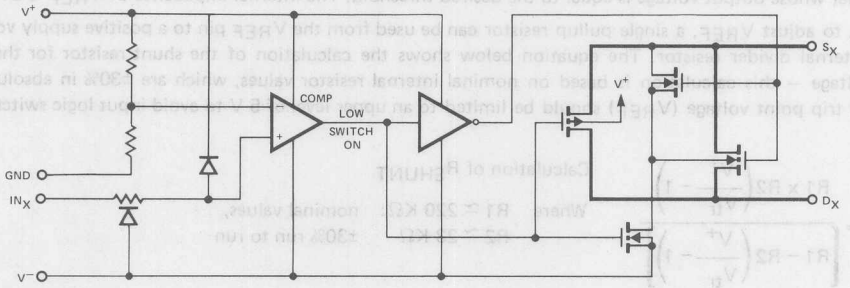
TOP VIEW

ORDER NUMBERS:
DG200AAK OR DG200ABK
OR DG200ACK
SEE PACKAGE 9

DG200ACJ
SEE PACKAGE 7

SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

SCHEMATIC DIAGRAM (typical channel)



ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–

V+ 44 V
GND 25 V
Digital inputs[4], V_S, V_D –2 V to (V^+ +2 V) or 20 mA, whichever occurs first.
Current, Any Terminal Except S or D 30 mA
Current, S or D 20 mA
Current, S or D Pulsed
(1 msec, 10% Duty Cycle Max) 100 mA
Operating Temp. (A Suffix) –55 to 125°C
(B Suffix) –20 to 85°C
(C Suffix) 0 to 70°C
Storage Temp. (A & B Suffix) –65 to 150°C
(C Suffix) –65 to +125°C
Power Dissipation (Package)*
Metal Can** 450 mW
14 Pin DIP*** 825 mW
14 Pin Plastic DIP**** 470 mW

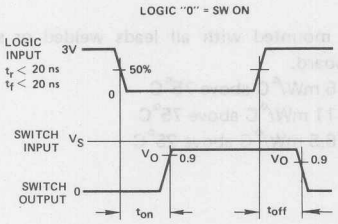
*Device mounted with all leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C
***Derate 11 mW/°C above 75°C
****Derate 6.5 mW/°C above 25°C

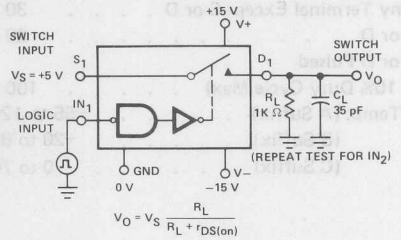
ELECTRICAL CHARACTERISTICS All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		TYP[1] 25°C	MAX LIMITS A SUFFIX –55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX –20/0°C	B/C SUFFIX 25°C	B/C SUFFIX 85/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V– = –15 V, Gnd = 0,	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V		
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	45	70	70	100	80	80	100	Ω	V_D = 10 V	V_{IN} = 0.8 V, I_S = –1 mA
3				45	70	70	100	80	80	100		V_D = –10 V	
4		$I_{S(off)}$	Source OFF Leakage Current	+0.01		2	100		5	100	nA	V_S = +14 V, V_D = –14 V	V_{IN} = 2.4 V
5				–0.02		–2	–100		–5	–100		V_S = –14 V, V_D = 14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	+0.01		2	100		5	100		V_D = 14 V, V_S = –14 V	
7				–0.02		–2	–100		–5	–100		V_D = –14 V, V_S = 14 V	
8		$I_{D(on)}$[2]	Channel ON Leakage Current	+0.1		2	200		–5	200		V_D = V_S = 14 V	V_{IN} = 0.8 V
9				–0.1		–2	–200		–5	–200		V_D = V_S = –14 V	
10	INPUT	I_{INH}	Input Current Input Voltage High	0.0009		–1	–10		–1	–10	µA	V_{IN} = 2.4 V	
11				0.005		1	10		1	10		V_{IN} = 15 V	
12		I_{INL}	Input Current Input Voltage Low	–.0015		–1	–10		–1	–10		V_{IN} = 0 V	
13	DYNAMIC	t_{on}	Turn-ON Time	440		1000			1000		ns	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time	370		500			500				
15		Q	Charge Injection	–10							pC	C_L = 1000pF, V_{GEN} = 0V, R_{GEN} = 0Ω	
16		$C_{S(off)}$	Source OFF Capacitance	9.0							pF	V_S = 0, V_{IN} = 5 V	f = 140 kHz
17		$C_{D(off)}$	Drain OFF Capacitance	9.0								V_D = 0, V_{IN} = 5V	
18		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	25								V_D = V_S = 0, V_{IN} = 0	
19		OIRR[3]	OFF Isolation	75							dB	V_{IN} = 5 V	
20		CCRR	Channel to Channel Crosstalk	90								V_S = 2 Vpp	Z_L = 75Ω, f = 1 MHz
21	SUP	I+	Positive Supply Current	0.8		2			2		mA	Both Channels "ON", or "OFF" V_{IN} = 0 or 2.4 V	
22		I–	Negative Supply Current	–.23		–1			–1				

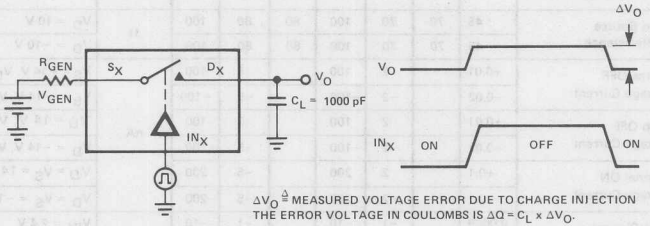
NOTES:
1. Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. "OFF" isolation $\triangleq$ 20 log V_S/V_D, V_S = input to OFF switch, V_D = output
4. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ICME



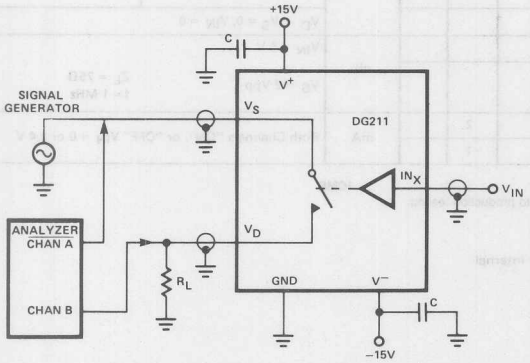


CHARGE INJECTION TEST CIRCUIT



$\Delta V_O \triangleq$ MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION
THE ERROR VOLTAGE IN COULOMBS IS $\Delta Q = C_L \times \Delta V_O$.

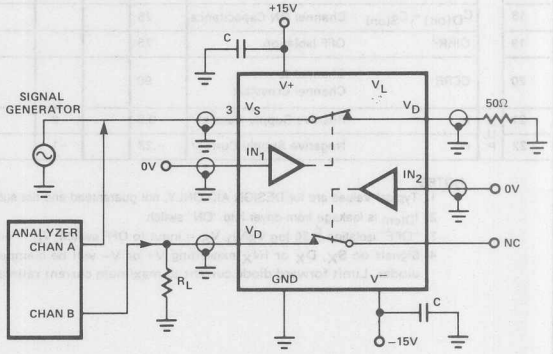
OIRR OFF ISOLATION TEST CIRCUIT



C = .001μF// .1μF CHIP CAPACITORS

$OIRR = 20 \text{ LOG} \left| \frac{V_S}{V_D} \right|$

CCRR CHANNEL TO CHANNEL CROSSTALK TEST CIRCUIT



C = .001μF// .1μF CHIP CAPACITORS

$CCRR = 20 \text{ LOG} \left| \frac{V_{S1}}{V_{D2}} \right|$

Quad Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Low Transient Switching i.e. Sample and Hold Circuits**
- **Switching Multiple Signals such as Multiplexing Inputs**
- **High Frequency Signal Switching**
- **TTL Compatible Systems**

BENEFITS

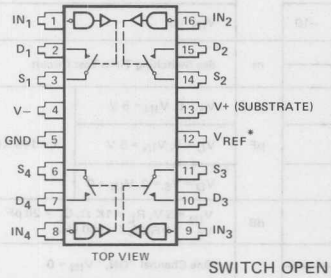
- **Environmentally Rugged**
 - Latch-proof CMOS
- **Reduced Switching Error**
 - Low Charge Coupling
- **Easily Interfaced**
 - TTL, DTL and CMOS Direct Control Interface Over Military Temperature Range
- **Reduces External Component Requirements**
 - ±15 V Analog Signal Range with ±15 V Supplies
- **Reduced System Cross-Talk**
 - Break-Before-Make Switching
- **Eliminates Signal Error**
 - 10 pA Typical Leakage From Source or Drain

DESCRIPTION

The DG201 is a 4-channel single pole signal throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0 V to 0.8 V) the switch will be ON, and a logic "1" (2.4 V to 15 V) will turn the switch OFF. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make. For new designs, use the DG201A.

PIN CONFIGURATION

Dual-In-Line Package



ORDER NUMBERS:
DG201AP OR DG201BP
SEE PACKAGE 12

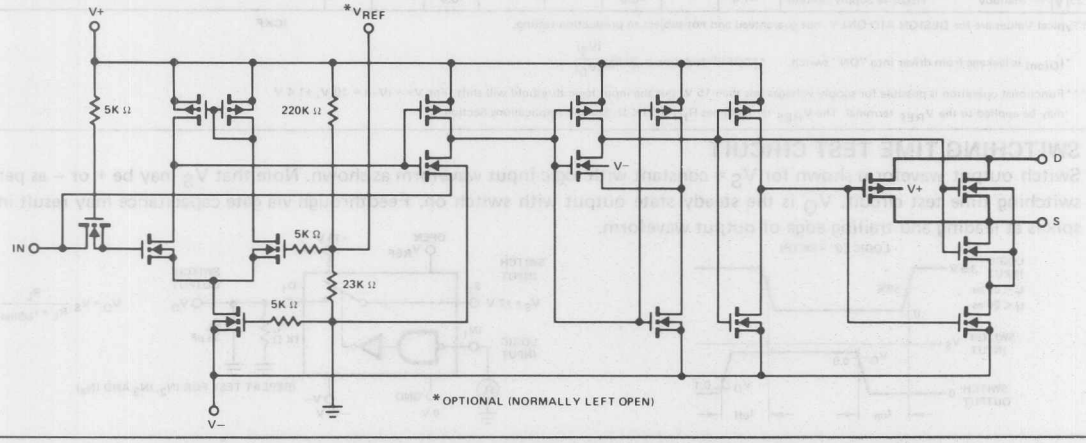
DG201CJ
SEE PACKAGE 8

LOGIC	SWITCH
0	ON
1	OFF

*Optional (Normally Left Open)

SWITCH OPEN FOR LOGIC "1" INPUT (POSITIVE LOGIC)

SCHEMATIC DIAGRAM (Typical Channel)



*OPTIONAL (NORMALLY LEFT OPEN)

ABSOLUTE MAXIMUM RATINGS

V_{IN} and V_{REF} to Ground −0.3 V, V+
V_S or V_D to V+ 0, −32 V
V_S or V_D to V− 0, 32 V
V+ to Ground 16 V
V− to Ground −16 V
Current, Any Terminal Except S or D 30 mA
Continuous Current, S or D 20 mA
Peak Current, S or D
(pulsed at 1 msec, 10% duty cycle max) . . 70 mA
Storage Temperature (A & B Suffix) . . −65 to 150°C
(C Suffix) −65 to 125°C
Operating Temperature (A Suffix) . . . −55 to 125°C
(B Suffix) . . . −20 to 85°C
(C Suffix) . . . 0 to 70°C
Power Dissipation (Package)*
16 Pin DIP** 900 mW
16 Pin Plastic DIP*** 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		TYP† 25°C	MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX −20°C/ 0°C	B/C SUFFIX 25°C	B/C SUFFIX 85°C/ 70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Gnd = 0, V_{REF} = Open***	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	115	175	175	250	200	200	250	Ω	V_D = 10 V	V_{IN} = 0.8 V, I_S = −1 mA
3				75	175	175	250	200	200	250		V_D = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current	0.01		1	100		5	100	nA	V_S = 14 V, V_D = −14V	V_{IN} = 2.4 V
5				−0.02		−1	−100		−5	−100		V_S = −14V, V_D = 14V	
6		$I_{D(off)}$	Drain OFF Leakage Current	0.01		1	100		5	100		V_D = 14V, V_S = −14V	
7				−0.02		−1	−100		−5	−100		V_D = −14V, V_S = 14V	
8		$I_{D(on)}$*	Drain ON Leakage Current	0.1		1	200		5	200		V_D = V_S = 14V	V_{IN} = 0.8 V
9				−0.15		−1	−200		−5	−200		V_D = V_S = −14V	
10	INPUT	I_{INH}	Input Current, Input Voltage High	−.0004		−1	−10		−1	−10	μA	V_{IN} = 2.4 V	
11				.003		1	10		1	10		V_{IN} = 15 V	
12		$I_{IN(peak)}$	Peak Input Current Required for Transition	−120								See Curve I_{IN} vs V_{IN}	
13		I_{INL}	Input Current, Input Voltage Low	−.0004		−1	−10		−1	−10		V_{IN} = 0	
14		t_{on}	Turn-ON Time	580		1000					ns	See Switching Time Test Circuit	
15		t_{off}	Turn-OFF Time	370		500							
16	DYNAMIC	$C_{S(off)}$	Source OFF Capacitance	7							pF	V_S = 0, V_{IN} = 5 V	f = 140 KHz
17		$C_{D(off)}$	Drain OFF Capacitance	7								V_D = 0, V_{IN} = 5 V	
18		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	20								V_D = V_S = 0, V_{IN} = 0	
19		Off Isolation**		54							dB	V_{IN} = 5 V, R_L = 1K Ω, C_L = 20 pF V_S = 7 VRMS, f = 500 kHz	
20	SUPPLY	I+	Positive Supply Current	2.1		4.0			4.0		mA	One Channel "ON," V_{IN} = 0	
21		I−	Negative Supply Current	−2.1		−4.0			−4.0				
22		I+ Standby	Positive Supply Current	1.4		3.0			3.0			All Channels "OFF," V_{IN} = 5 V	
23		I− Standby	Negative Supply Current	−1.4		−3.0			−3.0				

†Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

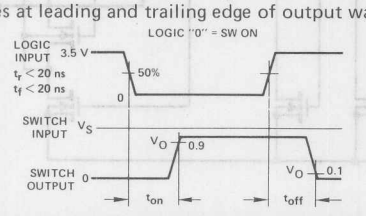
*$I_{D(on)}$ is leakage from driver into "ON" switch. **"OFF" Isolation = $20 \log \frac{|V_S|}{|V_D|}$

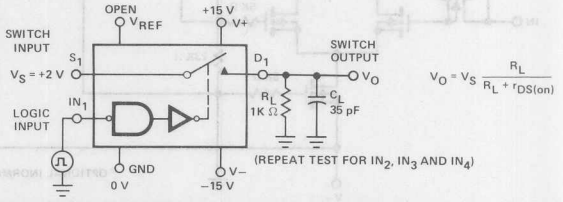
***Functional operation is possible for supply voltages less than 15 V, but the input logic threshold will shift. For V+ = |V−| = 10 V, +1.4 V may be applied to the V_{REF} terminal. The V_{REF} terminal has R_{IN} = 21K Ω. See the Applications Section.

ICXF

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





APPLICATIONS

Application Hints*

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{REF} Reference Pin Connection (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
+15**	−15	Open	2.4/0.8	−15 to +15
+12	−12	Open or 1.4 V	2.4/0.8	−12 to +12
+10	−10	1.4 V	2.4/0.8	−10 to +10
+8***	−8	1.4 V	2.4/0.8	−8 to +8

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics chart based on V+ = +15 V, V− = −15 V, V_{REF} = Open.

***Operation below ±8 V is not recommended.

Logic Inputs

Logic input circuitry protects the input MOS gate from static transients. A series MOS device shuts off when V_{IN} exceeds the positive power supply. Negative transients are clamped to ground by a diode clamp.

The input voltage characteristics have a current spike occurring at the transition voltage when the logic goes from V_{INH} to V_{INL}. If a series resistor is used for additional static protection, it should be limited to less than 5.6 KΩ to insure switching with worst case current spikes.

The Function of V_{REF}

V_{REF} is an internal connection which allows the user to establish the logic threshold voltage at which the switch changes state. The actual threshold voltage is equal to the voltage on the V_{REF} pin. V_{REF} is internally connected for a 1.4 V threshold at V+ = +15 V. For other thresholds and/or supply voltages, one may connect V_{REF} to a voltage source or resistive divider whose output voltage is equal to the desired threshold. The internal impedance of V_{REF} is 21 KΩ ±30%.

Additionally, to adjust V_{REF}, a single pullup resistor can be used from the V_{REF} pin to a positive supply voltage to shunt the upper internal divider resistor. The equation below shows the calculation of the shunt resistor for the desired logic threshold voltage — this calculation is based on nominal internal resistor values, which are ±30% in absolute magnitude. The adjusted trip point voltage (V_{REF}) should be limited to an upper level of 5 V to avoid input logic switching transition hysteresis.

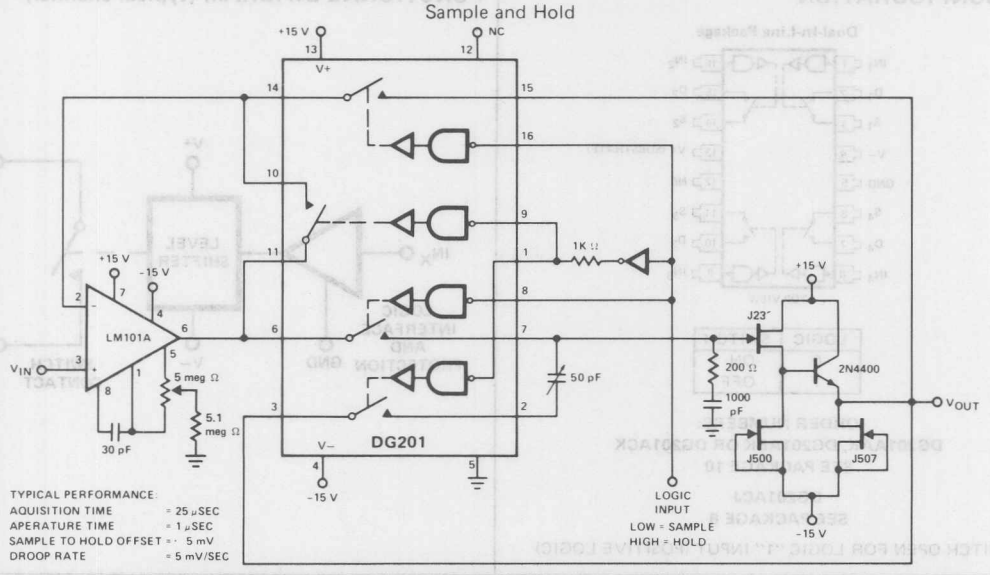
$$R_{SHUNT} = \frac{R1 \times R2\left(\frac{V^+}{V_{tr}} - 1\right)}{\left[R1 - R2\left(\frac{V^+}{V_{tr}} - 1\right)\right]}$$

Calculation of R_{SHUNT}

Where R1 ≃ 220 KΩ nominal values,
R2 ≃ 23 KΩ ±30% run to run

Example: for V+ = 15 V, V_{TRIP} = 5 V, using nominal R1, R2 calc R_{SHUNT} = 58 KΩ.

Sample and Hold



designed for . . .

- **Analog Multiplexing**
- **Remote Switching under TTL Logic Control**
- **Servo Control Switching**
- **Sampled Data Systems**
- **Programmable Gain Amplifiers**

BENEFITS

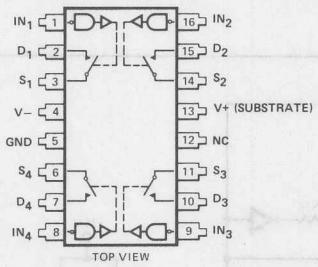
- **Environmentally Rugged**
 - 44V Power Supply Maximum Rating
 - Static Protected Logic Inputs
 - Latchproof
- **Easily Interfaced**
 - TTL and CMOS Compatible without Pull-Up Resistors
 - Logic Inputs Accept ± Comparator Transitions without Series Current Limiting Resistors
- **Pin for Pin Compatible with**
 - Analog Devices ADG201
 - Harris HI201
 - Intersil DG201
 - Siliconix DG201

DESCRIPTION

The DG201A designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 175 ohms contact resistance and very high OFF resistance. True switch action takes place over the full analog signal range of ±15V, with Break-Before-Make operation to prevent momentary shorting of signal inputs. Charge injection has been reduced by design to minimize spikes during switching transitions.

PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

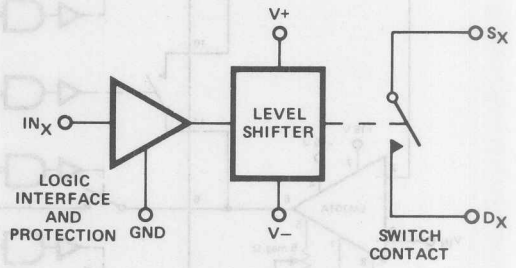
LOGIC	SWITCH
0	ON
1	OFF

ORDER NUMBERS:
DG201AAK, DG201ABK OR DG201ACK
SEE PACKAGE 10

DG201ACJ
SEE PACKAGE 8

SWITCH OPEN FOR LOGIC "1" INPUT (POSITIVE LOGIC)

FUNCTIONAL DIAGRAM (typical channel)



Digital inputs, V_S, V_D −2 V to (V+ +2 V) or 20 mA, whichever occurs first.
Current, Any Terminal Except S or D 30 mA
Continuous Current, S or D 20 mA
Peak Current, S or D
(pulsed at 1 msec, 10% duty cycle max) . . 70 mA
Storage Temperature (A & B Suffix) . . −65 to 150°C
(C Suffix) −65 to 125°C

Power Dissipation (Package)
16 Pin DIP** 900 mW
16 Pin Plastic DIP*** 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

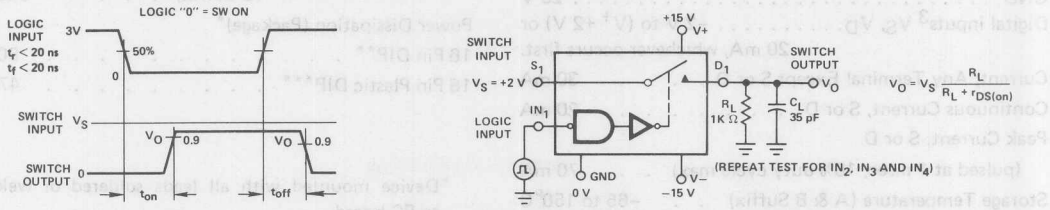
		CHARACTERISTIC		TYP 25°	MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX −20°C/0°C	B/C SUFFIX 25°C	B/C SUFFIX 85°C/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Gnd = 0	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V		
2		$r_{DS(on)}$	Drain Source ON Resistance	105	175	175	250	200	200	250	Ω	V_D = 10 V	V_{IN} = 0.8 V, I_S = −1 mA
3				115	175	175	250	200	200	250		V_D = −10 V	
4	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	0.01		1	100		5	100	nA	V_S = 14 V, V_D = −14 V	V_{IN} = 2.4 V
5				−0.02		−1	−100		−5	−100		V_S = −14 V, V_D = 14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	0.01		1	100		5	100		V_D = 14 V, V_S = −14 V	
7				−0.02		−1	−100		−5	−100		V_D = −14 V, V_S = 14 V	
8		$I_{D(on)}$[2]	Drain ON Leakage Current	0.1		1	200		5	200	μA	V_D = V_S = 14 V	V_{IN} = 0.8 V
9				−0.15		−1	−200		−5	−200		V_D = V_S = −14 V	
10	INPUT	I_{INH}	Input Current Input Voltage High	−.0004		−1	−10		−1	−10		V_{IN} = 2.4 V	
11				.003		1	10		1	10		V_{IN} = 15 V	
12		I_{INL}	Input Current Input Voltage Low	−.0004		−1	−10		−1	−10		V_{IN} = 0 V	
13	DYNAMIC	t_{on}	Turn-ON Time	480		600			600		ns	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time	370		450			450				
15		Q	Charge Injection	20							pC	C_L = 1000pF V_{GEN} = 0V R_{GEN} = 0Ω	
16		$C_{S(off)}$	Source OFF Capacitance	5							pF	V_S = 0, V_{IN} = 5 V	f = 140 kHz
17		$C_{D(off)}$	Drain OFF Capacitance	5								V_D = 0, V_{IN} = 5V	
18		$C_{D(on)}$ + $C_{S(on)}$	Channel ON Capacitance	16								V_D = V_S = 0, V_{IN} = 0	
19		OIRR	OFF Isolation	70							dB	V_{IN} = 5 V V_S = 2 Vpp, f = 100 KHz Z_L = 75Ω	
20		CCRR	Channel to Channel Crosstalk	90									
21	SUP	I+	Positive Supply Current	.9		2			2		mA	All Channels "ON" or "OFF", V_{IN} = 0 or 2.4 V	
22		I−	Negative Supply Current	−.3		−1			−1				

NOTES:
1. Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

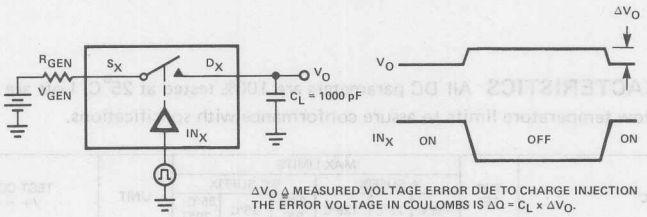
ICMC-B

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

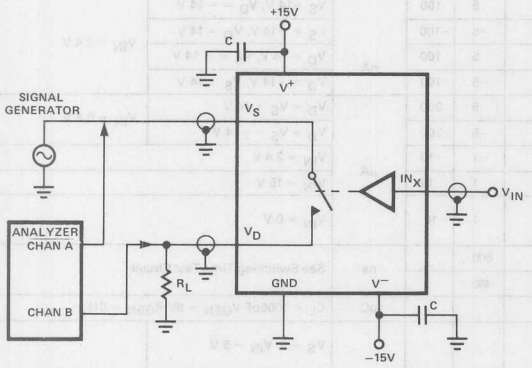


CHARGE INJECTION TEST CIRCUIT



$\Delta V_O \triangleq$ MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION
THE ERROR VOLTAGE IN COULOMBS IS $\Delta Q = C_L \times \Delta V_O$.

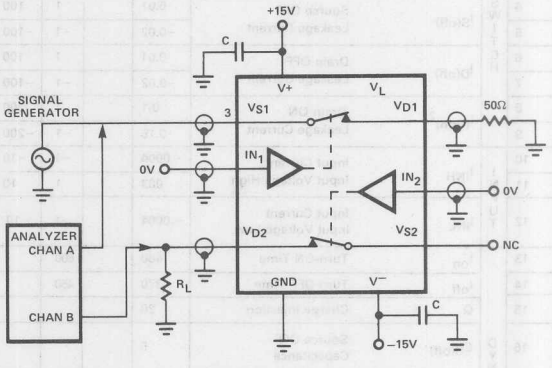
OIRR-OFF ISOLATION TEST CIRCUIT



C = .001μF// .1μF CHIP CAPACITORS

$OIRR = 20 \text{ LOG} \left| \frac{V_S}{V_D} \right|$

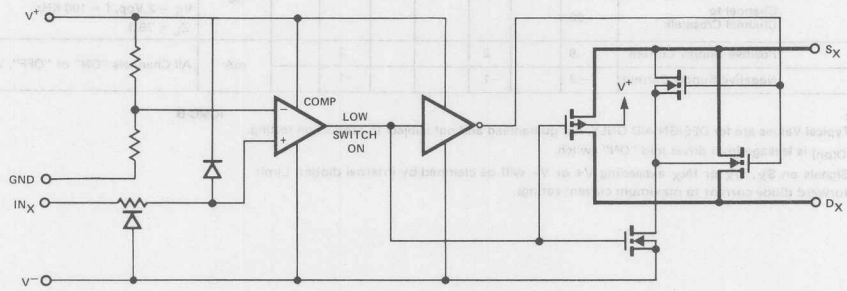
CCRR-CHANNEL TO CHANNEL CROSSTALK TEST CIRCUIT



C = .001μF// .1μF CHIP CAPACITORS

$CCRR = 20 \text{ LOG} \left| \frac{V_{S1}}{V_{D2}} \right|$

SCHEMATIC DIAGRAM (typical channel)



Quad Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Analog Multiplexing**
- **Remote Switching under TTL Logic Control**
- **Servo Control Switching**
- **Sampled Data Systems**
- **Programmable Gain Amplifiers**

BENEFITS

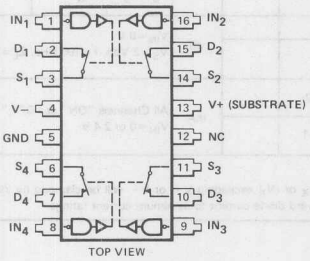
- **Environmentally Rugged**
 - 44 V Power Supply Max Rating
 - Static Protected Logic Inputs
 - Latch Proof
- **Easily Interfaced**
 - TTL and CMOS Compatible Without Pullup Resistors
 - Logic Inputs Accept ± Comparator Transitions Without Series Current Limiting Resistors
- **Pin for Pin Compatible With**
 - Intersil IH202
 - National LF11202

DESCRIPTION

The DG202 designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 175 ohms contact resistance and very high OFF resistance. True switch action takes place over the full analog signal range of ±15 V, with BREAK-BEFORE-MAKE operation to prevent momentary shorting of signals inputs. Charge injection has been reduced by design to minimize spikes during switching transitions.

PIN CONFIGURATION

Dual In-Line Package



TOP VIEW

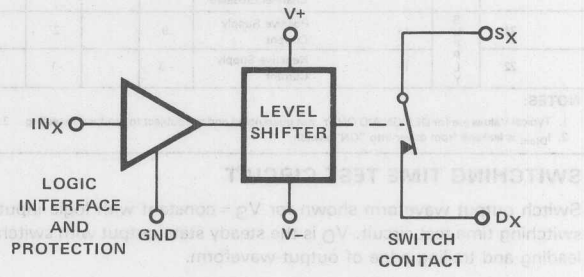
LOGIC	SWITCH
0	OFF
1	ON

ORDER NUMBERS:
DG202AK, DG202BK OR DG202CK
SEE PACKAGE 10

ORDER NUMBER:
DG202CJ
SEE PACKAGE 8

SWITCH CLOSED FOR LOGIC "1" INPUT (POSITIVE LOGIC)

FUNCTIONAL DIAGRAM (typical switch)



20 mA, whichever occurs first
Current, Any Terminal Except S or D 30 mA
Continuous Current, S or D 20 mA
Peak Current S or D
(pulsed at 1 msec, 10% duty cycle max) 70 mA
Storage Temperature (A & B Suffix) −65 to 150°C
(C Suffix) −65 to 125°C

16-Pin Plastic DIP*** 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		TYP[1] 25°C	MAX LIMITS A SUFFIX -55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX -20°C/ 0°C	B/C SUFFIX 25°C	B/C SUFFIX 85°C/ 70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V- = -15 V, GND = 0	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V		
2	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	105	175	175	250	200	200	250	Ω	V_D = 10 V	V_{IN} = 2.4 V, I_S = -1 mA
3				115	175	175	250	200	200	250		V_D = -10 V	
4		$I_{S(off)}$	Source OFF Leakage Current	0.01		1	100		5	100	nA	V_S = 14 V, V_D = -14 V	V_{IN} = 0.8 V
5				-0.02		-1	-100		-5	-100		V_S = -14 V, V_D = 14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	0.01		1	100		5	100		V_D = 14 V, V_S = -14 V	
7				-0.02		-1	-100		-5	-100		V_D = -14 V, V_S = 14 V	
8		$I_{D(on)}$[2]	Drain ON Leakage Current	0.1		1	200		5	200		$V_D = V_S$ = 14 V	V_{IN} = 2.4 V
9				-0.15		-1	-200		-5	-200		$V_D = V_S$ = -14 V	
10	INPUT	I_{INH}	Input Current, Input Voltage High	.0004		-1	-10		-1	-10	μA	V_{IN} = 2.4 V	
11				.003		1	10		1	10		V_{IN} = 15 V	
12		I_{INL}	Input Current, Input Voltage Low	-.0004		-1	-10		-1	-10		V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn-ON Time	480		600			600		ns	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time	370		450			450				
15		Q	Charge Injection	20							pC	C_L = 1000pF, V_{GEN} = 0 V, R_{GEN} = 0Ω	
16		$C_{S(off)}$	Source OFF Capacitance	5							pF	V_S = 0, V_{IN} = 0 V	f = 140 KHz
17		$C_{D(off)}$	Drain OFF Capacitance	5								V_D = 0, V_{IN} = 0 V	
18		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	16								$V_D = V_S$ = 0, V_{IN} = 5 V	
19		OIRR	Off Isolation	70							dB	V_{IN} = 0 V V_S = 2 Vpp, f = 100 KHz, Z_L = 75Ω	
20		CCRR	Channel to Channel Crosstalk	90									
21	SUPPLY	I+	Positive Supply Current	.9		2			2		mA	All Channels "ON" or "OFF," V_{IN} = 0 or 2.4 V	
22		I−	Negative Supply Current	-.3		-1			-1				

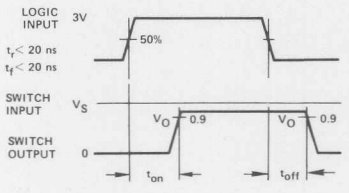
NOTES:

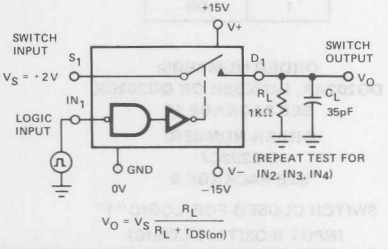
1. Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ICMC-D

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





designed for . . .

- **Low Transient Switching i.e., Sample and Hold Circuits**
- **Switching Multiple Signals such as Multiplexing Inputs**
- **High Frequency Signal Switching e.g., Computer Peripheral Equipment**
- **TTL Compatible Systems Including Microprocessor Systems**

BENEFITS

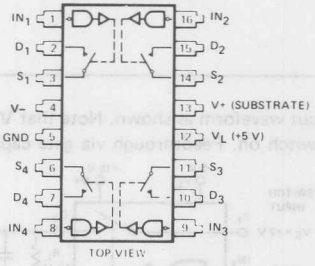
- **Environmentally Rugged**
 - Latchproof
 - Power Supply Overvoltage to 40V Max
- **Reduced Switching Error**
 - Low Charge Coupling
- **Easily Interfaced**
 - TTL, DTL and CMOS Compatible without Pull Up Resistors
- **Reduces External Component Requirements**
 - ±15 V Analog Signal Range with ±15 V Supplies
- **Reduced System Cross-Talk**
 - Break-Before-Make Switching
- **Eliminates Signal Error**
 - 0.01 nA Typical Leakage From Source Or Drain
- **Pin for Pin Compatible with**
 - Intersil IH5052, IH201
- **Low Cost**

DESCRIPTION

The DG211 designed on the Siliconix PLUS-40 CMOS process is a 4-channel single pole single throw analog switch with low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (– 15 V to 0.8 V) thw switch will be ON, and a logic "1" (2.4 V to 15 V) will turn the switch OFF. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make. Logic inputs can directly connect to op-amp output swings.

PIN CONFIGURATION

Dual-In-Line Package



LOGIC	SWITCH
0	ON
1	OFF

ORDER NUMBER:
DG211CJ
SEE PACKAGE 8

SWITCH OPEN FOR LOGIC "1" INPUT (POSITIVE LOGIC)

ABSOLUTE MAXIMUM RATINGS

V+ to V− 40 V
V_{IN} to Ground V−, V+
V_L to Ground −0.3 V, 25 V
V_S or V_D to V+ 0, −40 V
V_S or V_D to V− 0, 40 V
V+ to Ground 25 V
V− to Ground −25 V
Current, Any Terminal Except S or D 30 mA
Continuous Current, S or D 20 mA
Peak Current, S or D
(pulsed at 1 msec, 10% duty cycle max) 70 mA

Storage Temperature −65 to 125°C
Operating Temperature 0 to 70°C
Power Dissipation (Package)*
16 Pin Plastic DIP** 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

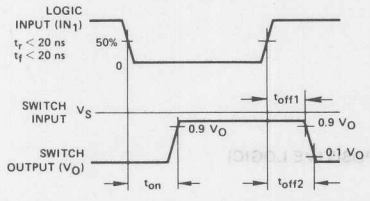
		CHARACTERISTIC		TYP[1] 25°C	MAX LIMITS C SUFFIX 25°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Gnd = 0, V_L = 5 V	
1		V_{ANALOG}	Min. Analog Signal Handling Capability	±15	±15	V		
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	105	175	Ω	V_D = 10 V	V_{IN} = 0.8 V, I_S = −1 mA
3	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	115	175	Ω	V_D = −10 V	V_{IN} = 0.8 V, I_S = −1 mA
4	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	0.01	5	nA	V_S = 14 V, V_D = −14 V	V_{IN} = 2.4 V
5	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	−0.02	−5	nA	V_S = −14 V, V_D = 14 V	V_{IN} = 2.4 V
6	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	0.01	5	nA	V_D = 14 V, V_S = −14 V	V_{IN} = 2.4 V
7	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	−0.02	−5	nA	V_D = −14 V, V_S = 14 V	V_{IN} = 2.4 V
8	SWITCH	$I_{D(on)}$[2]	Drain ON Leakage Current	0.1	5	nA	V_D = V_S = 14 V	V_{IN} = 0.8 V
9	SWITCH	$I_{D(on)}$[2]	Drain ON Leakage Current	−0.15	−5	nA	V_D = V_S = −14 V	V_{IN} = 0.8 V
10	INPUT	I_{INH}	Input Current, Input Voltage High	−0.0004	−1	μA	V_{IN} = 2.4 V	
11	INPUT	I_{INH}	Input Current, Input Voltage High	0.003	1	μA	V_{IN} = 15 V	
12	INPUT	I_{INL}	Input Current, Input Voltage Low	−0.0004	−1	μA	V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn-ON Time	460	1000	ns	V_S = 2 V, R_L = 1K Ω, C_L = 35 pF	See Switching Time Test Circuit
14	DYNAMIC	t_{off1}	Turn-OFF Time	360	500	ns	V_S = 2 V, R_L = 1K Ω, C_L = 35 pF	See Switching Time Test Circuit
15	DYNAMIC	t_{off2}	Turn-OFF Time	450		ns	V_S = 2 V, R_L = 1K Ω, C_L = 35 pF	See Switching Time Test Circuit
16	DYNAMIC	$C_{S(off)}$	Source OFF Capacitance	5		pF	V_S = 0, V_{IN} = 5 V	f = 1 MHz
17	DYNAMIC	$C_{D(off)}$	Drain OFF Capacitance	5		pF	V_D = 0, V_{IN} = 5 V	f = 1 MHz
18	DYNAMIC	$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	16		pF	V_D = V_S = 0, V_{IN} = 0	f = 1 MHz
19	DYNAMIC	OFF Isolation[3]		70		dB	V_{IN} = 5 V, R_L = 1K Ω, C_L = 15 pF, V_S = 1 VRMS, f = 100 kHz	
20	DYNAMIC	Interchannel Crosstalk Isolation		90		dB	V_{IN} = 5 V, R_L = 1K Ω, C_L = 15 pF, V_S = 1 VRMS, f = 100 kHz	
21	SUP	I+	Positive Supply Current	0.35	0.48	mA	V_{IN} = 0 or 2.4 V	
22	SUP	I−	Negative Supply Current	0.30	0.48	mA	V_{IN} = 0 or 2.4 V	
23	SUP	I_L	Logic Supply Current	0.5	1.2	mA	V_{IN} = 0 or 2.4 V	

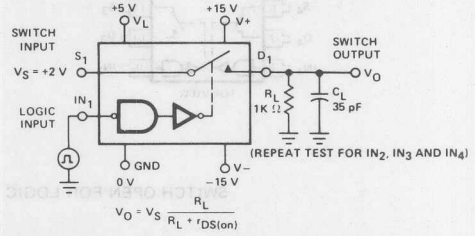
1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into ON switch.
3. OFF Isolation = $20 \log \frac{|V_S|}{|V_D|}$, V_S = input to OFF switch, V_D = output.

ICMC-A

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

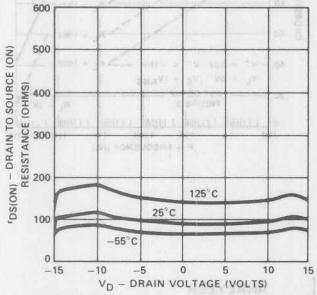




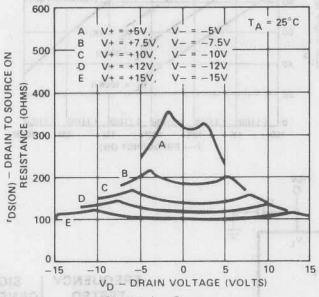
TYPICAL CHARACTERISTICS

The electrical characteristic table guarantees the DG211 for operation at ±15 V, ±10%; however, functional operation occurs over the designed range of ±5 V to ±20 V power supplies. These characteristic graphs show the effect of device parameters over several parameter permutations including power supply variations. These graphs are for design aid only and are not subject to production testing.

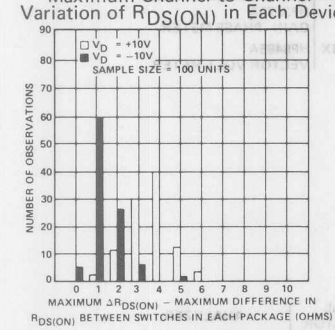
$r_{DS(ON)}$ vs V_D Temperature



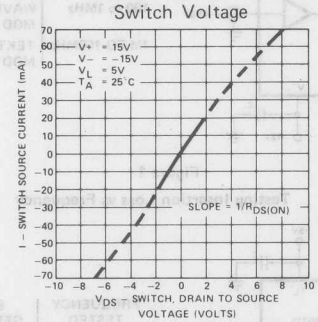
$r_{DS(ON)}$ vs V_D and Power Supply Voltage



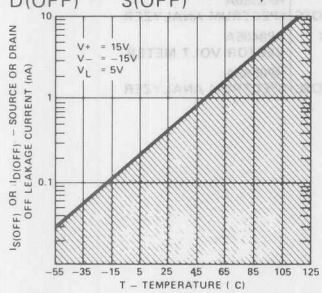
Maximum Channel to Channel Variation of $R_{DS(ON)}$ in Each Device



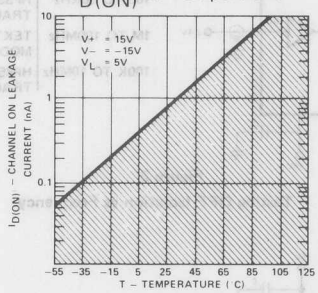
Switch Current vs Switch Voltage



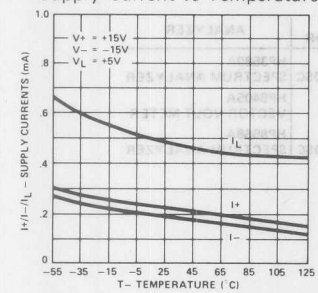
$I_{D(OFF)}$ or $I_{S(OFF)}$ vs Temperature*



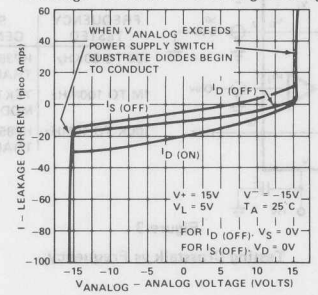
$I_{D(ON)}$ vs Temperature*



Supply Current vs Temperature

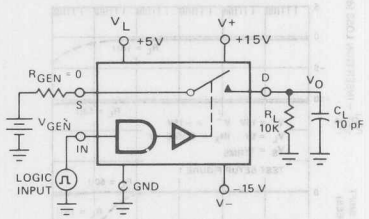


Leakage Current vs Analog Voltage

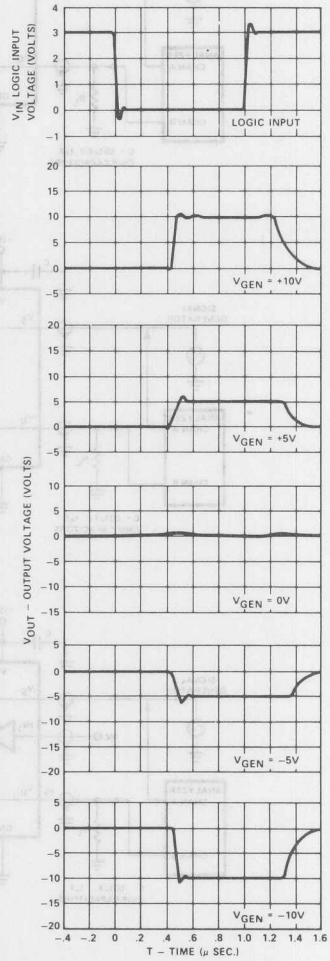


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

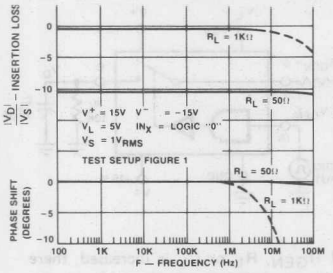
Typical delay, rise, fall, settling times, and switching transients in this circuit.

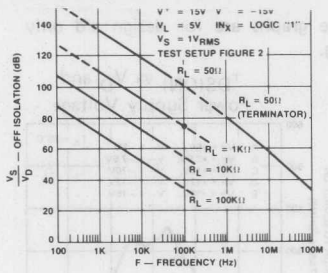


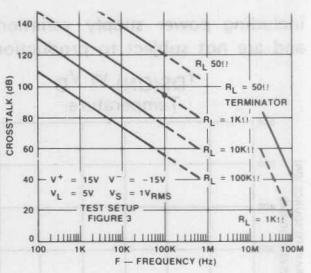
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater t_{on} spikes.

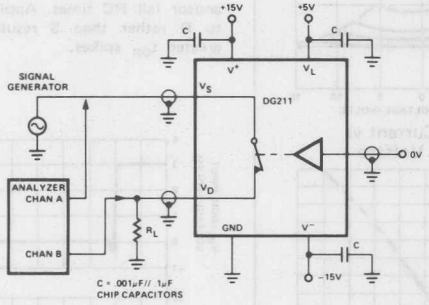


NOTE: Turn-off time is primarily limited here by the RC time constant (50ns) of the load.





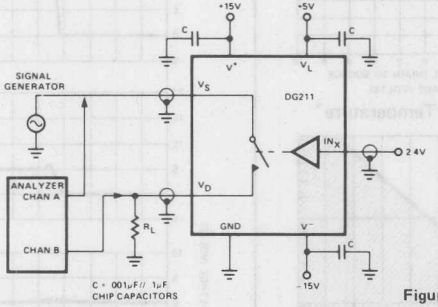




FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 to 1MHz	WAVETEK MOD 142	HP3575A GAIN–PHASE METER
1M TO 100MHz	TEKTRONIX MOD 191	HP8405A VECTOR VOLT METER

Figure 1

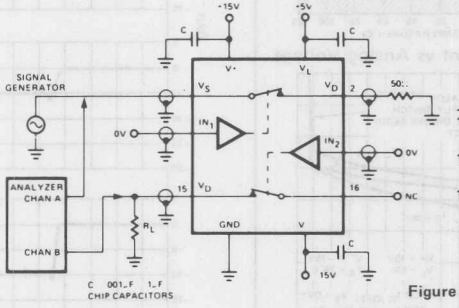
Testing Insertion Loss vs Frequency



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 TO 50KHz	HP3580A TRACKING OSC	HP3580A SPECTRUM ANALYZER
1M TO 100MHz	TEKTRONIX MOD 191	HP8405A VECTOR VOLT METER
100K TO 10MHz	HP8568A TRACKING OSC	HP8568A SPECTRUM ANALYZER

Figure 2

Testing OFF Isolation vs Frequency

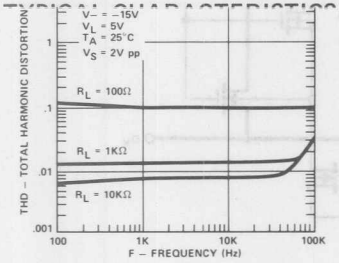


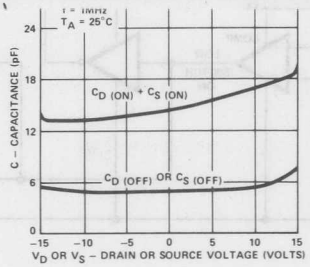
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 TO 50KHz	HP3580A TRACKING OSC	HP3580A SPECTRUM ANALYZER
1M TO 100MHz	TEKTRONIX MOD 191	HP8405A VECTOR VOLT METER
100K TO 10MHz	HP8568A TRACKING OSC	HP8568A SPECTRUM ANALYZER

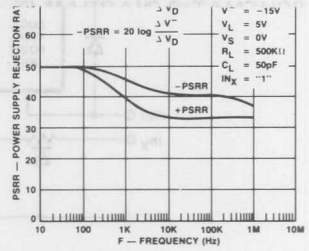
Figure 3

Testing Crosstalk vs Frequency

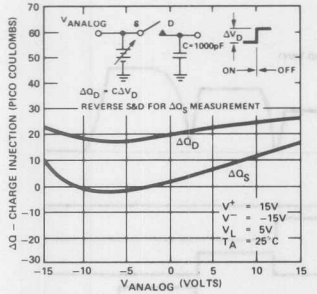
The data plotted in the frequency response graphs are measured in a special coax test fixture. Each lead of the IC package fits into the center conductor of a solid 50 ohm coax. The fixture eliminates stray capacitance normally encountered in printed circuit (PC) board layouts and sockets. The OFF isolation versus frequency degrades from the values shown with careless PC board layout. The best layout techniques include good ground planes, guardtraces between signal paths and bypassed power supplies.



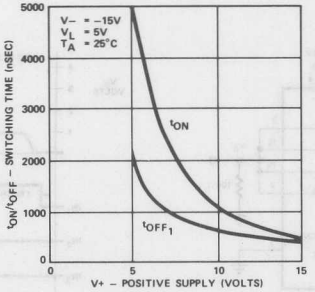




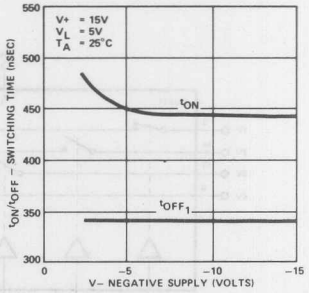
Charge Injection vs Analog Voltage



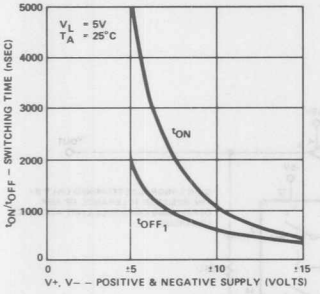
Switching Time vs Positive Supply Voltage



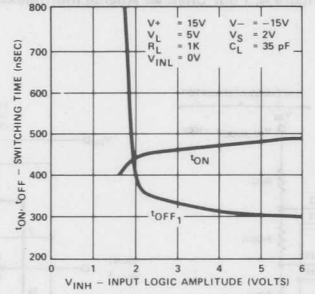
Switching Time vs Negative Supply Voltage



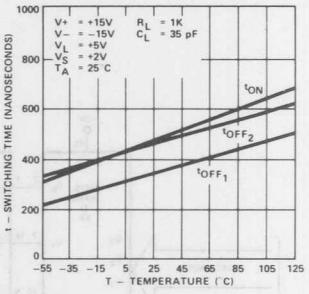
Switching Time vs Positive & Negative Supply Voltage



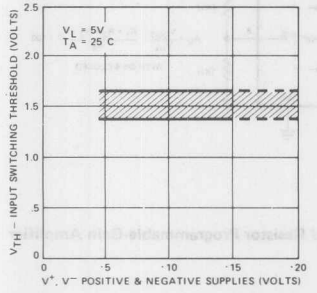
Switching Time vs Input Logic Amplitude



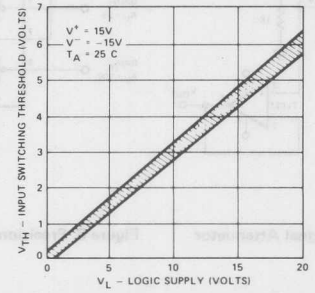
Switching Time vs Temperature



Input Switching Threshold vs V+ & V− Supply Voltages



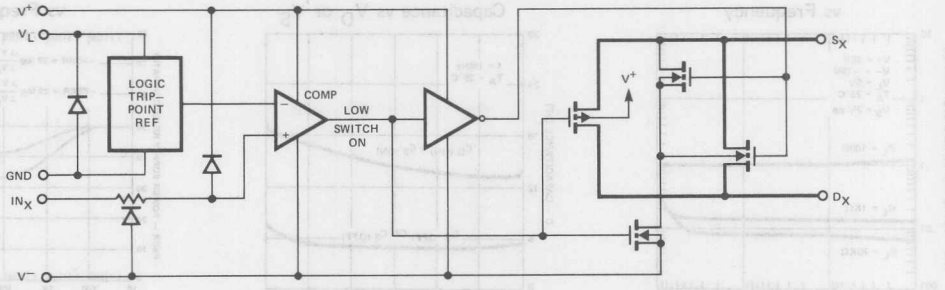
Input Switching Threshold vs Logic Supply Voltage



Some applications of the DG211 will find the logic control inputs (IN_X) driven from the output of comparators or op-amps with nearly plus to minus 15 volt transitions. In these applications the user can shift the input logic transition voltage from the normal 1.6 V of TTL to zero volts by connecting the V_L pin to the GND pin. In this mode of operation the input offset voltage between IN_X and V_L (= GND) measure less than ±500mV.

V_L=5V presets the input threshold voltage for TTL logic compatibility. Improved noise immunity for CMOS logic compatibility results by connecting V_L to the V_{DD} terminal of the CMOS logic.

SCHEMATIC DIAGRAM (Typical Channel)



APPLICATIONS

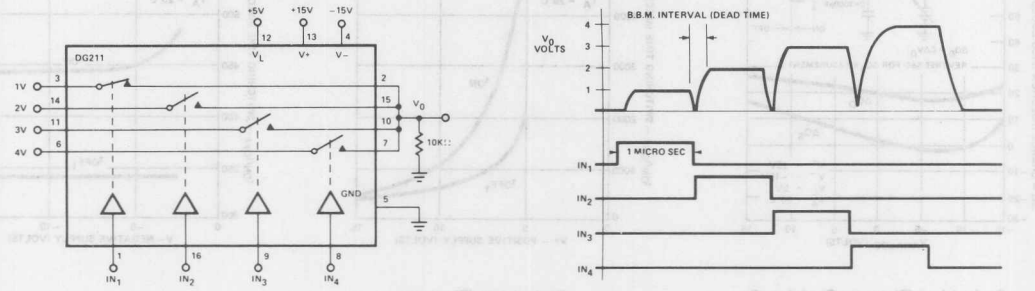


Figure 4. Four Channel Analog Multiplexer

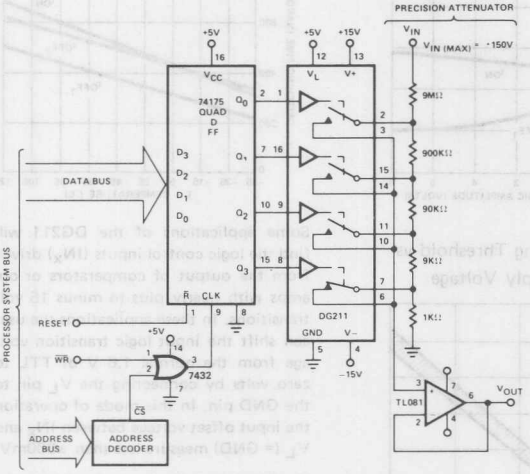


Figure 5. Microprocessor Controlled Analog Signal Attenuator

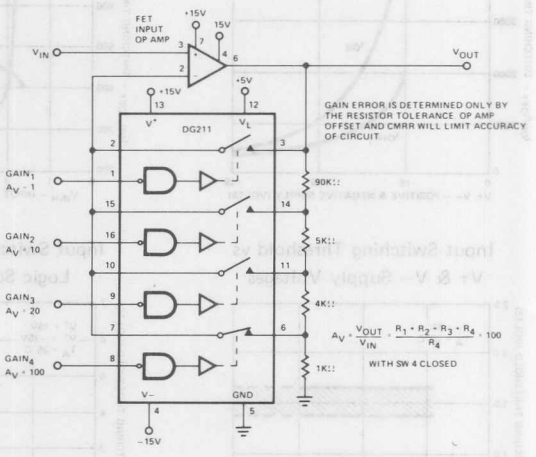


Figure 6. Precision-Weighted Resistor Programmable-Gain Amplifier

Quad Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Low Transient Switching i.e., Sample and Hold Circuits**
- **Switching Multiple Signals such as Multiplexing Inputs**
- **High Frequency Signal Switching e.g., Computer Peripheral Equipment**
- **TTL Compatible Systems Including Microprocessor Systems**

BENEFITS

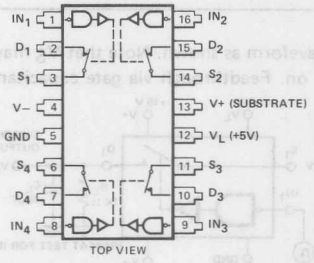
- **Environmentally Rugged**
 - Latchproof
 - 40 V Power Supply Max Rating
- **Reduced Switching Error**
 - Low Charge Coupling
- **Easily Interfaced**
 - TTL, DTL and CMOS Compatible without Pull Up Resistors
- **Reduces External Component Requirements**
 - ±15 V Analog Signal Range with ±15 V Supplies
- **Reduced System Cross-Talk**
 - Break-Before-Make Switching
- **Eliminates Signal Error**
 - 0.01 nA Typical Leakage From Source or Drain
- **Pin for Pin Compatible with**
 - Intersil IH5053,IH202
- **Opposite Logic Control of DG211**
- **Low Cost**

DESCRIPTION

The DG212 designed on the Siliconix PLUS-40 CMOS process is a 4-channel single pole single throw analog switch with low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (–15 V to 0.8 V) the switch will be OFF, and a logic "1" (2.4 V to 15 V) will turn the switch ON. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make. Logic inputs can directly connect to op-amp output swings.

PIN CONFIGURATION

Dual-In-Line Package



LOGIC	SWITCH
0	OFF
1	ON

ORDER NUMBER:
DG212CJ
SEE PACKAGE 8

SWITCH CLOSED FOR LOGIC "1" INPUT (POSITIVE LOGIC)

V_S or V_D to V+	0, −40 V
V_S or V_D to V−	0, 40 V
V+ to Ground	25 V
V− to Ground	−25 V
Current, Any Terminal Except S or D	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (pulsed at 1 msec, 10% duty cycle max)	70 mA

16 Pin Plastic DIP 470 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

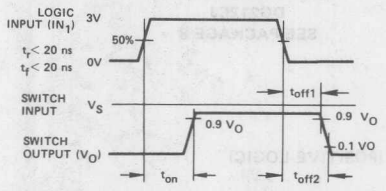
		CHARACTERISTIC		TYP[1] 25°C	MAX LIMITS C SUFFIX 25°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Gnd = 0, V_L = 5 V	
1		V_{ANALOG}	Min. Analog Signal Handling Capability	±15	±15	V		
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	105	175	Ω	V_D = 10 V	V_{IN} = 2.4 V, I_S = −1 mA
3	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	115	175	Ω	V_D = −10 V	V_{IN} = 2.4 V, I_S = −1 mA
4	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	0.01	5	nA	V_S = 14 V, V_D = −14 V	V_{IN} = 0.8 V
5	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	−0.02	−5	nA	V_S = −14 V, V_D = 14 V	V_{IN} = 0.8 V
6	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	0.01	5	nA	V_D = 14 V, V_S = −14 V	V_{IN} = 0.8 V
7	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	−0.02	−5	nA	V_D = −14 V, V_S = 14 V	V_{IN} = 0.8 V
8	SWITCH	$I_{D(on)}$[2]	Drain ON Leakage Current	0.1	5	nA	V_D = V_S = 14 V	V_{IN} = 2.4 V
9	SWITCH	$I_{D(on)}$[2]	Drain ON Leakage Current	−0.15	−5	nA	V_D = V_S = −14 V	V_{IN} = 2.4 V
10	INPUT	I_{INH}	Input Current, Input Voltage High	−0.0004	−1	μA	V_{IN} = 2.4 V	
11	INPUT	I_{INH}	Input Current, Input Voltage High	0.003	1	μA	V_{IN} = 15 V	
12	INPUT	I_{INL}	Input Current, Input Voltage Low	−0.0004	−1	μA	V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn-ON Time	460	1000	ns	V_S = 2 V, R_L = 1K Ω, C_L = 35 pF	See Switching Time Test Circuit
14	DYNAMIC	t_{off1}	Turn-OFF Time	360	500	ns	V_S = 2 V, R_L = 1K Ω, C_L = 35 pF	See Switching Time Test Circuit
15	DYNAMIC	t_{off2}	Turn-OFF Time	450		ns	V_S = 2 V, R_L = 1K Ω, C_L = 35 pF	See Switching Time Test Circuit
16	DYNAMIC	$C_{S(off)}$	Source OFF Capacitance	5		pF	V_S = 0, V_{IN} = 0 V	f = 1 MHz
17	DYNAMIC	$C_{D(off)}$	Drain OFF Capacitance	5		pF	V_D = 0, V_{IN} = 0 V	f = 1 MHz
18	DYNAMIC	$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	16		pF	V_D = V_S = 0, V_{IN} = 5 V	f = 1 MHz
19	DYNAMIC	OFF Isolation[3]		70		dB	V_{IN} = 0 V, R_L = 1K Ω, C_L = 15 pF, V_S = 1 VRMS, f = 100 kHz	
20	DYNAMIC	Interchannel Crosstalk Isolation		90		dB	V_{IN} = 0 V, R_L = 1K Ω, C_L = 15 pF, V_S = 1 VRMS, f = 100 kHz	
21	SUP	I+	Positive Supply Current	0.35	0.48	mA	V_{IN} = 0 or 2.4 V	
22	SUP	I−	Negative Supply Current	0.30	0.48	mA	V_{IN} = 0 or 2.4 V	
23	SUP	I_L	Logic Supply Current	0.5	1.2	mA	V_{IN} = 0 or 2.4 V	

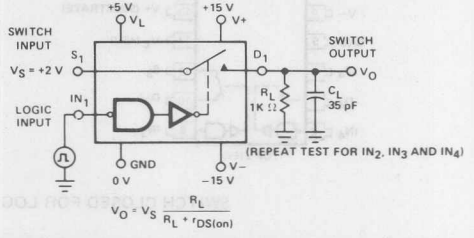
ICMC-C

1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into ON switch.
3. OFF Isolation = $20 \log \frac{|V_S|}{|V_D|}$, V_S = input to OFF switch, V_D = output.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





designed for . . .

- **Programmable Gain Amplifiers**
- **Analog Multiplexing**
- **Servo Control Switching**

BENEFITS

- **Transient Suppression**
 - Make-Before-Break Switch Operation
- **Environmentally Rugged**
 - 40V Power Supply Rating
 - Static Protected Logic Inputs
 - Latchproof
- **Easily Interfaced**
 - TTL and CMOS Compatible without Pull Up Resistors
- **Reduces External Component Requirements**
 - Full Rail to Rail Analog Signal Range
 - No Diode Protection Required Between V_L and V+ for Power Supply Sequencing
- **Pin for Pin Compatible with**
 - Intersil IH5043
 - Harris HI5043
 - Siliconix DG5043, DG191, DG390

DESCRIPTION

The DG243 designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 50 ohms contact resistance and very high OFF resistance. True switch action takes place over the full analog signal range of ±15 volts, with Make-Before-Break operation improving transient response in programmable gain amplifiers.

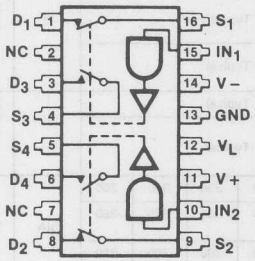
PIN CONFIGURATIONS

DUAL SPDT

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

ALL SWITCHES SHOWN IN THE LOGIC "1" SWITCH STATE

Dual-In-Line Package

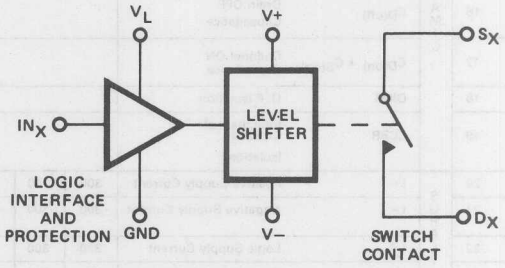


TOP VIEW

ORDER NUMBER:
DG243AK or DG243CK
SEE PACKAGE 10

DG243CJ
SEE PACKAGE 8

FUNCTIONAL DIAGRAM (typical channel)



ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–

V+ 44 V

V_L (GND –0.3 V) to 44 V

GND 25 V

Digital inputs[5] V_S, V_D –2 V to (V^+ +2 V) or 30 mA, whichever occurs first.

Current, Any Terminal Except S or D 30 mA

Continuous Current, S or D 30 mA

Peak Current, S or D

(pulsed at 1 msec, 10% duty cycle max) 100 mA

Storage Temperature (A Suffix) -65 to 150°C

(C Suffix) -65 to 125°C

Operating Temperature (A Suffix) -55 to 125°C

(C Suffix) 0 to 70°C

Power Dissipation*

Metal Can and Plastic DIP** 450 mW

16 Pin DIP**** 900 mW

Flat Pack***** 900 mW

*All leads welded or soldered to PC board.

**Derate 6 mW/°C above 75°C

****Derate 12 mW/°C above 75°C

*****Derate 10 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25° C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTICS		MAX LIMITS A SUFFIX –55°C	A SUFFIX 25°C	A SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS V+ = 15V, V– = –15V, V_L = 5V, GND = 0V	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability		±15	±15		±15	±15	V		
2	SWITCH	$r_{DS(on)}$[3]	Drain Source ON Resistance	50	50	75	50	50	75	Ω	V_D = 10 V, I_S = –10 mA	Note 1
3				50	50	75	50	50	75		V_D = –10 V, I_S = –10 mA	
4		$I_{S(off)}$[3]	Source OFF Leakage Current		1	100		1	100	nA	V_S =14 V, V_D = – 14 V	
5					–1	–100		–1	–100		V_S = –14 V, V_D = 14 V	
6		$I_{D(off)}$[3]	Drain OFF Leakage Current		1	100		1	100		V_S = –14 V, V_D = 14 V	
7					–1	–100		–1	–100		V_S = 14 V, V_D = – 14 V	
8		$I_{D(on)}$[3]	Drain ON Leakage Current		2	200		2	200		V_S = V_D = 14 V	
9					–2	–200		–2	–200		V_S = V_D = –14 V	
10	INPUT	I_{INH}[3]	Input Current Input Voltage High		±1	±1		±1	±1	µA	V_{INH} = 2.0 V	
11		I_{INL}[3]	Input Current Input Voltage Low		±1	±1		±1	±1		V_{INL} = 0.8 V	
12	DYNAMIC	t_{on}[4]	Turn-ON Time		500			700		ns	V_S = ±10 V, R_L = 1KΩ	Note 2
13		t_{off}[4]	Turn-OFF Time		1000			1200			C_L = 35 pF	
14		Q	Charge Injection	60 Typical						pC	C_L = 1000pF, R_{GEN} = 0Ω, V_{GEN} = 0 V	
15		$C_{S(off)}$	Source OFF Capacitance	15 Typical						pF	V_S = V_D = 0 V, f = 1 MHz	Note 1
16		$C_{D(off)}$	Drain OFF Capacitance	17 Typical								
17		$C_{D(on)}$ + $C_{S(on)}$	Channel ON Capacitance	45 Typical								
18		OIRR	OFF Isolation	75 Typical						dB	Z_L = 75Ω, V_S = 2 Vpp, f = 1 MHz	
19		CCRR	Interchannel Crosstalk Isolation	89 Typical								
20	SUPPLY	I_+[3]	Positive Supply Current	300	300	300	300	300	300	µA	V_{IN} = 0 V or 2.4 V	
21		I_-[3]	Negative Supply Current	–300	–300	–300	–300	–300	–300			
22		I_L[3]	Logic Supply Current	300	300	300	300	300	300			
23		I_{GND}	Ground Supply Current	–300	–300	–300	–300	–300	–300			

ICMK-C

NOTES:

1: V_{IN} = Input voltage to perform proper function.
For Logic "1" — V_{INH} = 2.0 V
For Logic "0" — V_{INL} = 0.8 V

2: See Switching Time Test Circuit.

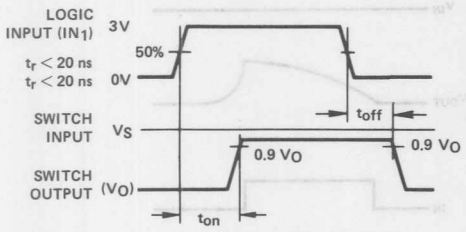
3: Limits of these paramaters are tested 100% at 25 °C and 125°C for "/883" devices.

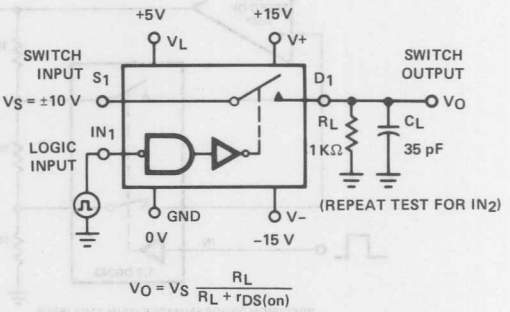
4: For "/883" devices these parameters are 100% tested at 25°C.

5: Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

SWITCHING TIME TEST CIRCUIT

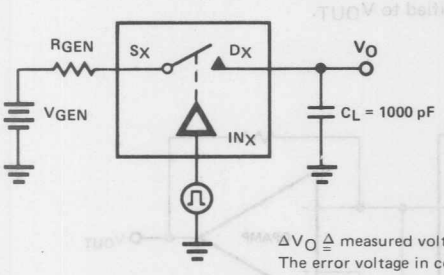
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

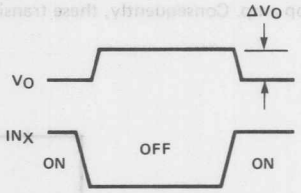




Note: Logic input waveform is inverted for switches that have the opposite logic sense control.

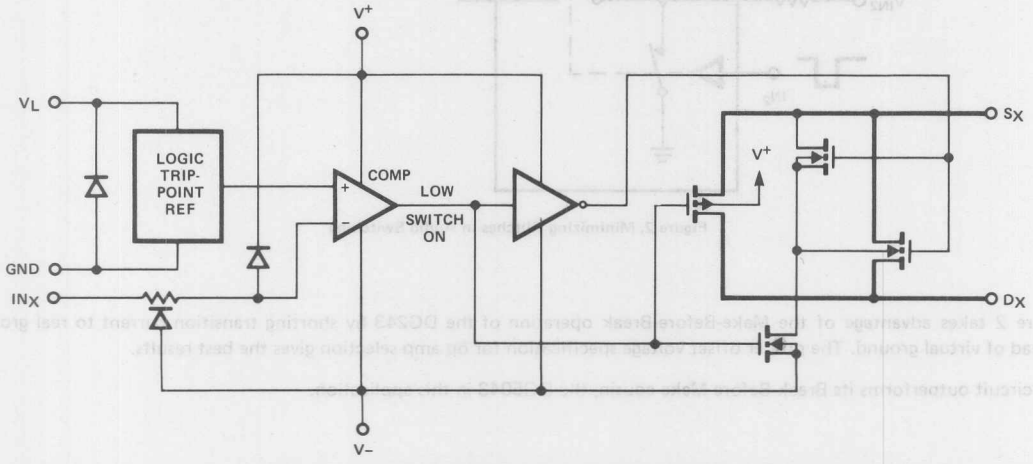
CHARGE INJECTION TEST CIRCUIT





$\Delta V_O \triangleq$ measured voltage error due to charge injection.
The error voltage in coulombs is $\Delta Q = C_L \times \Delta V_O$.

SCHEMATIC DIAGRAM (typical channel)



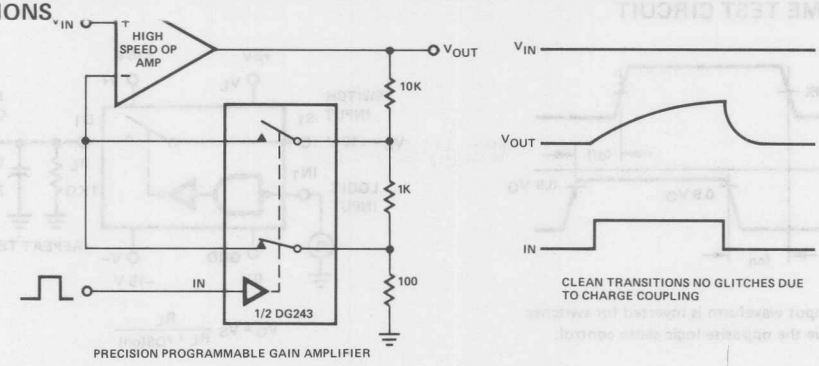


Figure 1. Improving Transient Response in Programmable Gain Amplifiers. "Getting Rid of Glitches".

Figure 1 shows a minimum amount of glitching during changes of gain states. The relatively low impedance of the gain setting resistors 10K, 1K, 100Ω shunt the injected charge to ground minimizing transient effects ocurring at the inverting input of the op amp. Consequently, these transients are not amplified to V_{OUT}.

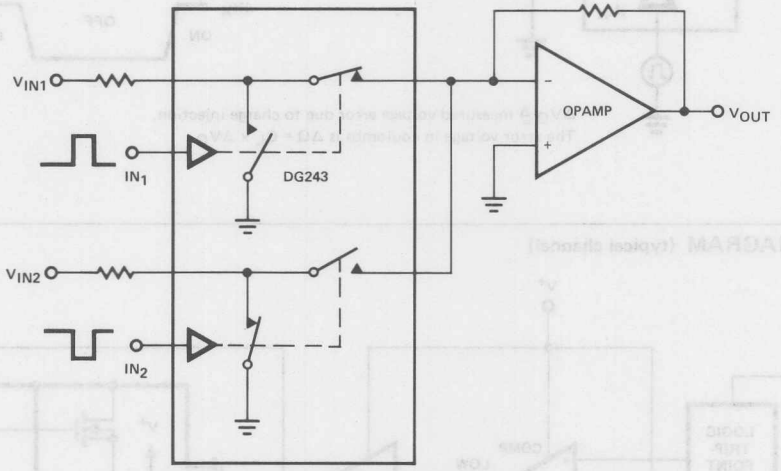


Figure 2. Minimizing Glitches in Audio Switching

Figure 2 takes advantage of the Make-Before-Break operation of the DG243 by shorting transition current to real ground instead of virtual ground. The proper offset voltage specification for op amp selection gives the best results.

The circuit outperforms its Break-Before-Make cousin, the DG5043 in this application.

designed for...

- **Low Error Sample and Hold Circuits**
- **100 MHz Signal Switching with High OFF Isolation**
- **Presettable Integrators with Minimum Offset Error**
- **Low Distortion Click Free Audio Switching**

BENEFITS

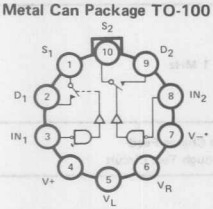
- **Minimum Signal Errors**
 - Low Charge Feedthrough 7 Picocoulombs Typical
 - Low "r_{on} x $I_{D(OFF)}$ Error Factor
 - Low Leakage Less Than 10 Picoamps Typical
 - Low Distortion – Constant ON Resistance
- **Easily Interfaced**
 - TTL and CMOS Logic Compatibility Over Full Temperature Range
- **Compact Circuit Layouts**
 - Several Form Factors Available in Single Packages (eg. 2XSPST, SPDT, 2XSPDT, 2XDPST)

DESCRIPTION

The DG281 series incorporates N-channel junction-type field-effect transistors (JFETs) designed to function as electronic switches. Level-shifting drivers enable TTL or CMOS outputs to control the ON-OFF state of each switch. The driver is designed to provide break-before-make action when switching from one channel to another. The low switch capacitance results in a minimal amount of charge-feedthrough into the analog signal path. In the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block voltages up to 22.5 V peak-to-peak.

PIN CONFIGURATIONS (Top View)

Metal Can Package TO-100

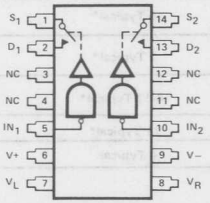


DUAL SPST

LOGIC	SW 1 & 2
0	ON
1	OFF

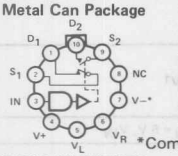
ORDER NUMBERS:
DG281AA OR DG281BA
SEE PACKAGE 2

Dual-In-Line Package TO-116



ORDER NUMBERS:
DG281AP OR DG281BP
SEE PACKAGE 11

Metal Can Package



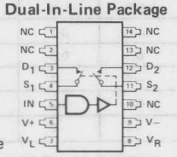
SPDT

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*Common to Substrate and Case

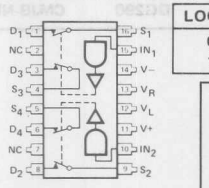
ORDER NUMBERS:
DG287AA OR DG287BA
SEE PACKAGE 2

Dual-In-Line Package



ORDER NUMBERS:
DG287AP OR DG287BP
SEE PACKAGE 11

Dual-In-Line Package



ORDER NUMBERS:
DG284AP OR DG284BP
SEE PACKAGE 12

DUAL DPST

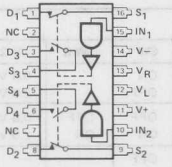
LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

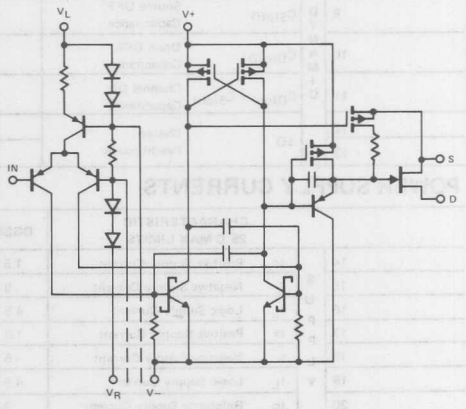
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

Dual-In- Line Package



ORDER NUMBERS:
DG290AP OR DG290BP
SEE PACKAGE 12

SCHEMATIC DIAGRAM (Typical Channel)



APPLICATION HINTS*

V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S Analog Voltage Range (V)
+15**	-15	+5	Gnd	2.0/0.8	-7.5 to +15
+10	-20	+5	Gnd	2.0/0.8	-12.5 to +10
+12	-12	+5	Gnd	2.0/0.8	-4.5 to +12

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Parameter Chart based on V+ = +15 V, V– = –15 V, V_L = 5 V, V_R = Gnd.

ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_D	33 V
V_D to V−	33 V
V_D to V_S	±22 V
V_L to V−	36 V
V_L to V_{IN}	8 V
V_L to V_R	8 V
V_{IN} to V_R	8 V
V_R to V−	27 V
V_R to V_{IN}	8 V
Current (Any Terminal)	20 mA
Storage Temperature	−65 to +150°C
Operating Temperature (A Suffix)	−55 to +125°C
(B Suffix)	−20 to +85°C

Power Dissipation*

Metal Can**	450 mW
14 Pin DIP***	825 mW
16 Pin DIP****	900 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.
****Derate 12 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS DG281A, DG284A DG287A, DG290A −55°C	25°C	125°C	DG281B, DG284B DG287B, DG290B −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, V_L = 5 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance		300	500		300	500	Ω	V_D = −7.5 V	I_S = −1 mA††
2	SWITCH	$I_{S(off)}$	Source OFF Leakage Current		0.5	100		2	100	nA	V_S = 7.5 V, V_D = −7.5 V	††
3	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current		0.2	100		1	100	nA	V_D = 7.5 V, V_S = −7.5 V	††
4	SWITCH	$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−200		−10	−200	nA	V_D = V_S = −7.5 V	††
5	IN	I_{INL}	Input Current, Input Voltage Low	−250	−250	−250	−250	−250	−250	µA	V_{IN} = 0	
6	IN	I_{INH}	Input Current, Input Voltage High		10	20		10	20	µA	V_{IN} = 5 V	
7		t_{on}	Turn-ON Time		150			180		ns	See Switching Time Test Circuit	
8		t_{off}	Turn-OFF Time		130			150		ns	See Switching Time Test Circuit	
9	DYNAMIC	$C_{S(off)}$	Source OFF Capacitance	6 Typical*						pF	V_S = −5 V, I_D = 0	f = 1 MHz
10	DYNAMIC	$C_{D(off)}$	Drain OFF Capacitance	2 Typical*						pF	V_D = −5 V, I_S = 0	f = 1 MHz
11	DYNAMIC	$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	14-17 Typical*						pF	V_D = V_S = 0	f = 1 MHz
12	DYNAMIC	ΔQ	Charge-Feedthrough	11 Typical*						pC	V_S = 7.5 V	See Charge-Feedthrough Test Circuit
13	DYNAMIC	ΔQ	Charge-Feedthrough	4 Typical						pC	V_S = −7.5 V	See Charge-Feedthrough Test Circuit

POWER SUPPLY CURRENTS

		CHARACTERISTIC 25°C MAX LIMITS		DG281	DG284	DG287	DG290	UNIT	TEST CONDITIONS
14	SUPPLY	I_+	Positive Supply Current	1.5	3	0.8	1.5	mA	V_{IN} = 0†
15	SUPPLY	I_-	Negative Supply Current	−5	−5.5	−3	−5	mA	V_{IN} = 0†
16	SUPPLY	I_L	Logic Supply Current	4.5	4.5	3.2	4.5	mA	V_{IN} = 0†
17	SUPPLY	I_+	Positive Supply Current	1.5	0.1	0.8	1.5	mA	V_{IN} = 5 V†
18	SUPPLY	I_-	Negative Supply Current	−5	−4	−3	−5	mA	V_{IN} = 5 V†
19	SUPPLY	I_L	Logic Supply Current	4.5	4.5	3.2	4.5	mA	V_{IN} = 5 V†
20	SUPPLY	I_R	Reference Supply Current	−2	−2	−2	−2	mA	Both V_{IN} = 5 V, V_{IN} = 0

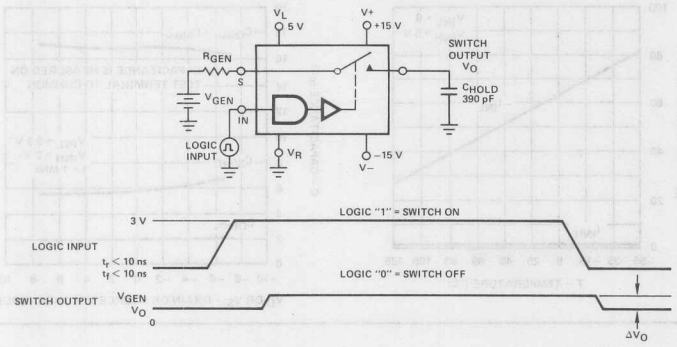
†If driver has two channels, both are active.
*Typical values are to DESIGN AID ONLY, not guaranteed and not subject to production testing.
††Switch being tested ON or OFF as indicated. Input Logic Low 0.8 V.
Input Logic High 2V.

DG281	CMJB-NH
DG284	CMJA-NH
DG287	CMJC-NH
DG290	CMJB-NH

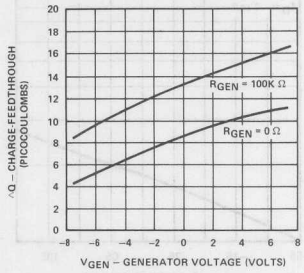
TRUTH TABLE

DEVICE	IN 1	SW 1	SW 3	IN 2	SW 2	SW 4
DG281	0.8 V	ON	–	0.8 V	ON	–
	2.0 V	OFF	–	2.0 V	OFF	–
DG284	0.8 V	OFF	OFF	0.8 V	OFF	OFF
	2.0 V	ON	ON	2.0 V	ON	ON
DG287	0.8 V	OFF	–	–	ON	–
	2.0 V	ON	–	–	OFF	–
DG290	0.8 V	OFF	ON	0.8 V	OFF	ON
	2.0 V	ON	OFF	2.0 V	ON	OFF

CHARGE INJECTION TEST CIRCUIT



Charge Feedthrough vs R_{GEN} and V_{GEN}

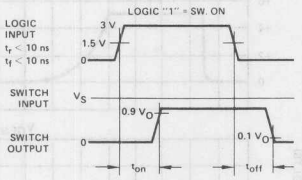


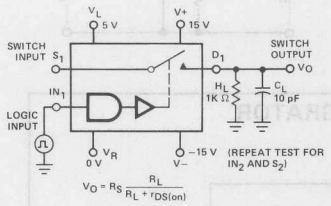
ΔV_O = ERROR VOLTAGE GENERATED ACROSS CAPACITOR

ΔQ = CHARGE INJECTED BY SWITCH DURING TURN-OFF = $\Delta V_O \times C_{HOLD}$

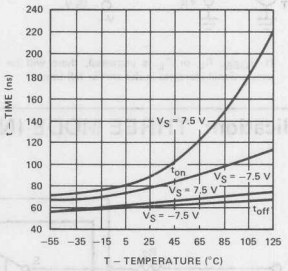
SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



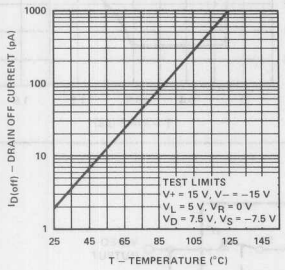


Switching Time vs V_S and Temperature

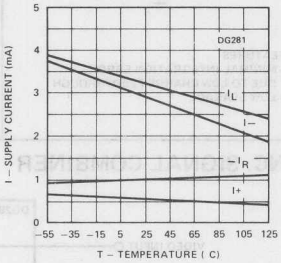


TYPICAL PERFORMANCE CURVES

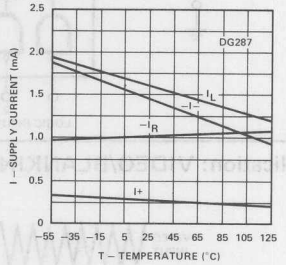
$I_{D(off)}$ vs. Temperature



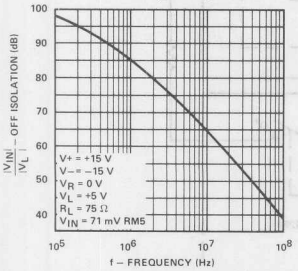
Supply Current vs Temperature



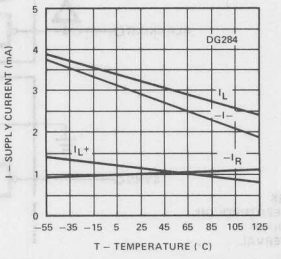
Supply Current vs Temperature



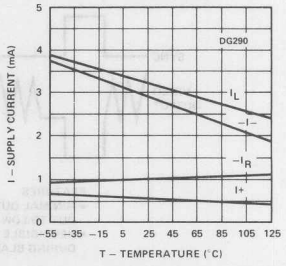
"OFF" Isolation vs Frequency



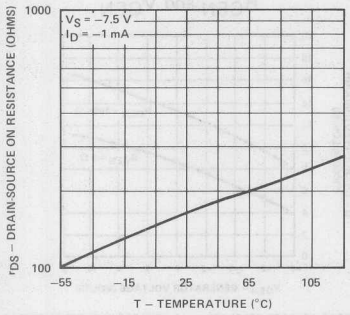
Supply Current vs Temperature



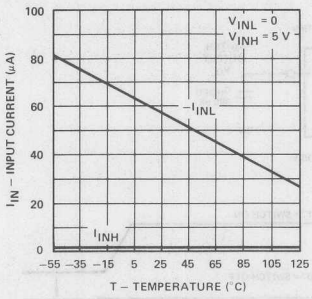
Supply Current vs Temperature



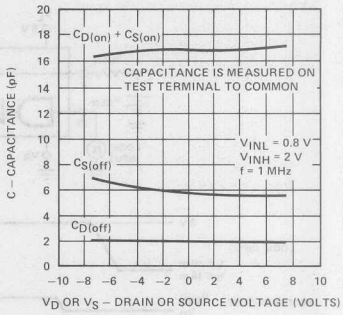
$r_{DS(on)}$ vs Temperature



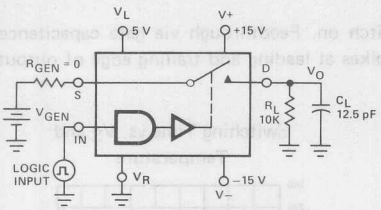
I_{IN} vs V_{IN} and Temperature



Capacitance vs V_D or V_S

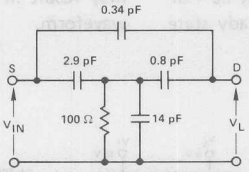


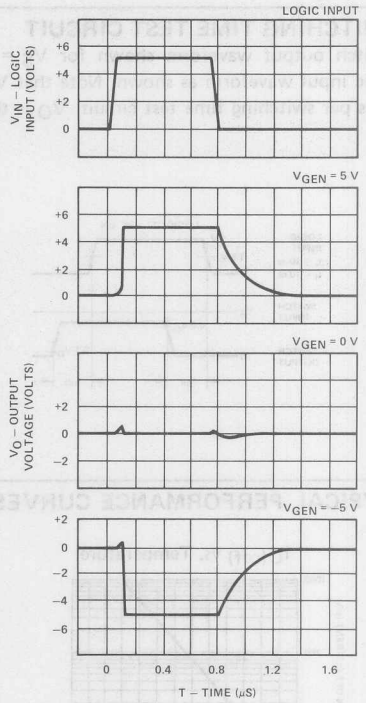
TYPICAL SWITCHING TRANSIENTS



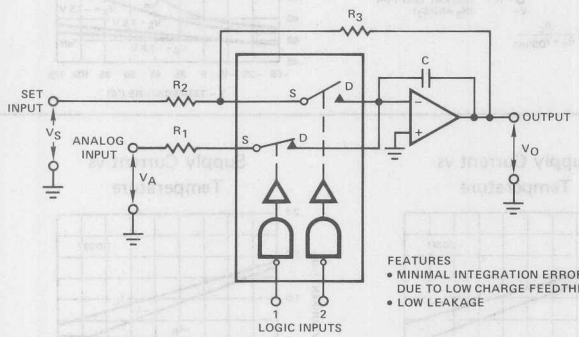
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall times.

Equivalent "OFF" Circuit



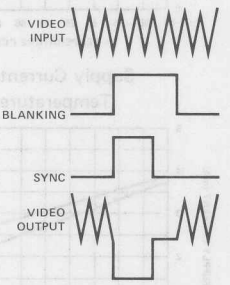


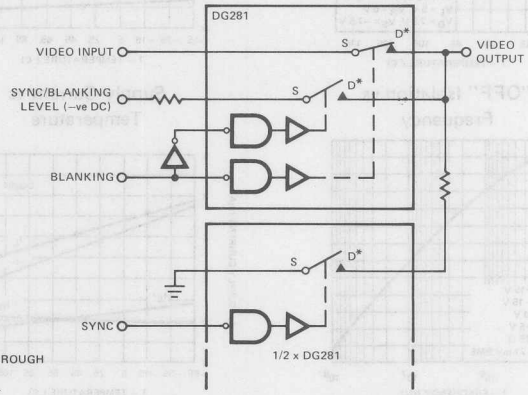
Application: THREE MODE INTEGRATOR



FEATURES
- MINIMAL INTEGRATION ERROR DUE TO LOW CHARGE FEEDTHROUGH
- LOW LEAKAGE

Application: VIDEO/BLANKING/SYNC. SIGNAL COMBINER





FEATURES
- MINIMAL OUTPUT SPIKES DUE TO LOW CHARGE FEEDTHROUGH
- NEGLIGIBLE FEEDTHROUGH DURING BLANKING INTERVAL

designed for . . .

- **Portable, Battery Operated Circuits**
- **Low Leakage Switching i.e. Sample and Hold Circuits**
- **Communication Systems**
- **Low Level Switching Circuits**
- **Fast Switching Circuits such as Multiplexers**
- **Standard Linear Dual Supply Voltages or Single Supply Systems**

BENEFITS

- **Environmentally Rugged**
 - Latchproof CMOS
- **Low Standby Power**
 - 0.06 μW Typical
- **Minimizes Signal Error**
 - 0.1 nA Typical Leakage
- **Low Operating Power**
 - 0.06 μW Typical for DG304-307
- **Reduced Voltage Drop Across Switch in ON Condition**
 - $r_{ds(on)} < 50\ \Omega$
- **Minimizes Switching Time**
 - Typ t_{on} & $t_{off} < 180$ ns
- **Minimizes System Power Requirements**
 - Single Supply Operation Capabilities
- **Easily Interfaced**
 - TTL, DTL and CMOS Input Compatible
- **Reduces External Component Requirements**
 - Logic Input Overvoltage Protection

DESCRIPTION

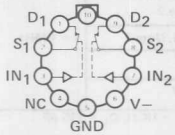
The DG300 through DG307 switch family features four switching functions using CMOS technology for low and nearly constant ON resistance (less than 50 Ω) over the full analog signal range. In the ON condition the switches will conduct current in either direction with no offset voltage. With low power dissipation, (a few milliwatts for the DG300-303, a few hundred microwatts for the DG304-307), this series of switches becomes an ideal candidate for battery-powered or remote switching applications. The switching speed is among the fastest available with the low quiescent power dissipation. In the OFF condition, the switches will block voltages up to 30 V peak-to-peak. A logic input driver controls the ON/OFF state of the switches. (See the "Pin Configuration" for switch status with a logic "1" input.) The DG300-303 switches are TTL and CMOS input compatible and have a logic "0" state with an input less than 0.8 V and a logic "1" state with an input greater than 4.0 V. A pull-up resistor should be added for totem pole TTL outputs. The DG304-307 switches are CMOS input compatible and have a logic "0" state with an input less than 3.5 V and a logic "1" state with an input greater than 11 V (for 15 V positive supply). The logic inputs are protected against overvoltage up to 18 V above and 36 V below the positive supply. The combination of low cost, low power, low resistance and fast speed optimizes system design.

PIN CONFIGURATIONS

DUAL SPST DG300 or DG304

Metal Can Package

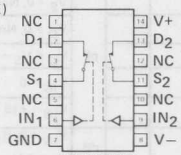
V+ (SUBSTRATE AND CASE)



TOP VIEW

ORDER NUMBERS:
DG300AA OR DG300BA
DG304AA OR DG304BA
SEE PACKAGE 2

Dual-In-Line and Flat Package



TOP VIEW

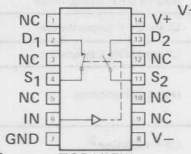
ORDER NUMBERS:
DG300AP OR DG300BP
DG304AP OR DG304BP
SEE PACKAGE 11
DG300CJ
DG304CJ
SEE PACKAGE 7
DG300AL OR DG304AL
SEE PACKAGE 16

LOGIC	SWITCH
0	OFF
1	ON

SPDT DG301 or DG305

Dual-In-Line and Flat Package

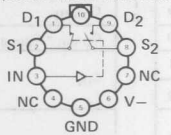
ORDER NUMBERS:
DG301AP OR DG301BP
DG305AP OR DG305BP
SEE PACKAGE 11
DG301CJ
DG305CJ
SEE PACKAGE 7
DG301AL OR DG305AL
SEE PACKAGE 16



TOP VIEW

Metal Can Package

V+ (SUBSTRATE AND CASE)



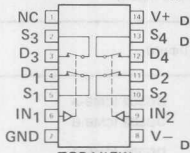
TOP VIEW

ORDER NUMBERS:
DG301AA OR DG301BA
DG305AA OR DG305BA
SEE PACKAGE 2

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

DUAL DPST DG302 or DG306

Dual-In-Line and Flat Package



TOP VIEW

ORDER NUMBERS:
DG302AP OR DG302BP
DG306AP OR DG306BP
SEE PACKAGE 11
DG302CJ
DG306CJ
SEE PACKAGE 7
DG302AL OR DG306AL
SEE PACKAGE 16

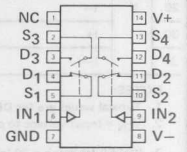
LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT DG303 or DG307

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

ORDER NUMBERS:
DG303AP OR DG303BP
DG307AP OR DG307BP
SEE PACKAGE 11
DG303CJ
DG307CJ
SEE PACKAGE 7
DG303AL OR DG307AL
SEE PACKAGE 16

Dual-In-Line and Flat Package



TOP VIEW

SWITCH STATES ARE FOR LOGIC "1" INPUTS (POSITIVE LOGIC)

SAN QUALIFIED

ABSOLUTE MAXIMUM RATINGS

V_{IN} to Ground V^+ +18 V, V^+ −36 V
V_S or V_D V^+ to V^-
V^+ to Ground +36 V
V^+ to V^- +36 V
Current, Any Terminal (Except S or D) 30 mA
Current, S or D, Continuous 30 mA
Pulsed 1 ms 10% Duty Cycle 100 mA
Operating Temperature (A Suffix) . . . −55 to +125°C
(B Suffix) . . . −20 to +85°C
(C Suffix) 0 to +70°C
Storage Temperature (A & B Suffix) . . −65 to +150°C
(C Suffix) −65 to +125°C

Power Dissipation*
14 Pin Sidebraze DIP (P)** 825 mW
14 Pin Plastic DIP (J)*** 470 mW
Metal Can (A)**** 450 mW
Flat Package (L)***** 750 mW

*Device mounted with all leads welded or soldered to PC board.
**Derate 11 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C
****Derate 6 mW/°C above 75°C
*****Derate 10 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		Characteristics			Typ[1] 25°C	Max Limits A/B Suffix −55°C/−20°C	A/B Suffix 25°C	A/B Suffix 125°C/85°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Unit	Test Conditions V+ = +15 V, V− = −15 V, Gnd = 0 V	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability		±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance		30	50	50	75	50	50	75	Ω	V_D = +10 V, I_S = −10 mA	Note 2
3					30	50	50	75	50	50	75		V_D = −10 V, I_S = +10 mA	
4		$I_{S(off)}$	Source OFF Leakage Current		0.1		1	100		5	100	nA	V_S = +14 V, V_D = −14 V	Note 2
5					−0.1		−1	−100		−5	−100		V_S = −14V, V_D = +14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current		0.1		1	100		5	100		V_D = +14 V, V_S = −14 V	
7					−0.1		−1	−100		−5	−100		V_D = −14 V, V_S = +14 V	
8		$I_{D(on)}$	Channel ON Leakage Current		0.1		1	100		5	100		V_D = V_S = +14 V	Note 2
9					−0.1		−2	−200		−5	−200		V_D = V_S = −14 V	
10	INPUTS	I_{INH}	Input Current Input Voltage High	DG300-303 Only	−0.001	−1	−1	−1		−1		μA	V_{IN} = +5.0 V	
11				DG300-307 Only	0.001	1	1	1		1			V_{IN} = +15 V	
12		I_{INL}	Input Current Input Voltage Low		−0.001	−1	−1	−1		−1			V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn ON Time	DG300-303 Only	150		300					nS	See Switching Time Test Circuit	
14		t_{off}	Turn OFF Time		130		250							
15		t_{on}	Turn ON Time	DG304-307 Only	110		250							
16		t_{off}	Turn OFF Time		70		150							
17		$t_{on} - t_{off}$	Break-Before-Make Interval	DG301/303 DG305/307 Only	50								See Break-Before-Make Time Test Circuit	
18		$C_{S(off)}$	Source OFF Capacitance		14							pF	V_S = 0, Note 2	f = 1 MHz
19		$C_{D(off)}$	Drain OFF Capacitance		14								V_D = 0, Note 2	
20		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		40								V_D = V_S = 0, Note 2	
21		C_{IN}	Input Capacitance		6								V_{IN} = 0	
22					3.5								V_{IN} = +15 V	
23			OFF Isolation[3]		58							dB	V_{IN} = 0, R_L = 1K Ω, C_L = +15 pF V_S = 1 V_{RMS}, f = 500 kHz	
24	SUPPLY	I+	Positive Supply Current	DG300-303 Only	0.23	1	0.5	0.5		1		mA	V_{IN} = 4 V (One Input) (All Other Inputs = 0)	
25		I−	Negative Supply Current		−0.001	−10	−10	−100		−100				
26		I+	Positive Supply Current		0.001	10	10	100		100		μA	V_{IN} = 0.8 V (All Inputs)	
27		I−	Negative Supply Current		−0.001	−10	−10	−100		−100				
28		I+	Positive Supply Current	DG304-307 Only	0.001	10	10	100		100			V_{IN} = +15 V (All Inputs)	
29		I−	Negative Supply Current		−0.001	−10	−10	−100		−100				
30		I+	Positive Supply Current		0.001	10	10	100		100			V_{IN} = 0 (All Inputs)	
31		I−	Negative Supply Current		−0.001	−10	−10	−100		−100				

NOTES:
1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. V_{IN} = Input voltage to perform proper function. DG300-303: V_{IN} — For logic "1" = 4 V, for logic "0" = 0.8 V. DG304-307: V_{IN} — For logic "1" = 11 V, for logic "0" = 3.5 V
3. "OFF" Isolation = 20 log V_S/V_D. V_S = Input to OFF switch, V_D = Output. Since the DG300-301 and DG304/305 have a N/C pin between S and D, the OFF Isolation generally improves by 7 dB @ 500 KHz over value shown here.

DG300 ICMA-A DG302 ICMB-A
DG301 ICMA-B DG303 ICMB-B
DG304 ICMA-C DG306 ICMB-C
DG305 ICMA-D DG307 ICMB-D

Monolithic CMOS Analog Switches

Siliconix

designed for . . .

- **Portable, Battery Operated Circuits**
- **Low Leakage Switching i.e. Sample and Hold Circuits**
- **Communication Systems**
- **Low Level Switching Circuits**
- **Fast Switching Circuits such as Multiplexers**
- **Standard Linear Dual Supply Voltages or Single Supply Systems**

BENEFITS

- **Environmentally Rugged**
 - Latchproof CMOS
- **Low Standby Power**
 - 0.06 μW Typical
- **Minimizes Signal Error**
 - 0.1 nA Typical Leakage
- **Low Operating Power**
 - 7.5 mW Typical
- **Reduced Voltage Drop Across Switch in ON Condition**
 - $r_{ds(on)} < 50\ \Omega$
- **Minimizes Switching Time**
 - Typ t_{on} & $t_{off} < 180$ ns
- **Minimizes System Power Requirements**
 - Single Supply Operation Capabilities
- **Easily Interfaced**
 - TTL, DTL / CMOS Input Compatible
 - Pin to Pin Replacement for DG180 Series Switches
- **Reduces External Component Requirements**
 - Logic Input Overvoltage Protection

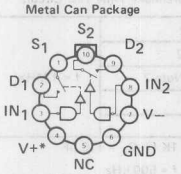
DESCRIPTION

The DG381 through DG390 switch family features four switching functions using CMOS technology for low and nearly constant ON resistance (less than 50 Ω) over the full analog signal range. In the ON condition the switches will conduct current in either direction with no offset voltage. With low power dissipation, a few milliwatts, this series of switches becomes an ideal candidate for battery-powered or remote switching applications. The switching speed is among the fastest available with the low quiescent power dissipation. In the OFF condition, the switches will block voltages up to 30 V peak-to-peak. A logic input driver controls the ON/OFF state of the switches. (See the "Pin Configuration" for switch status with a logic "1" input.) The switches are TTL and CMOS input compatible and have a logic "0" state with an input less than 0.8 V and a logic "1" state with an input greater than 4.0 V. A pull-up resistor should be added for totem pole TTL outputs. The logic inputs are protected against overvoltage up to 18 V above and 36 V below the positive supply. The combination of low cost, low power, low resistance and fast speed optimizes system design.

PIN CONFIGURATIONS

DUAL SPST DG381

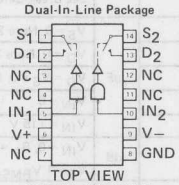
Metal Can Package



TOP VIEW

ORDER NUMBERS:
DG381AA OR DG381BA
SEE PACKAGE 2

Dual-In-Line Package



TOP VIEW

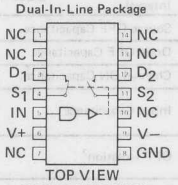
ORDER NUMBERS:
DG381AP OR DG381BP
SEE PACKAGE 11
DG381CJ
SEE PACKAGE 7

LOGIC	SW 1 SW 2
0	ON
1	OFF

*(SUBSTRATE AND CASE)

SPDT DG387

Dual-In-Line Package



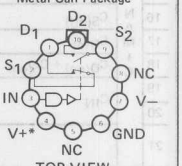
TOP VIEW

ORDER NUMBERS:
DG387AP OR DG387BP
SEE PACKAGE 11
DG387CJ
SEE PACKAGE 7

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*(SUBSTRATE AND CASE)

Metal Can Package

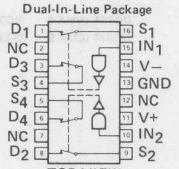


TOP VIEW

ORDER NUMBERS:
DG387AA OR DG387BA
SEE PACKAGE 2

DUAL DPST DG384

Dual-In-Line Package



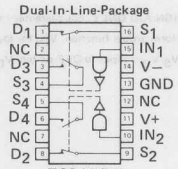
TOP VIEW

ORDER NUMBERS:
DG384AP OR DG384BP
SEE PACKAGE 12
DG384CJ
SEE PACKAGE 8

LOGIC	SW 1–4
0	OFF
1	ON

DUAL SPDT DG390

Dual-In-Line-Package



TOP VIEW

ORDER NUMBERS:
DG390AP OR DG390BP
SEE PACKAGE 12
DG390CJ
SEE PACKAGE 8

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

SWITCH STATES ARE FOR LOGIC "1" INPUTS (POSITIVE LOGIC)

V+ to V− 36 V
Current, Any Terminal (Except S or D) 30 mA
Current, S or D, Continuous 30 mA
Pulsed 1 ms 10% Duty Cycle 100 mA
Operating Temperature (A Suffix) . . −55 to +125°C
(B Suffix) . . −20 to +85°C
(C Suffix) . . . 0 to +70°C
Storage Temperature (A & B Suffix) . . −65 to +150°C
(C Suffix) −65 to +125°C

*Device mounted with all leads welded or soldered to PC board.
**Derate 11 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C
****Derate 6 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

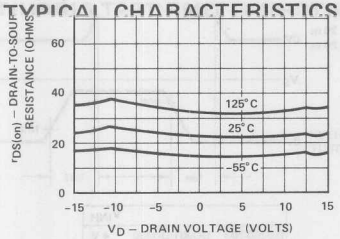
All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

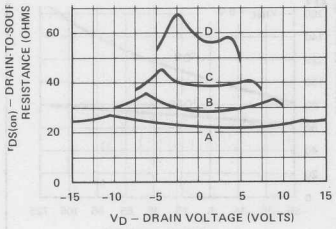
		Characteristics		Typ[1] 25°C	Max Limits A/B Suffix −55°C/−20°C	A/B Suffix 25°C	A/B Suffix 125°C/85°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Unit	Test Conditions V+ = +15 V, V− = −15 V, Gnd = 0 V	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	30	50	50	75	50	50	75	Ω	V_D = +10 V, I_S = −10 mA	Note 2
3				30	50	50	75	50	50	75		V_D = −10 V, I_S = +10 mA	
4		$I_{S(off)}$	Source OFF Leakage Current	0.1		1	100		5	100	nA	V_S = +14 V, V_D = −14 V	Note 2
5				−0.1		−1	−100		−5	−100		V_S = −14 V, V_D = +14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	0.1		1	100		5	100		V_D = +14 V, V_S = −14 V	
7				−0.1		−1	−100		−5	−100		V_D = −14 V, V_S = + 14 V	
8		$I_{D(on)}$	Channel ON Leakage Current	0.1		1	100		5	100		V_D = V_S = +14 V	Note 2
9				−0.1		−2	−200		−5	−200		V_D = V_S = −14 V	
10	IN	I_{INH}	Input Current Input Voltage High	−0.001	−1	−1	−1		−1		μA	V_{IN} = +5 V	
11				0.001	1	1	1		1			V_{IN} = +15 V	
12		I_{INL}	Input Current Input Voltage Low	−0.001	−1	−1	−1		−1			V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn ON Time	150		300					nS	See Switching Time Test Circuit	
14		t_{off}	Turn OFF Time	130		250							
15		$t_{on} - t_{off}$	Break-Before-Make Interval DG387/390 only	50								See Break-Before-Make Time Test Circuit	
16		$C_{S(off)}$	Source OFF Capacitance	14							pF	V_S = 0, Note 2	f = 1 MHz
17		$C_{D(off)}$	Drain OFF Capacitance	14								V_D = 0, Note 2	
18		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	40								V_D = V_S = 0, Note 2	
19		C_{IN}	Input Capacitance	6								V_{IN} = 0	
20				3.5								V_{IN} = +15 V	
21			OFF Isolation[3]	58							dB	V_{IN} = 0, R_L = 1K Ω, C_L = +15 pF V_S = 1 V_{RMS}, f = 500 kHz	
22	SUPPLY	I+	Positive Supply Current	0.23	1	0.5	0.5		1		mA	V_{IN} = 4 V (One Input) (All Other Inputs = 0)	
23		I−	Negative Supply Current	−0.001	−10	−10	−100		−100				
24		I+	Positive Supply Current	0.001	10	10	100		100		μA	V_{IN} = 0.8 V (All Inputs)	
25		I−	Negative Supply Current	−0.001	−10	−10	−100		−100				

NOTES:
1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing
2. V_{IN} = Input voltage to perform proper function, V_{IN} for logic "1" = 4 V, for logic "0" = 0.8 V
3. "OFF" Isolation $\triangleq$ 20 log V_S/V_D = Input to OFF switch, V_D = Output

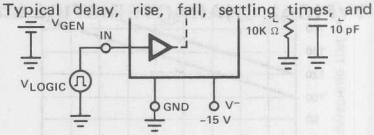
DG381 ICMA-E DG384 ICMB A
DG387 ICMA B DG390 ICMB B

TYPICAL CHARACTERISTICS





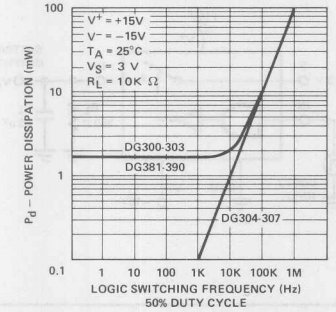
Typical delay, rise, fall, settling times, and



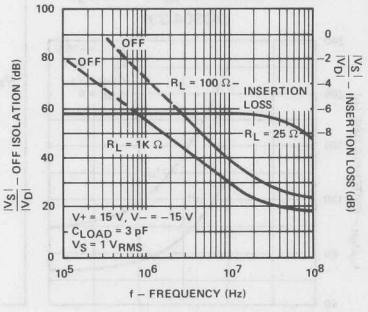
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater spikes.

Device Power Dissipation vs Switching Frequency

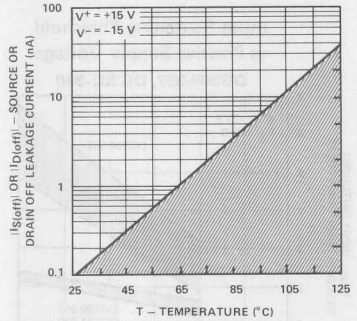
Single Logic Input



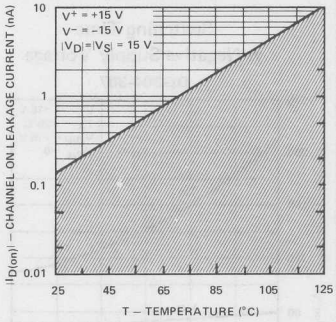
OFF Isolation Insertion Loss vs Frequency



$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*

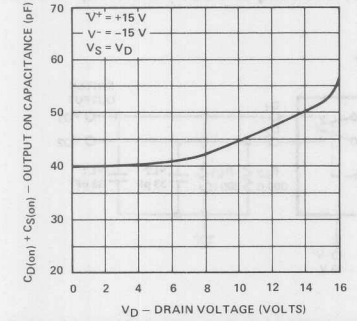


$I_{D(on)}$ vs Temperature*

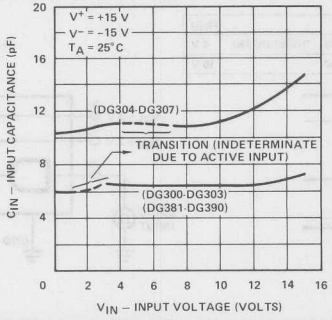


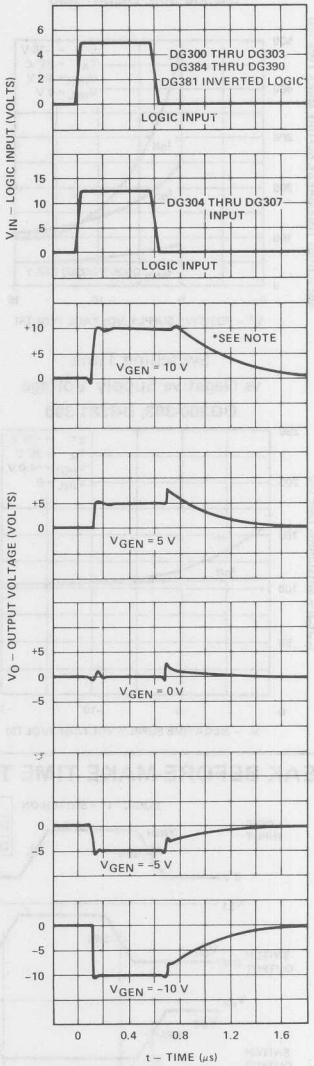
*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

Output ON Capacitance vs Drain Voltage



Input Capacitance vs Input Voltage

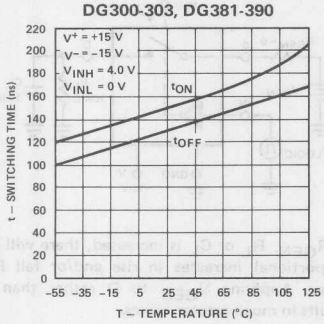




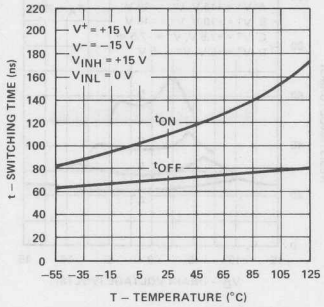
*Note: The turn-off time is primarily limited here by the RC time constant (100 ns) of the load.

TYPICAL CHARACTERISTICS (Cont'd)

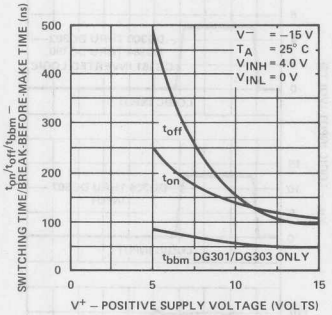
Switching Time vs Temperature
DG300-303, DG381-390



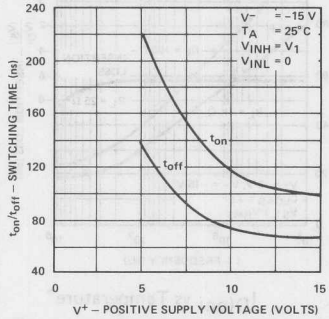
Switching Time vs Temperature
DG304-307



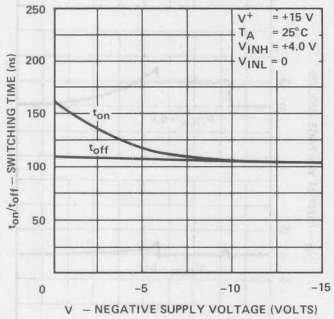
Switching Time and Break-Before-Make Time vs Positive Supply Voltage
DG300-303, DG381-390



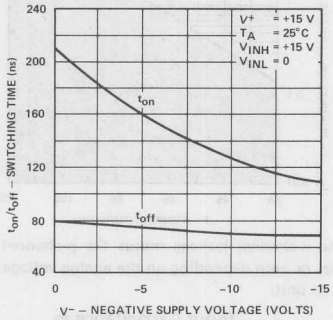
Switching Time vs Positive Supply Voltage
DG304-307



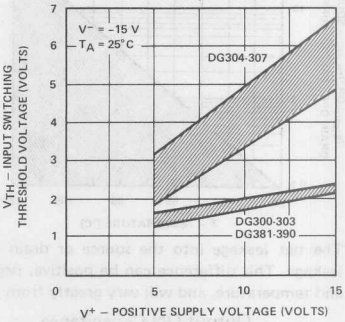
Switching Time vs Negative Supply Voltage
DG300-303, DG381-390



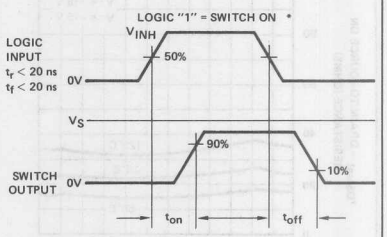
Switching Time vs Negative Supply Voltage
DG304-307



Input Switching Threshold vs Positive Supply Voltage
DG300-307, DG381-390

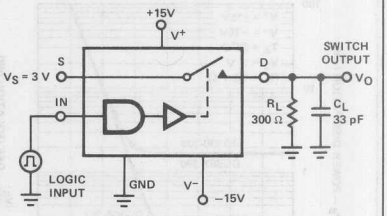


SWITCHING TIME TEST CIRCUIT (DG300-307 DG381-390)

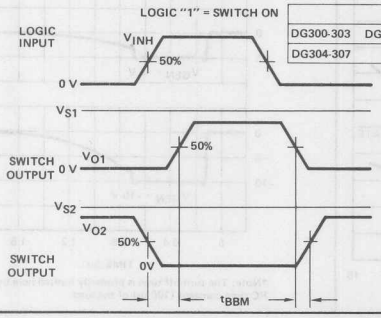


		VINH
DG300-303	DG381-DG390	4 V
DG304-307		15 V

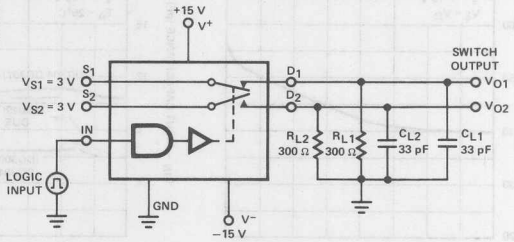
*INVERTED LOGIC FOR DG381



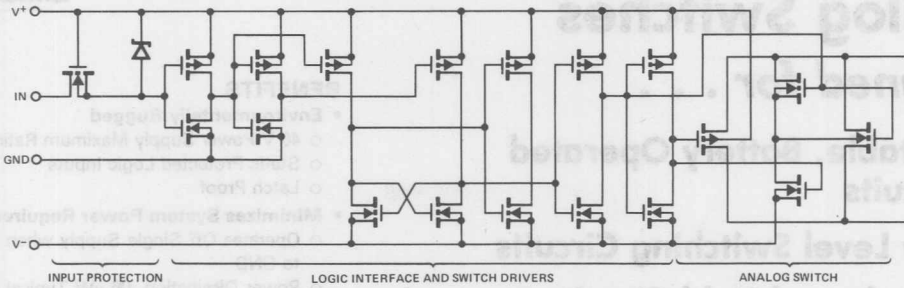
BREAK-BEFORE-MAKE TIME TEST CIRCUIT SPDT (DG301, DG303, DG305, DG307, DG384, DG390)



		VINH
DG300-303	DG381-DG390	4 V
DG304-307		15 V



PARTIAL SCHEMATIC OF TYPICAL SWITCH (DG300-307, DG381-390)

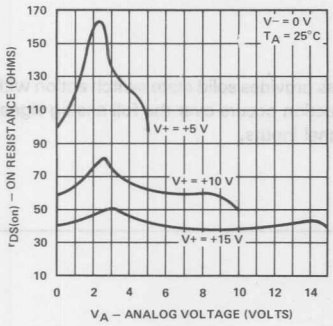


APPLICATIONS

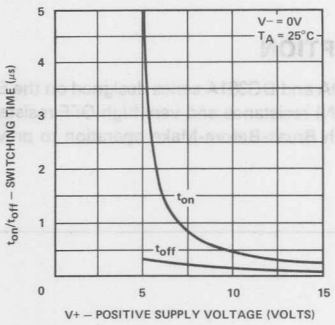
Single Supply Operation

The DG300 series of analog switches will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) Increased $r_{DS(ON)}$; 2) slower switching speed. Typical curves for aid in designing with single supplies are supplied in the Figures below. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single operation are V+ and 0 volts.

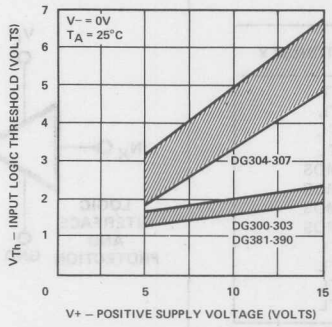
$R_{DS(on)}$ vs Analog and Positive Supply Voltage With V– = 0V



Switching Time vs V+ – Positive Supply Voltage



Input Threshold Voltage vs Positive Supply



Single Supply Range:
(V– and GND Tied Together)
V+: +5 V to +25 V

Analog Signal Range:
$V- \leq V_{ANALOG} \leq V+$

designed for . . .

- **Portable, Battery Operated Circuits**
- **Low Level Switching Circuits**
- **Sample and Hold Circuits**
- **High Speed Switching**
- **Programmable Gain Amplifiers**
- **Single or Dual Supply Systems**

BENEFITS

- **Environmentally Rugged**
 - 40 V Power Supply Maximum Rating
 - Static Protected Logic Inputs
 - Latch Proof
- **Minimizes System Power Requirements**
 - Operates Off Single Supply when V– Tied to GND
 - Power Dissipation .06 μW Typical DG304A-307A
- **Fast t_{on} and t_{off} <110 nsec DG304-DG307A**
- **Minimizes Signal Error**
 - Low $r_{DS(on)}$ 30 ohm Typical
 - Low Leakage 40 pA @ 25°C
 1 nA @ 125°C
 - Full Rail to Rail Analog Signal Range
- **Easily Interfaced**
 - TTL and CMOS Compatible
- **Pin for Pin Compatible With**
 - Harris HI-3XX Family
- **DG381A-DG390A are Pin for Pin Compatible with DG180 Series**

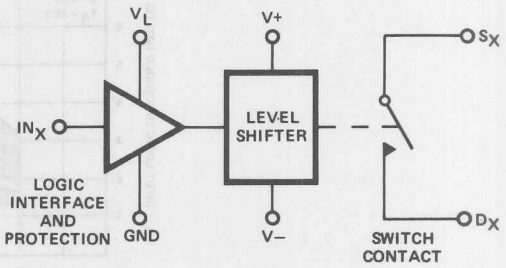
DESCRIPTION

The DG300A and DG381A series designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 30 ohms contact (ON) resistance and very high OFF resistance. True bidirectional switch action occurs over the full analog signal range of ±15V, with Break-Before-Make operation to prevent momentary shorting of signal inputs.

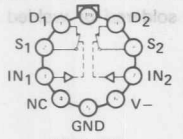
FUNCTIONAL DESCRIPTION

PART NUMBER	TYPE SWITCH	COMPATIBILITY
DG300A	Dual SPST	TTL
DG301A	SPDT	TTL
DG302A	Dual DPST	TTL
DG303A	Dual SPDT	TTL
DG304A	Dual SPST	CMOS
DG305A	SPDT	CMOS
DG306A	Dual DPST	CMOS
DG307A	Dual SPDT	CMOS
DG381A	Dual SPST	TTL
DG384A	Dual DPST	TTL
DG387A	SPDT	TTL
DG390A	Dual SPDT	TTL

FUNCTIONAL DIAGRAM (typical channel)

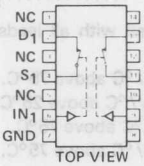


V+ (SUBSTRATE AND CASE)



TOP VIEW

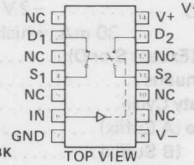
ORDER NUMBERS:
DG300AAA OR DG300ABA
DG304AAA OR DG304ABA
SEE PACKAGE 2



TOP VIEW

LOGIC	SWITCH
0	OFF
1	ON

ORDER NUMBERS:
DG300AAK OR DG300ABK
OR DG300ACK
DG304AAK OR DG304ABK
OR DG304ACK
SEE PACKAGE 9
DG300ACJ
DG304ACJ
SEE PACKAGE 7
DG300AAL OR DG304AAL
SEE PACKAGE 16

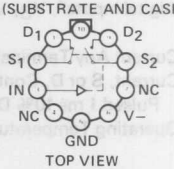


TOP VIEW

ORDER NUMBERS:
DG301AAK OR DG301ABK
OR DG301ACK
DG305AAK OR DG305ABK
OR DG305ACK
SEE PACKAGE 9
DG301ACJ
DG305ACJ
SEE PACKAGE 7
DG301AAL OR DG305AAL
SEE PACKAGE 16

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

V+ (SUBSTRATE AND CASE)

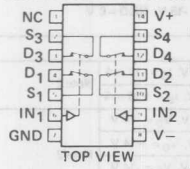


TOP VIEW

ORDER NUMBERS:
DG301AAA OR DG301ABA
DG305AAA OR DG305ABA
SEE PACKAGE 2

DUAL DPST DG302A or DG306A

Dual-In-Line and Flat Package



TOP VIEW

ORDER NUMBERS:
DG302AAK OR DG302ABK
OR DG302ACK
DG306AAK OR DG306ABK
OR DG306ACK
SEE PACKAGE 9
DG302ACJ
DG306ACJ
SEE PACKAGE 7
DG302AAL OR DG306AAL
SEE PACKAGE 16

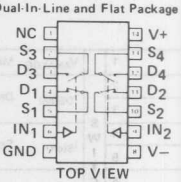
LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT DG303A or DG307A

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

ORDER NUMBERS:
DG303AAK OR DG303ABK
OR DG303ACK
DG307AAK OR DG307ABK
OR DG307ACK
SEE PACKAGE 9
DG303ACJ
DG307ACJ
SEE PACKAGE 7
DG303AAL OR DG307AAL
SEE PACKAGE 16

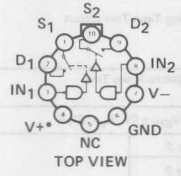
Dual-In-Line and Flat Package



TOP VIEW

DUAL SPST DG 381A

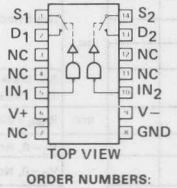
Metal Can Package



TOP VIEW

ORDER NUMBERS:
DG381AAA OR DG381ABA
SEE PACKAGE 2

Dual-In-Line Package



TOP VIEW

ORDER NUMBERS:
DG381AAK OR DG381ABK
OR DG381ACK
SEE PACKAGE 9
DG381ACJ
SEE PACKAGE 7

LOGIC	SW 1 SW 2
0	ON
1	OFF

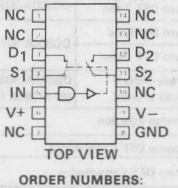
*(SUBSTRATE AND CASE)

SPDT DG387A

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*(SUBSTRATE AND CASE)

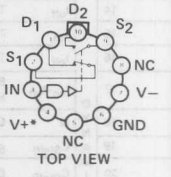
Dual-In-Line Package



TOP VIEW

ORDER NUMBERS:
DG387AAK OR DG387ABK
OR DG387ACK
SEE PACKAGE 9
DG387ACJ
SEE PACKAGE 7

Metal Can Package

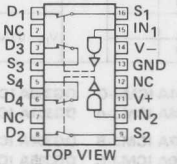


TOP VIEW

ORDER NUMBERS:
DG387AAA OR DG387ABA
SEE PACKAGE 2

DUAL DPST DG384A

Dual-In-Line Package



TOP VIEW

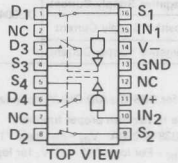
ORDER NUMBERS:
DG384AAK OR DG384ABK
OR DG384ACK
SEE PACKAGE 10
DG384ACJ
SEE PACKAGE 8

LOGIC	SW 1–4
0	OFF
1	ON

DUAL SPDT DG390A

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

Dual-In-Line-Package



TOP VIEW

ORDER NUMBERS:
DG390AAK OR DG390ABK
OR DG390ACK
SEE PACKAGE 10
DG390ACJ
SEE PACKAGE 8

SWITCH STATES ARE FOR LOGIC "1" INPUTS (POSITIVE LOGIC)

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–

V+ 44 V
GND 25 V
Digital inputs[4], V_S, V_D –2 V to (V^+ +2 V) or 30 mA, whichever occurs first
Current Any Terminal (Except S or D) 30 mA
Current, S or D, Continuous 30 mA
Pulsed 1 ms 10% Duty Cycle 100 mA
Operating Temperature (A Suffix) –55 to 125°C
(B Suffix) –20 to 85°C
(C Suffix) 0 to 70°C
Storage Temperature (A & B Suffix) –65 to 150°C
(C Suffix) –65 to 125°C
Power Dissipation*
Cerdip (K)** 825 mW
Plastic DIP (J)*** 470 mW
Metal Can (A)**** 450 mW
Flat Package (L)***** 750 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 11 mW/°C above 75°C.
***Derate 6.5 mW/°C above 25°C.
****Derate 6 mW/°C above 75°C.
*****Derate 10 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

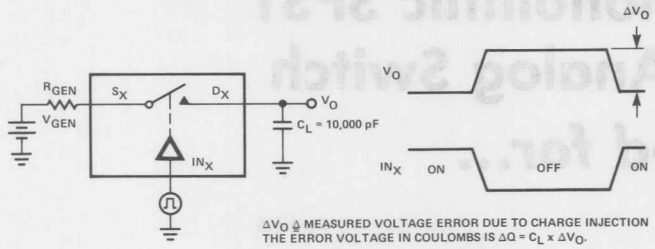
All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC			TYP[1] 25°C	MAX LIMITS A SUFFIX -55°C/-20°C	A SUFFIX 25°C	A SUFFIX 125°C/85°C	B/C SUFFIX 0°C	B/C SUFFIX 25°C	B/C SUFFIX 70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V- = -15 V, GND = 0 V	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability		±15		±15	±15		±15	±15	V		
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance		30	50	50	75	50	50	75	Ω	V_D = +10 V, I_S = -10 mA	Note 2
3					30	50	50	75	50	50	75		V_D = -10 V, I_S = +10 mA	
4		$I_{S(off)}$	Source OFF Leakage Current		0.1		1	100		5	100	nA	V_S = +14 V, V_D = -14 V	Note 2
5					-0.1		-1	-100		-5	-100		V_S = -14 V, V_D = +14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current		0.1		1	100		5	100		V_D = +14 V, V_S = -14 V	
7					-0.1		-1	-100		-5	-100		V_D = -14 V, V_S = +14 V	
8		$I_{D(on)}$	Channel ON Leakage Current		0.1		1	100		5	100		V_D = V_S = +14 V	Note 2
9					-0.1		-2	-200		-5	-200		V_D = V_S = -14 V	
10	INPUT	I_{INH}	Input Current Input Voltage High	DG300A-307A Only	-0.001	-1	-1	-1		-1		µA	V_{IN} = +5.0 V	
11					0.001	1	1	1		1			V_{IN} = +15 V	
12		I_{INL}	Input Current Input Voltage Low		-0.001	-1	-1	-1		-1			V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn-ON Time	DG381A-390A DG300A-303A Only	150		300					ns	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time		130		250							
15		t_{on}	Turn ON Time	DG304A-307A Only	110		250							
16		t_{off}	Turn OFF Time		70		150							
17		t_{on}-t_{off}	Break-Before-Make Interval	DG301A/303A/305A/307A 387A/390A Only	50								See Break-Before-Make Time Test Circuit	
18		Q	Charge Injection		3							mV	R_{GEN} = 0Ω, V_{GEN} = 0V, C_L = .01µF	
19		$C_{S(off)}$	Source OFF Capacitance		14							pF	V_S = 0, Note 2	f = 1 MHz
20		$C_{D(off)}$	Drain OFF Capacitance		14								V_D = 0, Note 2	
21		$C_{D(on)}$ + $C_{S(on)}$	Channel ON Capacitance		40								V_D = V_S = 0, Note 2	
22		C_{IN}	Input Capacitance		6								V_{IN} = 0	
23					7								V_{IN} = +15 V	
24		OIRR	OFF Isolation[3]		62							dB	V_{IN} = 0, R_L = 1 KΩ, V_S = 1 V_{RMS}, f = 500 KHz	
25		CCRR	Channel to Channel Crosstalk		74									
26	SUPPLY	I+	Positive Supply Current	DG381A-390A DG300A-303A Only	0.23	1	0.5	0.5		1		mA	V_{IN} = 4V (One Input) (All Other Inputs = 0)	
27		I–	Negative Supply Current		-0.001	-10	-10	-100		-100		µA		
28		I+	Positive Supply Current		0.001	10	10	100		100			V_{IN} = 0.8 V (All Inputs)	
29		I–	Negative Supply Current		-0.001	-10	-10	-100		-100				
30		I+	Positive Supply Current	DG304A-307A Only	0.001	10	10	100		100			V_{IN} = +15V (All Inputs)	
31		I–	Negative Supply Current		-0.001	-10	-10	-100		-100				
32		I+	Positive Supply Current		0.001	10	10	100		100			V_{IN} = 0 (All Inputs)	
33		I–	Negative Supply Current		-0.001	-10	-10	-100		-100				

NOTES:
1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. V_{IN} = input voltage to perform proper function.
 DG300A-303A, DG381A-390A: V_{IN} – For logic "1" = 4 V, for logic "0" = 0.8V
 DG304A-307A: V_{IN} – For logic "1" = 11 V, for logic "0" = 3.5 V
3. "OFF" isolation = 20 log V_S/V_D, V_S = input to OFF switch, V_D = Output
4. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

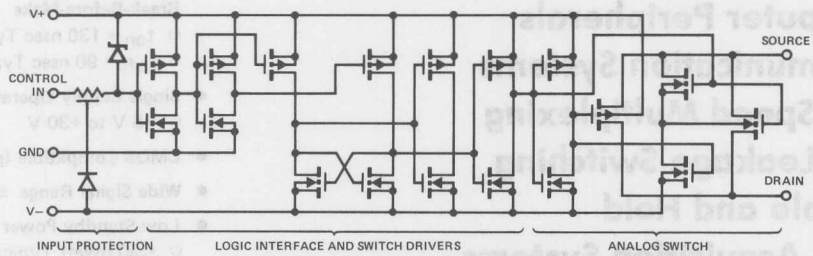
DG381A ICMJ-C **DG300A ICMJ-A** **DG302A ICMJ-A**
DG384A ICMJ-A **DG301A ICMJ-B** **DG303A ICMJ-C**
DG387A ICMJ-B **DG304A ICMJ-D** **DG306A ICMJ-D**
DG390A ICMJ-C **DG305A ICMJ-E** **DG307A ICMJ-F**

CHARGE INJECTION TEST CIRCUIT

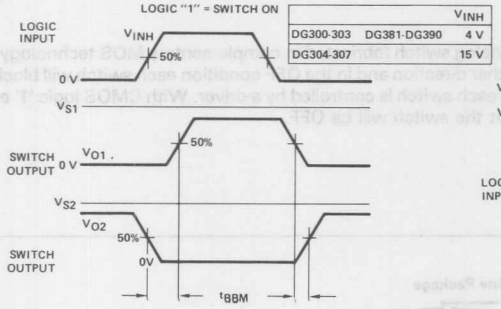


$\Delta V_O \triangleq$ MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION
THE ERROR VOLTAGE IN COULOMBS IS $\Delta Q = C_L \times \Delta V_O$.

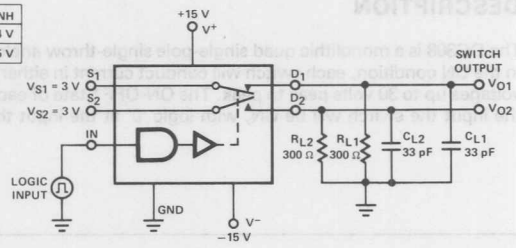
SCHEMATIC OF TYPICAL SWITCH



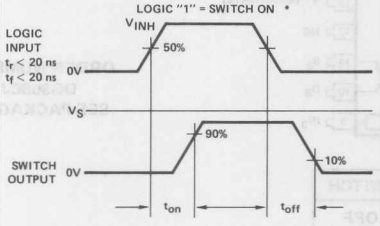
TEST CIRCUITS
BREAK-BEFORE-MAKE TIME TEST CIRCUIT SPDT
(DG301A, DG303A, DG305A, DG307A, DG384A, DG390A)



		V_{INH}
DG300-303	DG381-DG390	4 V
DG304-307		15 V

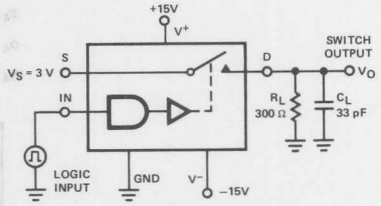


SWITCHING TIME TEST CIRCUITS (DG300A–307A, DG381A–390A)



		V_{INH}
DG300-303	DG381-DG390	4 V
DG304-307		15 V

*INVERTED LOGIC FOR DG381



designed for...

- **Portable, Battery Instrumentation**
- **Automotive Applications**
- **Computer Peripherals**
- **Communication Systems**
- **Hgh Speed Multiplexing**
- **Low Leakage Switching**
- **Sample and Hold**
- **Data Acquisition Systems**

BENEFITS

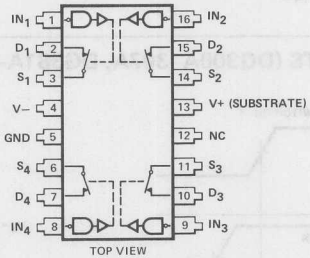
- **High Speed Switching with Break-Before-Make**
 - t_{on} = 130 nsec Typical
 - t_{off} = 90 nsec Typical
- **Single Supply Operation**
 - +5 V to +30 V
- **CMOS Compatible (positive logic)**
- **Wide Signal Range ±15 V**
- **Low Standby Power**
 - <30 μWatt Typical
- **Minimizes Signal Error**
 - $r_{DS} < 80\ \Omega$ Typical
 - $I_{D(off)} < 100$ pA Typical
- **Environmentally Rugged**
 - Latchproof CMOS Process

DESCRIPTION

The DG308 is a monolithic quad single-pole single-throw analog switch fabricated in complementary MOS technology. In the ON condition, each switch will conduct current in either direction and in the OFF condition each switch will block voltages up to 30 volts peak to peak. The ON-OFF State of each switch is controlled by a driver. With CMOS logic '1' at the input the switch will be ON, with logic '0' at the input the switch will be OFF.

PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

LOGIC	SWITCH
0	OFF
1	ON

SWITCH CLOSED FOR LOGIC "1" INPUT (POSITIVE LOGIC)

ORDER NUMBER:
DG308CJ
SEE PACKAGE 7

ABSOLUTE MAXIMUM RATING

V_{IN} to Ground $V^+ + 18$ V, $V^+ - 36$ V
V_S or V_D V^+ to V^-
V^+ to Ground +36 V
V^+ to V^- +36 V
Current, Any Terminal (Except S or D) 30 mA
Current, S or D, Continuous 20 mA
Pulsed 1 ms 10% Duty Cycle 100 mA
Operating Temperature (C Suffix) 0 to +70°C
Storage Temperature (C Suffix) −65 to +125°C
Power Dissipation (Package)*
16 Pin Plastic DIP** 470 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

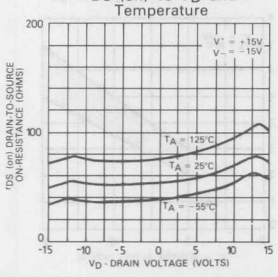
		CHARACTERISTIC	(Note 1) TYP 25°C	MAX LIMITS C SUFFIX 0°C	25°C	70°C	UNIT	TEST CONDITIONS V+ = +15 V, V− = −15 V, Gnd = 0 V	
1		V_{ANALOG} Minimum Analog Signal Handling Capability	±15		±15	±15	V	Switch ON I_S = 10 mA	
2	SWITCH	$r_{DS(ON)}$ Drain Source ON Resistance	70	100	100	125	Ω	V_D = 10 V, I_S = −1 mA	(Note 2)
3			60	100	100	125		V_D = −10 V, I_S = 1 mA	
4		$I_{S(off)}$ Source OFF Leakage Current	0.1		5	100	nA	V_S = +14 V, V_D = −14 V	(Note 2)
5			−0.1		−5	−100		V_S = −14 V, V_D = +14 V	
6		$I_{D(off)}$ Drain OFF Leakage Current	0.1		5	100		V_S = −14V, V_D = +14 V	
7			−0.1		−5	−100		V_S = +14V V_D = −14 V	
8		$I_{D(on)}$ Drain ON Leakage Current	0.1		5	200		V_D = V_S = + 14 V	(Note 2)
9			−0.1		−5	−200		V_D = V_S = − 14 V	
10	INPUT	I_{INH} Input Current Input Voltage High	0.001		1		µA	V_{IN} = 15 V	
11		I_{INL} Input Current Input Voltage Low	−0.001		−1			V_{IN} = 0 V	
12	DYNAMIC	t_{on} Turn-ON Time	130		200		ns	See Switching Time Test Circuit	
13		t_{off} Turn-OFF Time	90		150				
14		$C_{S(off)}$ Source OFF	8				pF	V_S = 0 V, V_{IN} = 0 V	
15		$C_{D(off)}$ Drain OFF Capacitance	8					V_D = 0 V, V_{IN} = 0 V	
16		$C_{D(on)}$ + $C_{S(on)}$ Channel ON Capacitance	22					V_D = V_S = 0 V, V_{IN} = 15 V	
17		OFF Isolation (Note 3)	78				dB	V_{IN} = 0 V, R_L = 1K Ω, C_L = 3 pF V_S = 70m V rms, f = 500 kHz	
18	SUP	I+ Positive Supply Current	0.001		100		µA	V_{IN} = 15 V or 0 V	
19		I− Negative Supply Current	−0.001		−100				

ICMD

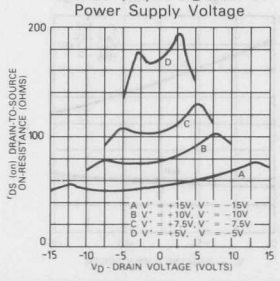
NOTES:
1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. V_{IN} = Input Voltage to perform proper function for logic '1' = 11V, for logic '0' = 3.5V
3. OFF Isolation = $20 \log_{10} \frac{|V_D|}{|V_S|}$ V_D = Output, V_S = Input to OFF Switch

TYPICAL CHARACTERISTICS

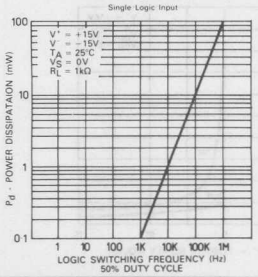
rDS (on) vs VD and Temperature



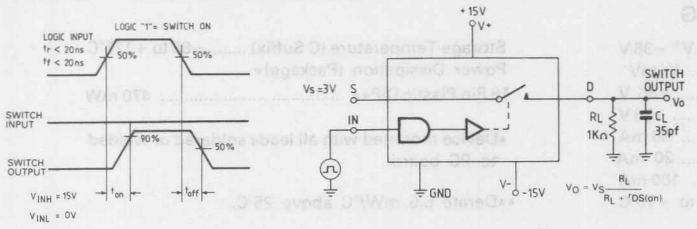
rDS (on) vs VD and Power Supply Voltage



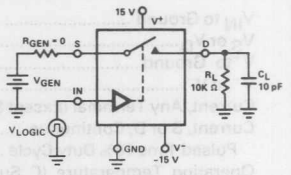
Device Power Dissipation vs Switching Frequency



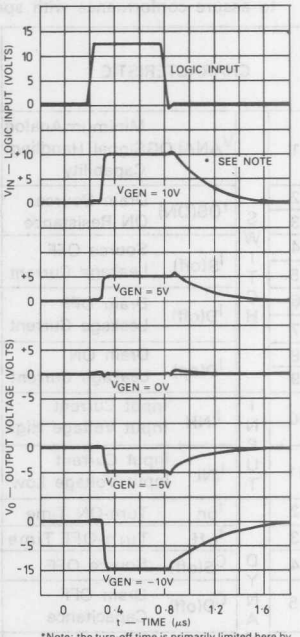
SWITCHING TIME TEST CIRCUIT



Typical delay, rise, fall, settling times, and switching transients in this circuit.



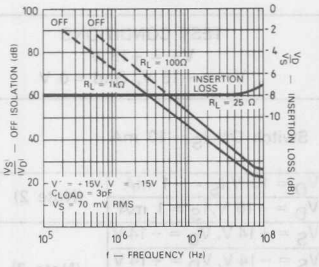
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater spikes.



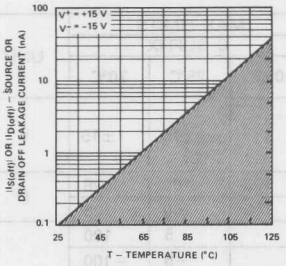
*Note: the turn-off time is primarily limited here by the RC time constant (100ns) of the load.

TYPICAL CHARACTERISTICS continued

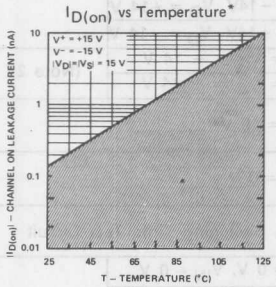
OFF-Isolation, Insertion Loss vs Frequency



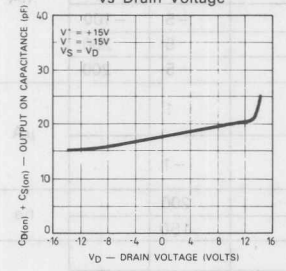
$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*



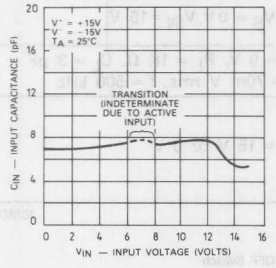
$I_{D(on)}$ vs Temperature*



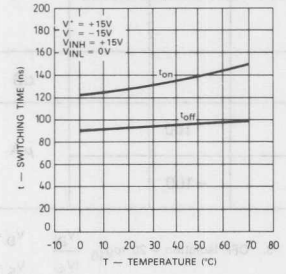
Output ON Capacitance vs Drain Voltage



Input Capacitance vs Input Voltage

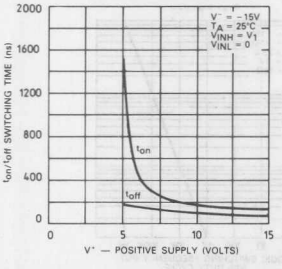


Switching Time vs Temperature

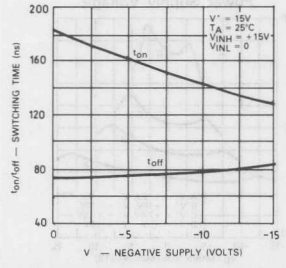


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

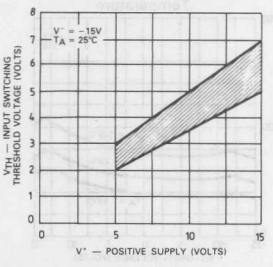
Switching Time vs Positive Supply Voltage



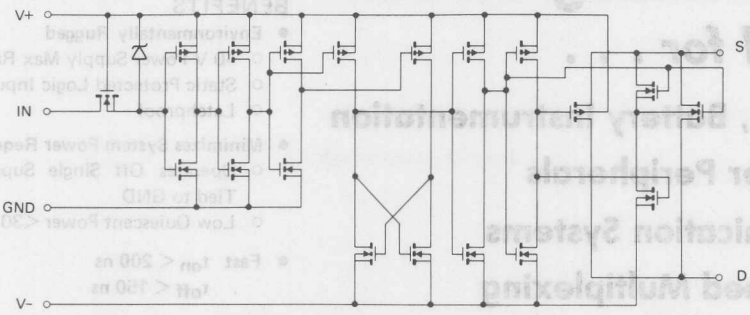
Switching Time vs Negative Supply Voltage



Input Switching Threshold vs Postitive Supply Voltage



PARTIAL SCHEMATIC OF TYPICAL SWITCH



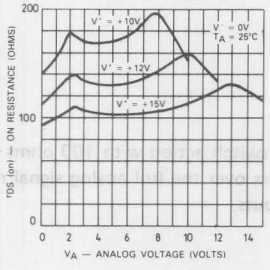
Switch closed for Logic '1' Input (V_{INH})

Single Supply Operation

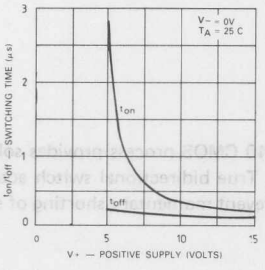
The DG308 will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The performance trade-offs while using single supplies are: 1) Increased $r_{DS(ON)}$; 2) slower switching speed. Typical curves for aid in designing with single supplies are supplied in the Figures below. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single operation are V+ and 0 volts.

Single Supply Range: (V− and GND Tied Together) V+: +5 V to +25 V
Analog Signal Range: $V- \leqslant V_{ANALOG} \leqslant V+$

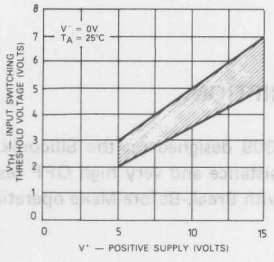
rDS(on) vs Analog and Positive Supply Voltage with $V^- = 0V$



Switching Time vs V^+ – Positive Supply Voltage



Input Switching Threshold vs Postitive Supply Voltage



designed for . . .

- **Portable, Battery Instrumentation**
- **Computer Peripherals**
- **Communication Systems**
- **High Speed Multiplexing**
- **Sample and Hold**
- **Single or Dual Supply Systems**

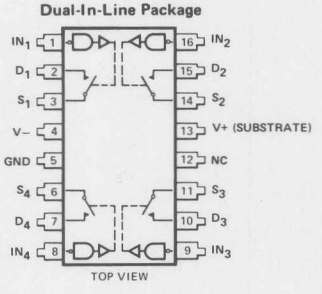
- **Environmentally Rugged**
 - 40 V Power Supply Max Rating
 - Static Protected Logic Inputs
 - Latchproof
- **Minimizes System Power Requirements**
 - Operates Off Single Supply When V– Tied to GND
 - Low Quiescent Power <30 μW Typ
- **Fast** $t_{on} < 200$ ns, $t_{off} < 150$ ns
- **Minimizes Signal Error**
 - $r_{DS(ON)} < 100\Omega$
 - $I_{D(OFF)} < 5$ nA
 - Full Rail-to-Rail Analog Signal Range
- **Easily Interfaced**
 - CMOS Logic Compatible
 - Available in Normally Open or Normally Closed
- **DG201A/DG202 are TTL Input Pin-for-Pin Compatible**

DESCRIPTION:

The DG309 designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 100 ohms contact (ON) resistance and very high OFF resistance. True bidirectional switch action occurs over the full analog signal range of ±15 V, with Break-Before-Make operation to prevent momentary shorting of signal inputs.

PIN CONFIGURATION

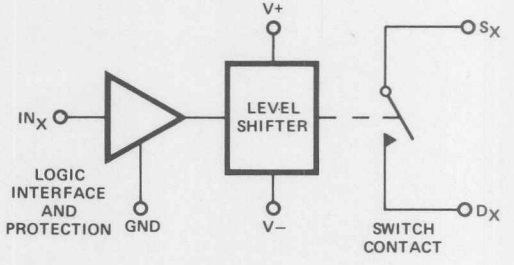
LOGIC	SWITCH
0	ON
1	OFF



ORDER NUMBER:
DG309CJ
See Package 8

SWITCHES ARE SHOWN IN THE LOGIC "1" INPUT STATE

FUNCTIONAL DIAGRAM (typical switch)



20 mA, whichever occurs first.

Current, Any Terminal
(Except S or D). 30 mA
Current, S or D, Continuous 20 mA
Pulsed 1 ms 10% Duty Cycle 100 mA

16 Pin Plastic DIP** 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

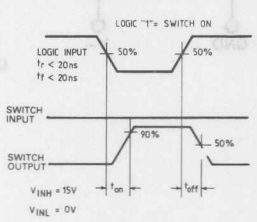
		CHARACTERISTIC		(Note 1) TYP 25°C	MAX LIMITS C SUFFIX 0°C	MAX LIMITS C SUFFIX 25°C	MAX LIMITS C SUFFIX 70°C	UNIT	TEST CONDITIONS V+ = +15 V, V− = −15 V, Gnd = 0 V	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15	V		
2	SWITCH	$r_{DS(ON)}$	Drain Source ON Resistance	70	100	100	125	Ω	V_D = 10 V, I_S = −1 mA	(Note 2)
3				60	100	100	125		V_D = −10 V, I_S = 1 mA	
4		$I_{S(off)}$	Source OFF Leakage Current	0.1		5	100	nA	V_S = +14 V, V_D = −14 V	(Note 2)
5				−0.1		−5	−100		V_S = −14 V, V_D = +14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	0.1		5	100		V_S = −14V, V_D = +14 V	
7				−0.1		−5	−100		V_S = +14V V_D = −14 V	
8		$I_{D(on)}$	Drain ON Leakage Current	0.1		5	200		V_D = V_S = + 14 V	(Note 2)
9				−0.1		−5	−200		V_D = V_S = − 14 V	
10	INPUT	I_{INH}	Input Current Input Voltage High	0.001		1		μA	V_{IN} = 15 V	
11		I_{INL}	Input Current Input Voltage Low	−0.001		−1			V_{IN} = 0 V	
12	DYNAMIC	t_{on}	Turn-ON Time	130		200		ns	See Switching Time Test Circuit	
13		t_{off}	Turn-OFF Time	90		150				
14		$C_{S(off)}$	Source OFF	8				pF	V_S = 0 V, V_{IN} = 15 V	
15		$C_{D(off)}$	Drain OFF Capacitance	8					V_D = 0 V, V_{IN} = 15 V	
16		$C_{D(on)}$ + $C_{S(on)}$	Channel ON Capacitance	22					V_D = V_S = 0 V, V_{IN} = 0 V	
17		OFF Isolation (Note 3)		78				dB	V_{IN} = 15 V, R_L = 1K Ω, C_L = 3 pF, V_S = 70m V rms, f = 500 kHz	
18	SUP	I+	Positive Supply Current	0.001		100		μA	V_{IN} = 15 V or 0 V	
19		I−	Negative Supply Current	−0.001		−100				

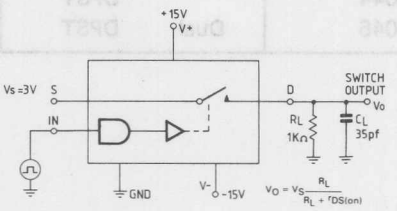
NOTES:

1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. V_{IN} = Input Voltage to perform proper function for logic '1' = 11V, for logic '0' = 3.5V
3. OFF Isolation = $20 \log_{10} \frac{|V_D|}{|V_S|}$ V_D = Output, V_S = Input to OFF Switch
4. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ICMF-B

SWITCHING TIME TEST CIRCUIT





Monolithic General Purpose CMOS Analog Switches

designed for . . .

- **Programmable Gain Amplifiers**
- **Analog Multiplexing**
- **Servo Control Switching**
- **Sampled Data Systems**
- **Synchronous Demodulators**

Siliconix

BENEFITS

- **Environmentally Rugged**
 - 44V Power Supply Rating
 - Static Protected Logic Inputs
 - Latchproof
- **Easily Interfaced**
 - TTL and CMOS Compatible without Pull Up Resistors
- **Reduces External Component Requirements**
 - Full Rail to Rail Analog Signal Range
 - No Diode Protection Required Between V_L and V+ for Power Supply Sequencing
- **Pin for Pin Compatible with**
 - IH5040 Family
 - HI5040 Family

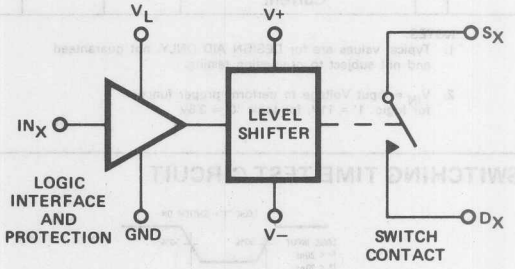
DESCRIPTION

The DG5040 through DG4045 series designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 50 ohms contact resistance and very high OFF resistance. True switch action takes place over the full analog signal range of ±15 volts, with Break-Before-Make operation to prevent momentary shorting of signal inputs.

FUNCTIONAL DESCRIPTION

PART NUMBER	TYPE	
DG5040		SPST
DG5041	Dual	SPST
DG5042		SPDT
DG5043	Dual	SPDT
DG5044		DPST
DG5045	Dual	DPST

FUNCTIONAL DIAGRAM (typical channel)

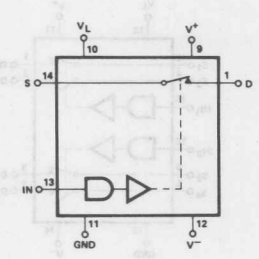


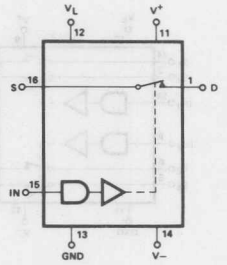
PIN CONFIGURATIONS

ALL SWITCHES SHOWN IN THE LOGIC "1" SWITCH STATE	FLAT PACK (L) SEE PACKAGE 5	CERDIP (K) OR PLASTIC (J) SEE PACKAGE 8 or 10	METAL CAN (A) SEE PACKAGE 2

SPST
DG5040

LOGIC	SWITCH
0	OFF
1	ON



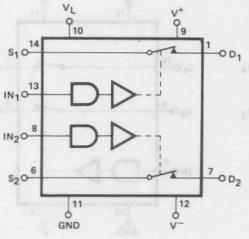


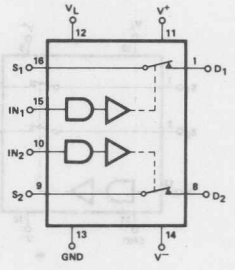
ORDER NUMBER: DG5040AL

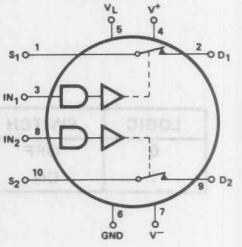
DG5040AK or DG5040CK or DG5040CJ

DUAL SPST
DG5041

LOGIC	SWITCH
0	OFF
1	ON







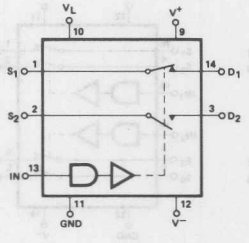
ORDER NUMBER: DG5041AL

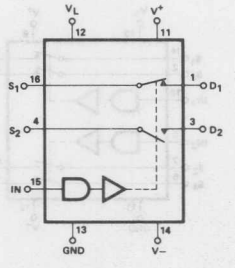
DG5041AK or DG5041CK or DG5041CJ

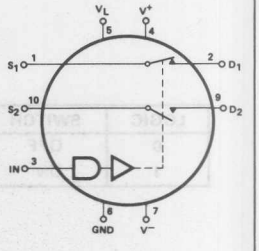
DG5041AA

SPDT
DG5042

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF







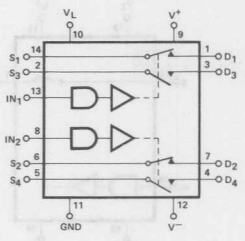
ORDER NUMBER: DG5042AL

DG5042AK or DG5042CK or DG5042CJ

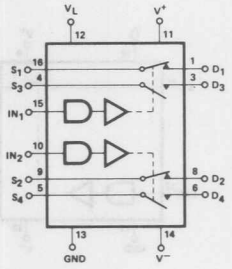
DG5042AA

DUAL SPDT
DG5043

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF



(DG191 EQUIVALENT)

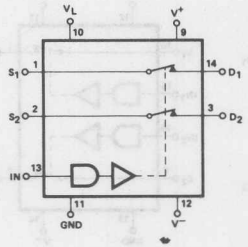


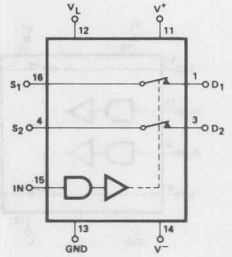
ORDER NUMBER: DG5043AL

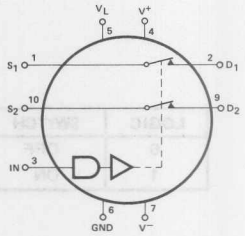
DG5043AK or DG5043CK
or DG5043CJ

DPST
DG5044

LOGIC	SWITCH
0	OFF
1	ON







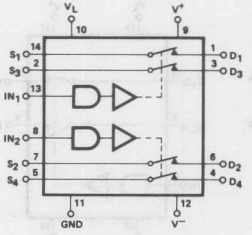
ORDER NUMBER: DG5044AL

DG5044AK or DG5044CK
or DG5044CJ

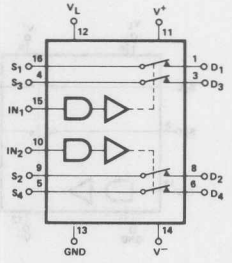
DG5044AA

DUAL DPST
DG5045

LOGIC	SWITCH
0	OFF
1	ON



(DG185 EQUIVALENT)



ORDER NUMBER: DG5045AL

DG5045AK or DG5045CK
or DG5045CJ

Digital inputs[5], V_S, V_D −2 V to (V^+ +2 V) or 30 mA, whichever occurs first.
Current, Any Terminal Except S or D 30 mA
Continuous Current, S or D. 30 mA
Peak Current, S or D (pulsed at 1 msec, 10% duty cycle max) 100 mA
Storage Temperature (A Suffix) −65 to 150°C
(C Suffix) −65 to 125°C

16 Pin DIP**** 900 mW
Flat Pak***** 900 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C.
****Derate 12 mW/°C above 75°C.
*****Derate 10 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		Characteristics		Max Limits A Suffix −55°C	A Suffix 25°C	A Suffix 125°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Unit	Test Conditions V+ = 15V, V− = −15V, V_L = 5V, GND = 0V	
1		V_{ANALOG}	Min. Analog Signal Handling Capability		±15	±15		±15	±15	V		
2	SWITCH	$r_{DS(on)}$[3]	Drain Source ON Resistance	50	50	75	50	50	75	Ω	V_D = 10V, I_S = −10 mA	Note 1
3				50	50	75	50	50	75		V_D = −10V, I_S = −10 mA	
4		$I_{S(off)}$[3]	Source OFF Leakage Current		1	100		1	100	nA	V_S = 14V, V_D = −14V	
5					−1	−100		−1	−100		V_S = −14V, V_D = 14V	
6		$I_{D(off)}$[3]	Drain OFF Leakage Current		1	100		1	100		V_S = −14V, V_D = 14V	
7					−1	−100		−1	−100		V_S = 14V, V_D = −14V	
8		$I_{D(on)}$[3]	Drain ON Leakage Current		2	200		2	200		V_S = V_D = 14V	
9					−2	−200		−2	−200		V_S = V_D = −14V	
10	INPUT	I_{INH}[3]	Input Current, Input Voltage High		±1	±1		±1	±1	µA	V_{INH} = 2.0V	
11		I_{INL}[3]	Input Current, Input Voltage Low		±1	±1		±1	±1		V_{INL} = 0.8V	
12	DYNAMIC	t_{on}[4]	Turn-ON Time		1000			1200		ns	V_S = ±10V, R_L = 1KΩ, C_L = 35 pF	Note 2
13		t_{off}[4]	Turn-OFF Time		500			700				
14		Q	Charge Injection	3 Typical						mV	C_L = 10,000 pF, R_{GEN} = 0Ω, V_{GEN} = 0V	
15		$C_{S(off)}$	Source OFF Capacitance	15 Typical						pF	V_S = V_D = 0V, f = 1 MHz	Note 1
16		$C_{D(off)}$	Drain OFF Capacitance	17 Typical								
17		$C_{D(on)}$ + $C_{S(on)}$	Channel ON Capacitance	45 Typical								
18		OIRR	OFF Isolation	75 Typical						dB	Z_L = 75Ω, V_S = 2 Vpp, f = 1 MHz	
19		CCRR	Interchannel Crosstalk Isolation	89 Typical								
20	SUPPLY	I_{+}[3]	Positive Supply Current	300	300	300	300	300	300	µA	V_{IN} = 0V or 2.4V	
21		I_{-}[3]	Negative Supply Current	−300	−300	−300	−300	−300	−300			
22		I_L[3]	Logic Supply Current	300	300	300	300	300	300			
23		I_{GND}	Ground Current	−300	−300	−300	−300	−300	−300			

ICMK–A, B

NOTES:

1: V_{IN} = Input voltage to perform proper function.
For Logic "1" — V_{INH} = 2.0 V
For Logic "0" — V_{INL} = 0.8 V

2: See Switching Time Test Circuit.

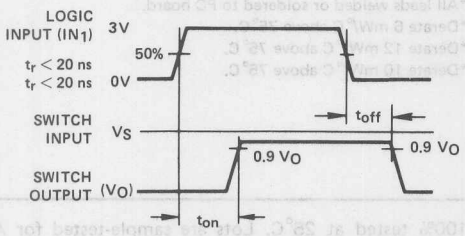
3: Limits of these paramaters are tested 100% at 25 °C and 125°C for "/883" devices.

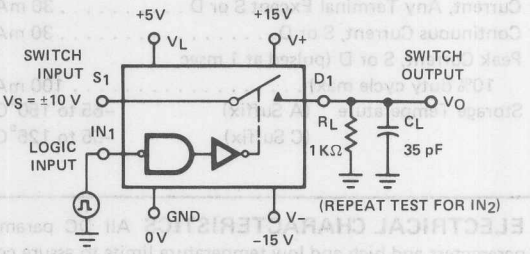
4: For "/883" devices these parameters are 100% tested at 25°C.

5: Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

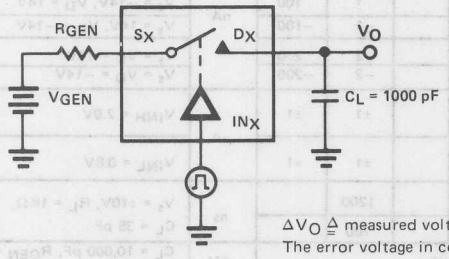


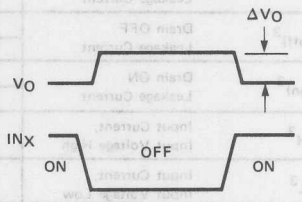


Note: Logic input waveform is inverted for switches that have the opposite logic sense control.

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

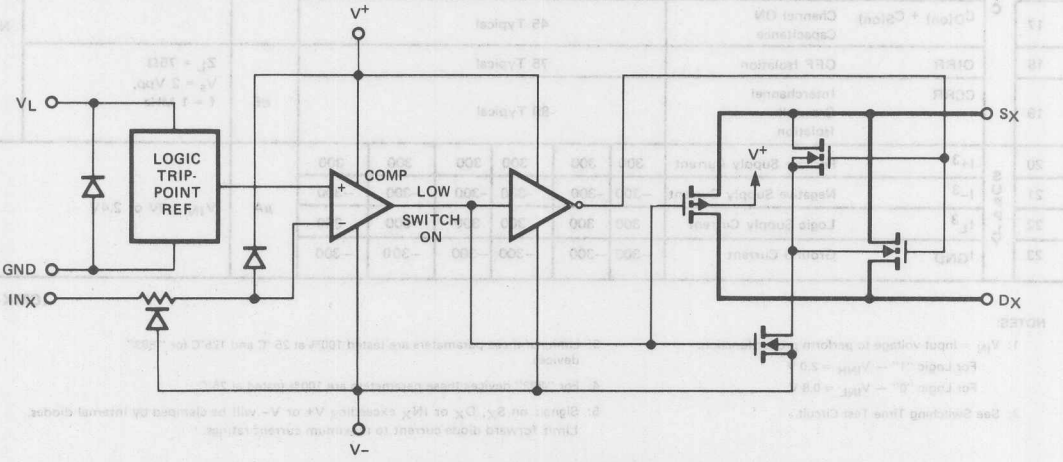
CHARGE INJECTION TEST CIRCUIT





$\Delta V_O \triangleq$ measured voltage error due to charge injection.
The error voltage in coulombs is $\Delta Q = C_L \times \Delta V_O$.

SCHEMATIC DIAGRAM (typical channel)



Monolithic SPST MOS Switch with Driver

Siliconix

designed for . . .

- **Switching Analog Signals such as Reference Signals**

BENEFITS

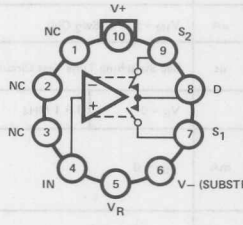
- **Reduces External Component Requirements**
 - Internal Zener Diodes Protect All MOS Gates
- **Easily Interfaced**
 - TTL and DTL Integrated Logic

DESCRIPTION

The SI3002 contains two P-channel MOS field-effect transistors designed to function as single-pole double-throw electronic switches. A level-shifting driver enables a low-level input (0.8 to 2 V) to control the ON-OFF state of the switches. In the ON state, each switch will conduct current equally well in either direction. In the OFF state the switches will block voltages up to 20 V peak-to-peak. With logic "0" at the driver input, a common drain (D) is connected through an ON switch to source (S_1). With logic "1" at the input, "D" is connected to S_2. Switch action is make-before-break.

PIN CONFIGURATIONS

Metal Can Package

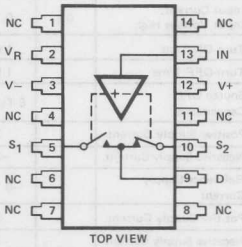


TOP VIEW

LOGIC	SW 1	SW 2
0	ON	OFF
1	OFF	ON

ORDER NUMBER: Si3002AA
SEE PACKAGE 2

Dual-In-Line Package

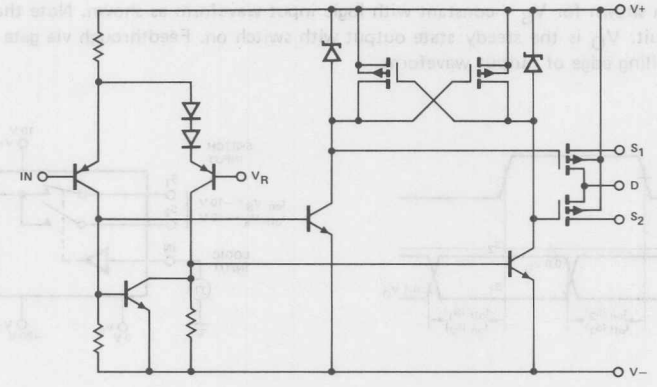


TOP VIEW

ORDER NUMBER: Si3002BP
SEE PACKAGE 11

LOGIC STATES ARE FOR LOGIC "1" INPUT
(POSITIVE LOGIC)

SCHEMATIC DIAGRAM



V_D to V−	36 V
V_S to V−	36 V
V_D to V_S	±25 V
V_{IN} to V_R	±6 V
Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C

Metal Can**	450 mW
14 Pin DIP***	825 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 6 mW/°C above 75°C.

***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

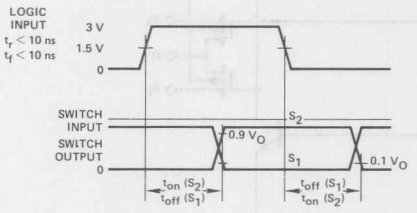
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX −20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 10 V, V− = −20 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	100	100	150	100	100	150	Ω	V_D = 10 V	I_S = −1 mA; V_{INL} = 0.8 V (Sw_1 ON), V_{INH} = 2.0 V (Sw_2 ON)
2	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	150	150	250	150	150	250	Ω	V_D = 0	I_S = −1 mA; V_{INL} = 0.8 V (Sw_1 ON), V_{INH} = 2.0 V (Sw_2 ON)
3	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	400	400	500	400	400	500	Ω	V_D = −10 V	I_S = −1 mA; V_{INL} = 0.8 V (Sw_1 ON), V_{INH} = 2.0 V (Sw_2 ON)
4	SWITCH	$I_{S(off)}$	Source OFF Leakage Current		−1	−1000		−5	−100	nA	V_S = −10 V, V_D = 10 V	V_{INL} = 0.8 V (Sw_1 ON), V_{INH} = 2.0 V (Sw_2 ON)
5	SWITCH	$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−2000		−10	−200	nA	V_D = −10 V, I_S = 0	V_{INL} = 0.8 V (Sw_1 ON), V_{INH} = 2.0 V (Sw_2 ON)
6	INPUT	I_{INL}	Input Current, Input Voltage Low	−1.0	−0.8	−0.8	−1.0	−0.8	−0.8	mA	V_{IN} = 0 (Sw_1 ON)	
7	INPUT	I_{INH}	Input Current, Input Voltage High	0.1	0.1	10	0.1	0.1	10	µA	V_{IN} = 5.5 V (Sw_2 ON)	
8	DYN	t_{on}	Turn-ON Time		1.0			1.0		µs	See Switching Time Test Circuit	
9	DYN	t_{off}	Turn-OFF Time		1.5			1.5		µs	See Switching Time Test Circuit	
10	DYN	$C_{S(off)}$	Source OFF Capacitance		6 Typ*			6 Typ*			V_S = 0	f = 1 MHz
11	SUPPLY	I+	Positive Supply Current		3			3.5		mA	V_{IN} = 0	
12	SUPPLY	I−	Negative Supply Current		−3			−3		mA	V_{IN} = 0	
13	SUPPLY	I_R	Reference Supply Current		−0.1			−0.1		mA	V_{IN} = 0	
14	SUPPLY	I+	Positive Supply Current		3			3.5		mA	V_{IN} = 5 V	
15	SUPPLY	I−	Negative Supply Current		−3			−3		mA	V_{IN} = 5 V	
16	SUPPLY	I_R	Reference Supply Current		−1.5			−1.5		mA	V_{IN} = 5 V	

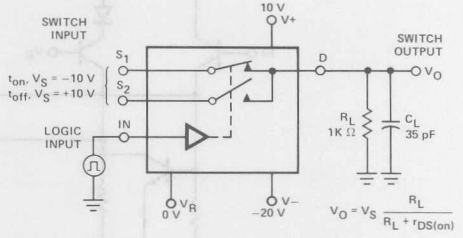
*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

CMBC

SWITCHING TIME TEST CIRCUIT

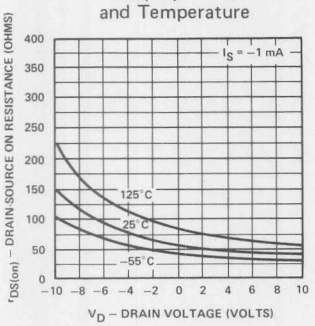
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



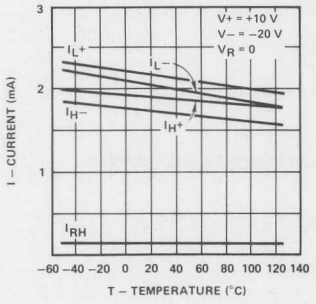


TYPICAL CHARACTERISTICS

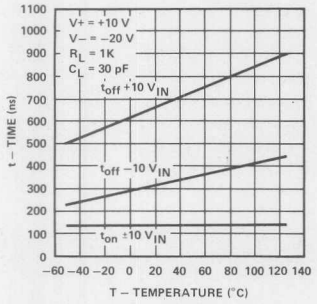
$r_{DS(on)}$ vs V_D and Temperature



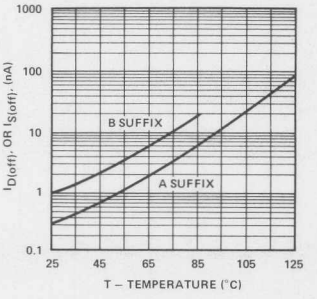
Supply Current vs Temperature



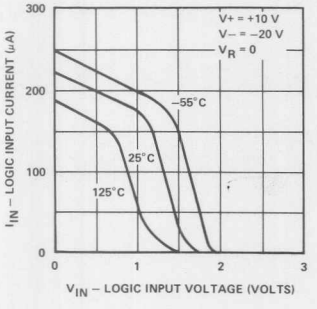
Switching Time vs Temperature



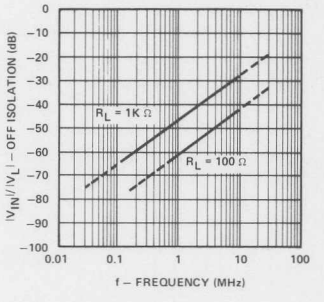
$I_{S(off)}$ vs Temperature



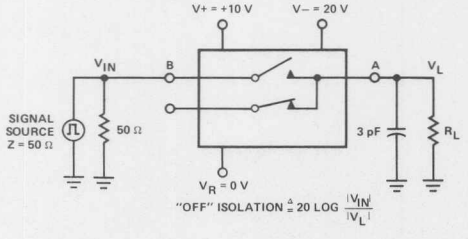
V_{IN} vs I_{IN} and Temperature



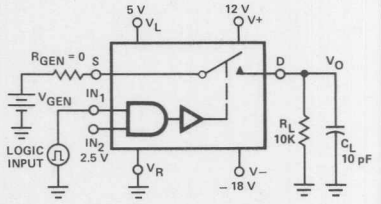
"OFF" Isolation vs R_L and Frequency



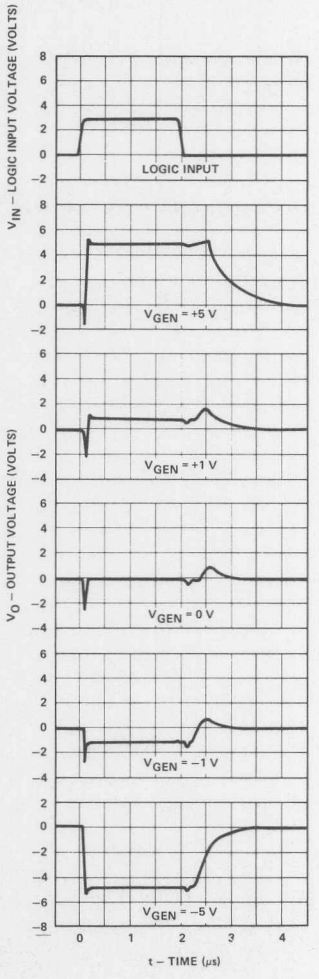
"OFF" Isolation Circuit



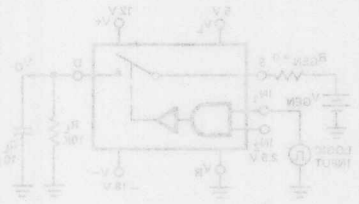
Typical delay, rise, fall, settling times, and switching transients in this circuit.



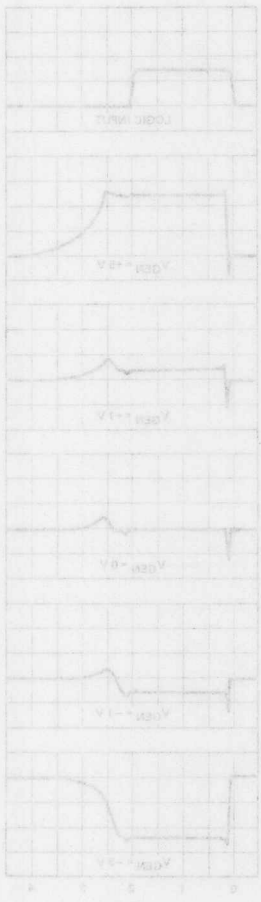
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If RGEN, RL or CL is increased, there will be proportional increases in rise and/or fall and RC times.



Siliconix

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Analog Multiplexers 4
Multi-Channel FETs 5
Linear 6
A/D Converters 7
D/A Converters 8
Die Process & Topography 9
Burn-In Pin Connections 10
Package Data 11
Appendices 12

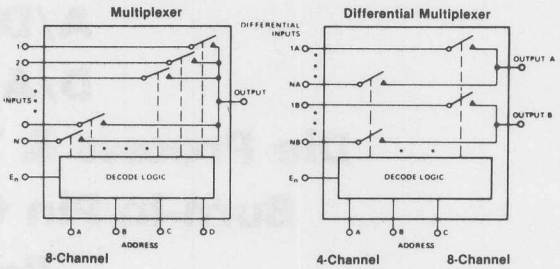
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ANALOG MULTIPLEXERS

Basic Part No.	Process Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$ (nA)	Transition Time (μsec) (Note 2)	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Supply Voltage (V) (+) Sup. V+	Supply Voltage (V) (−) Sup. V−	Comments
EIGHT CHANNEL MUX + ENABLE										
DG501	PMOS	+5 to −5	150-240	8	1.5	0.6	3.5	5	−20	Logic Pullup Resistors
DG503	PMOS	+10 to −10	150-800	8	1.5	0.6	8.5	10	−20	
DG508A	CMOS	+10 to −15	400	10	1.0	0.8	2.4	15	−15	Break-Before-Make
DG528	CMOS	+15 to −15	400	10	1.0	0.8	2.4	+15	−15	Latches On Inputs
SIXTEEN CHANNEL MUX + ENABLE										
DG506A	CMOS	+15 to −15	400	10	1.0	0.8	2.4	15	−15	Break-Before-Make
FOUR CHANNEL DIFFERENTIAL MUX + ENABLE										
DG509A	CMOS	+15 to −15	400	10	1.0	0.8	2.4	15	−15	Break-Before-Make
DG529	CMOS	+15 to −15	400	10	1.0	0.8	2.4	15	−15	Latches On Inputs
EIGHT CHANNEL DIFFERENTIAL MUX + ENABLE										
DG507A	CMOS	+15 to −15	400	5	1.0	0.8	2.4	+15	−15	Break-Before-Make

Switch Configurations



8-Channel 4-Channel 8-Channel

NOTES:
1. The devices shown in **boldface** are recommended parts for new designs.
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. $V_{REF} = 1.5$ V is used when supply voltages < ± 15 V are used. Not needed when supply voltages of ± 15 are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to + 10 V.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

8-Channel Multiplex Switch with Decode

Siliconix

designed for . . .

- **Multiplexing Signals**
- **Data Acquisition**

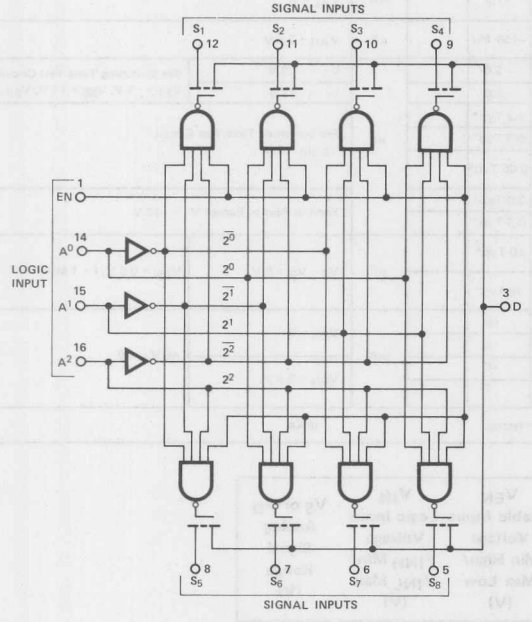
BENEFITS

- **Reduces Cross-Talk in Systems**
 - Break-Before-Make Switching
- **Easily Interfaced**
 - Pull-Up Resistors on Inputs for TTL Compatibility

DESCRIPTION

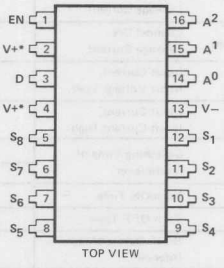
The DG501 is designed to function as a single-pole, 8-position (plus OFF) electronic switch. The function is implemented by using eight P-channel MOS field-effect transistors as analog switches. In the ON state, each switch will conduct current equally well in either direction and in the OFF state each switch will block voltages up to 10 V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 3-bit binary word plus an Enable-Inhibit input. The truth table shown below indicates the binary word required to select any one of the eight switch positions. Logic input levels "L" and "H" correspond to positive logic "0" and "1". Assuming supply voltages of +5 V and −20 V, logic "L" $\leq$ 0.6 V and logic "H" $\geq$ 3.5 V. "Pull-up" resistors are provided at each logic input to improve TTL compatibility. The rise and fall times of the drivers are designed to provide break-before-make switch action.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



ORDER NUMBERS: DG501AP OR DG501BP
SEE PACKAGE 12

DG501CJ
SEE PACKAGE 8

*Both V+ lines are internally connected, either one or both may be used. V+ common to substrate.

TRUTH TABLE

LOGIC INPUTS				CHANNEL
A^0	A^1	A^2	En	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

ABSOLUTE MAXIMUM RATINGS

V+ to V– –0.3, +30 V
V+ to V_A, V_{En} –0.3, +30 V
V+ to V_D or V_S –0.3, +30 V
V_D to V_S ±25 V
V_A, V_{En} to V– 30 V
V_D or V_S to V– 30 V
Current (Any Terminal) –20 mA
Storage Temperature (A & B Suffix) –65 to 150°C
(C Suffix) –65 to 125°C
Operating Temperature (A Suffix) –55 to 125°C
(B Suffix) –20 to 85°C
(C Suffix) 0 to 70°C
Power Dissipation*
16 Pin DIP** 900 mW
16 Pin Plastic DIP*** 470 mW

*Device mounted with all leads welded or soldered to PC board.
**Derate 12 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS DG501A –55°C	DG501A 25°C	DG501A 125°C	DG501B/C –20°C/0°C	DG501B/C 25°C	DG501B/C 85°C/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V– = –20 V, V+ = 5 V, V_{EN} = 3.5 V, V_{AL} = 0.6 V, V_{AH} = 3.5 V	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	150	150	225	150	150	200	Ω	V_D = 5 V	I_S = –1 mA, V– = –20 V
2				200	200	300	200	200	300		V_D = 0	
3				250	250	375	250	250	350		V_D = –5 V	
4				200	200	300	200	200	300		V_D = 5 V	I_S = –100 µA, V– = –15 V
5				250	250	375	250	250	350		V_D = 0	
6				600	600	900	600	800	900		V_D = –5 V	
7		$I_{S(off)}$	Source OFF Leakage Current		–1	–1000		–3	–150	nA	V_S = –5 V, V_D = 5 V	V_{EN} = 0.6 V
8		$I_{D(off)}$	Drain OFF Leakage Current		–8	–4000		–10	–500		V_D = –5 V, V_S = 5 V	
9		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		8	4000		10	500		$V_D = V_S$ = 5 V	
10	IN	I_{INL}	Input Current, Input Voltage Low		–1.2			–1.2		mA	V_{AL} = 0	
11		I_{INH}	Input Current, Input Current High		–150 Min			–150 Min		µA	V_{AH} = 3.5 V	
12	DYNAMIC	$t_{transition}$	Switching Time of Multiplexer		1.5			2.0		µs	V– = –20 V	See Switching Time Test Circuit V_{S1} = ±1 V, V_{S8} = ±1 V, V_{S2-7} = gnd
13					2.5			3.0			V– = –15 V	
14		t_{on}	Turn-ON Time		1.2 Typ*			1.2 Typ*			See Switching Time Test Circuit $V_{S(all)}$ = 1 V	
15		t_{off}	Turn-OFF Time		0.8 Typ*			0.8 Typ*				
16		t_{open}	Break-Before-Make Interval		0.05 Typ*			0.05 Typ*				
17		t_{on}	Turn-ON Time		2.0 Typ*			2.0 Typ*			Same as Above, Except V– = –15 V	
18		t_{off}	Turn-OFF Time		0.8 Typ*			0.8 Typ*				
19		$C_{S(off)}$	Source OFF Capacitance		10 Typ*			10 Typ*		pF	$V_S = V_D$ = 5 V	V_{EN} = 0.6 V, f = 1 MHz
20		$C_{D(off)}$	Drain OFF Capacitance		20 Typ*			20 Typ*				
21	SUPPLY	I–	Drain Supply Current		–6			–6		mA	V_{EN} = 0	All V_A = 0
22		I+	Source Supply Current		8			8				
23		I–	Drain Supply Current		–6			–6			V_{EN} = 3.5 V	
24		I+	Source Supply Current		7			7				

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

IPAA

APPLICATION HINTS*

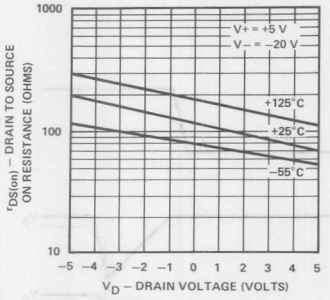
V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	V_{EN} Enable Input Voltage Min High/ Max Low (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Signal Range (V)
+5**	–20	3.5/0.6	3.5/0.6	–5 to +5
+5	–15	3.5/0.6	3.5/0.6	–5 to +5

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

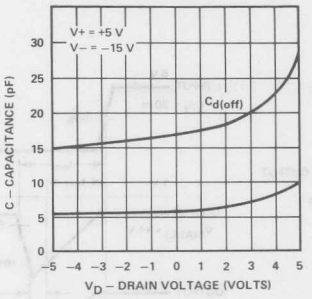
**Electrical parameters chart based on V+ = 5 V, V– = –20 V.

TYPICAL CHARACTERISTICS

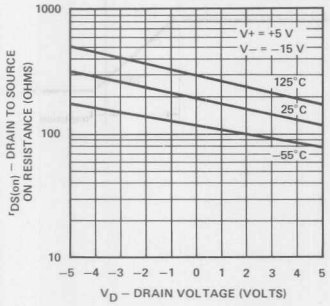
$r_{DS(on)}$ vs V_D and Temperature



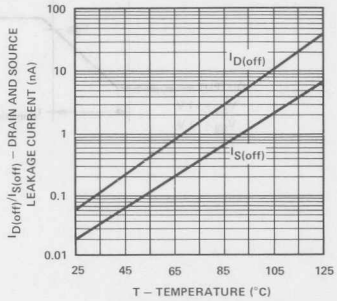
$C_{D(off)}$, $C_{S(off)}$ vs V_D



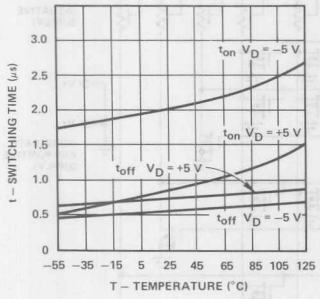
$r_{DS(on)}$ vs V_D and Temperature



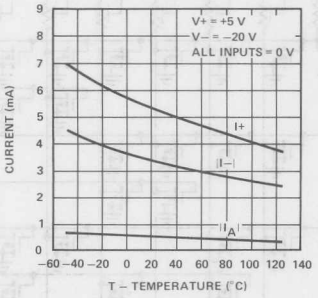
$I_{D(off)}/I_{S(off)}$ vs Temperature



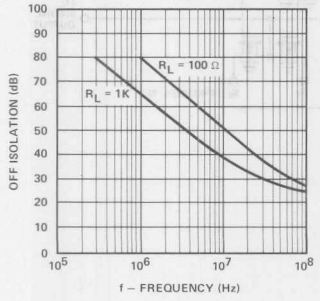
Switching Time vs Temperature

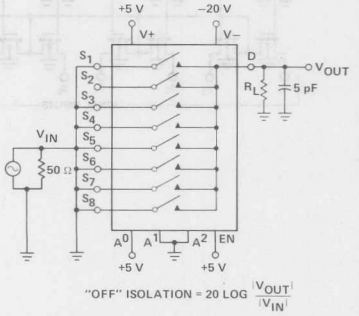


Supply Current vs Temperature

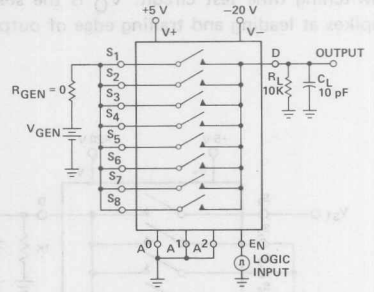


"OFF" Isolation vs R_L and Frequency

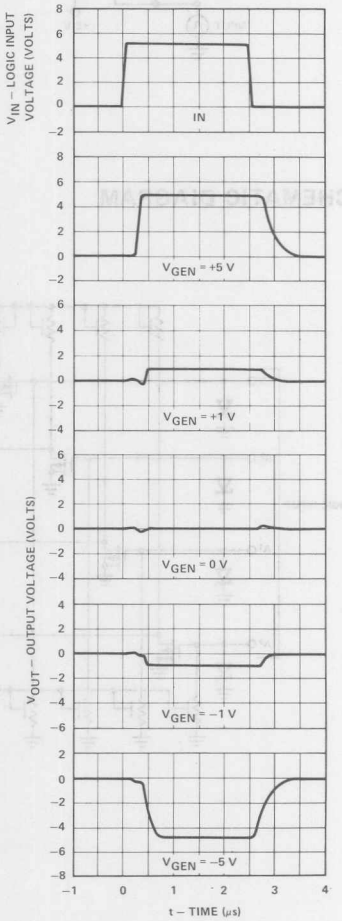


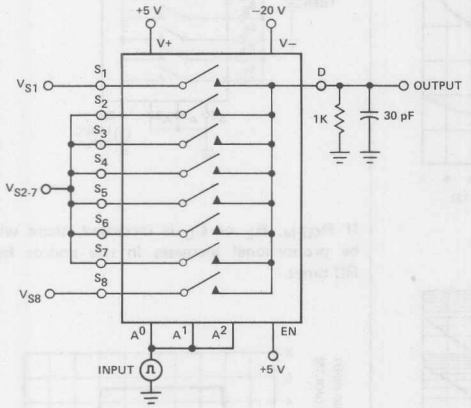


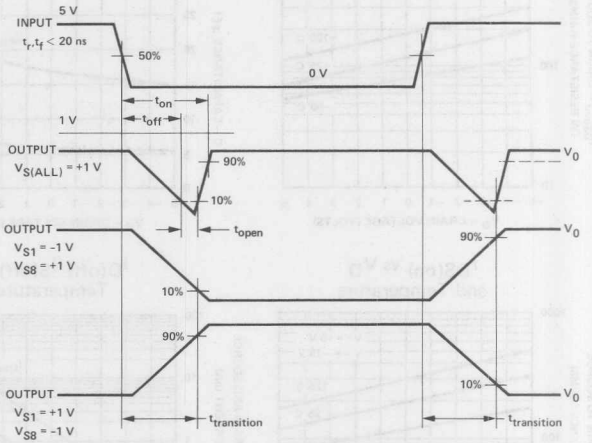
"OFF" ISOLATION = 20 LOG $\frac{|V_{OUT}|}{|V_{IN}|}$



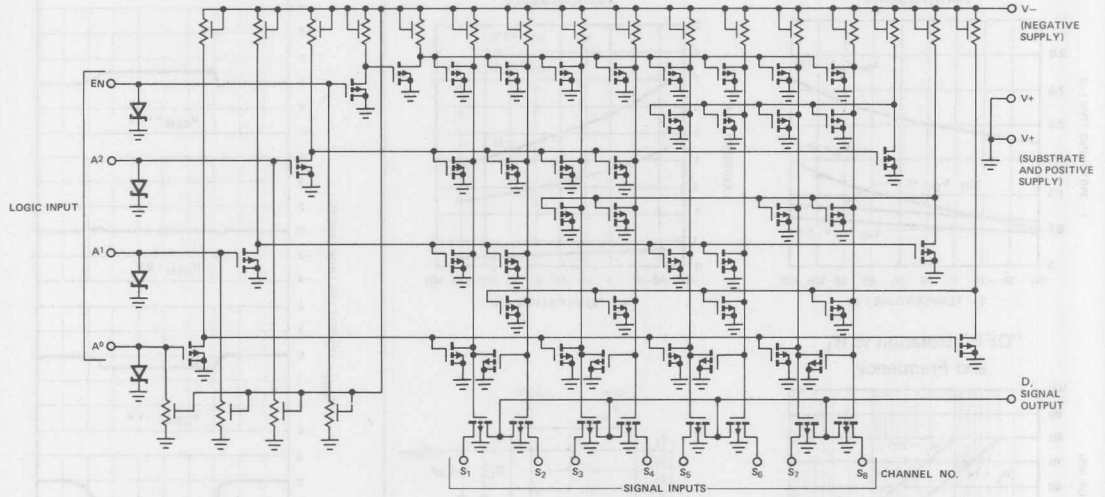
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.







SCHEMATIC DIAGRAM



8-Channel Multiplex Switch with Decode

Siliconix

designed for . . .

- **Multiplexing Signals**
- **Data Acquisition**

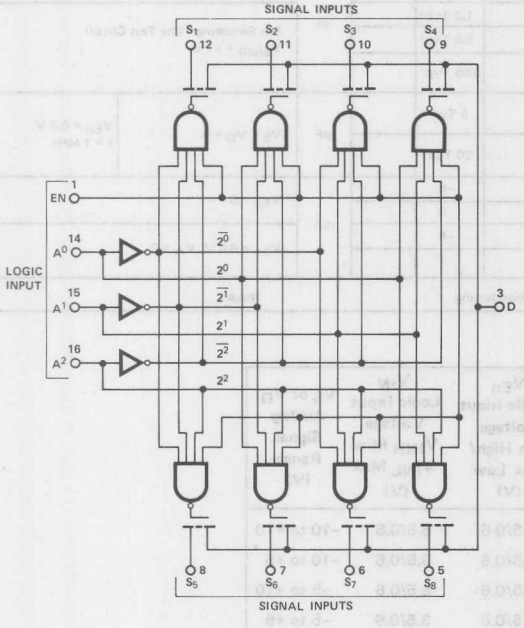
BENEFITS

- **Reduces Cross-Talk in Systems**
 - Break-Before-Make Switching

DESCRIPTION

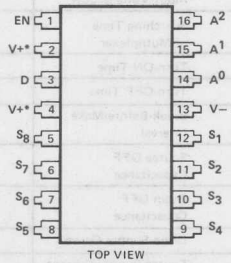
The DG503 is designed to function as a single-pole, 8-position (plus OFF) electronic switch. The function is implemented by using eight P-channel MOS field-effect transistors as analog switches. In the ON state, each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 3-bit binary word plus an Enable-Inhibit input. The truth table shown below indicates the binary word required to select any one of the eight switch positions. Logic input levels "L" and "H" correspond to positive logic "0" and "1". Assuming supply voltages of 10 and −20 V, logic "L" $\leq$ 0.6 V and logic "H" $\geq$ 8.5 V. The rise and fall times of the drivers are designed to provide break-before-make switch action.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

Dual In-Line Package



ORDER NUMBERS: DG503AP OR DG503BP
SEE PACKAGE 12

*Both V+ lines are internally connected, either one or both may be used. V+ common to substrate.

TRUTH TABLE

LOGIC INPUTS				CHANNEL
A^0	A^1	A^2	En	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

ABSOLUTE MAXIMUM RATINGS

V+ to V– –0.3, 33 V
V+ to V_A, V_{En} –0.3, 33 V
V+ to V_D or V_S –0.3, 33 V
V_D to V_S ±25 V
V_A, V_{En} to V– 33 V
V_D or V_S to V– 33 V

Current (Any Terminal) –20 mA
Storage Temperature (A & B Suffix) –65 to 150°C
Operating Temperature (A Suffix) –55 to 125°C
(B Suffix) –20 to 85°C
Power Dissipation* 900 mW

*All leads soldered or welded to PC board. Derate 12 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS A SUFFIX –55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX –20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V– = –20 V, V+ = 10 V, V_{En} = 8.5 V, V_{AL} = 0.6 V, V_{AH} = 8.5 V	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	150	150	225	150	150	200	Ω	V_D = 10 V	I_S = –1 mA
2				250	250	375	250	250	350		V_D = 0	
3				600	800	1250	600	800	1000		V_D = –10 V	I_S = –100 μA
4		$I_{S(off)}$	Source OFF Leakage Current		–2	–2000		–3	–150	nA	V_S = –10 V, V_D = 10 V	V_{En} = 0.6 V
5		$I_{D(off)}$	Drain OFF Leakage Current		–8	–4000		–10	–500		V_D = –10 V, V_S = 10 V	
6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		8	4000		10	500		V_D = V_S = 10 V	
7	IN	I_{INL}	Input Current, Input Voltage Low		–1			–1		μA	V_{AL} = 0	
8		$t_{transition}$	Switching Time of Multiplexer		1.5			2.0		μs	See Switching Time Test Circuit V_{S1} = ±1 V, V_{S8} = ∓1 V, V_{S2-7} = gnd	
9	DYNAMIC	t_{on}	Turn-ON Time		1.2 Typ*			1.2 Typ*			See Switching Time Test Circuit $V_{S(all)}$ = ±1 V	
10		t_{off}	Turn-OFF Time		0.8 Typ*			0.8 Typ*				
11		t_{open}	Break-Before-Make Interval		0.05 Typ*			0.05 Typ*				
12		$C_{S(off)}$	Source OFF Capacitance		5 Typ*			5 Typ*		pF	V_S = V_D = 0	V_{En} = 0.5 V, f = 1 MHz
13		$C_{D(off)}$	Drain OFF Capacitance		20 Typ*			20 Typ*				
14	SUPPLY	I–	Drain Supply Current		–6			–6		mA	V_{En} = 0	
15		I+	Source Supply Current		8			8				
16		I–	Drain Supply Current		–6			–6			V_{En} = 8.5 V, V_A = 0	
17		I+	Source Supply Current		7			7				

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

IPAA

APPLICATION HINTS*

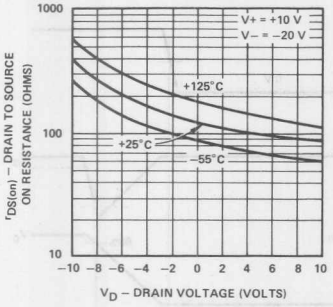
V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	V_{En} Enable Input Voltage Min High/ Max Low (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Signal Range (V)
+10**	–20	8.5/0.6	8.5/0.6	–10 to +10
+5	–20	3.5/0.6	3.5/0.6	–10 to +5
+10	–15	8.5/0.6	8.5/0.6	–5 to +10
+5	–15	3.5/0.6	3.5/0.6	–5 to +5

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

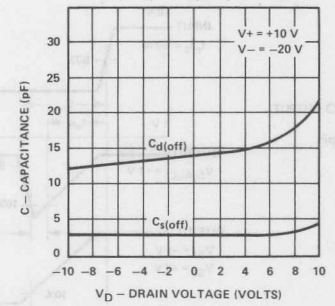
**Electrical parameters chart based on V+ = +10 V, V– = - 20 V.

TYPICAL CHARACTERISTICS

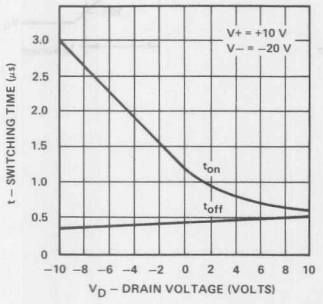
$r_{DS(on)}$ vs V_D and Temperature



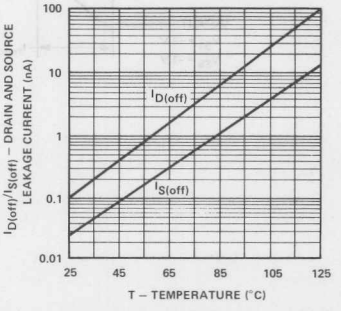
$C_{D(off)}$, $C_{S(off)}$ vs V_D



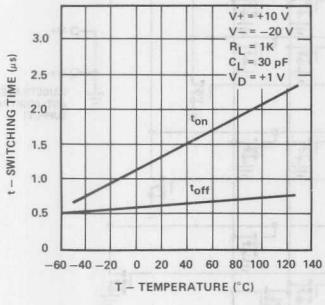
Switching Time vs V_D



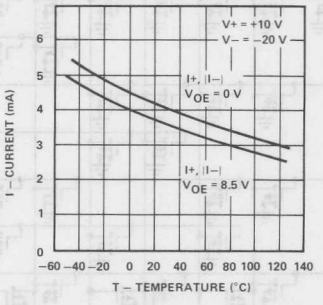
$I_{D(off)}/I_{S(off)}$ vs Temperature



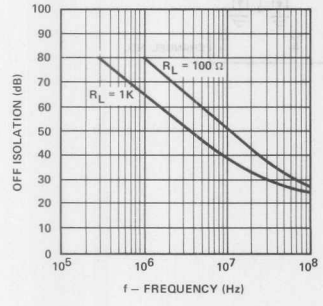
Switching Time vs Temperature

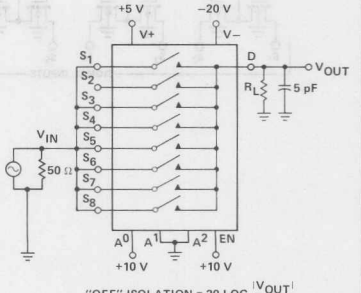


Supply Current vs Temperature

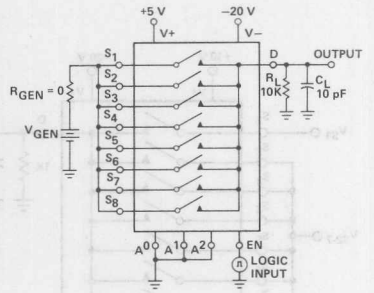


"OFF" Isolation vs R_L and Frequency

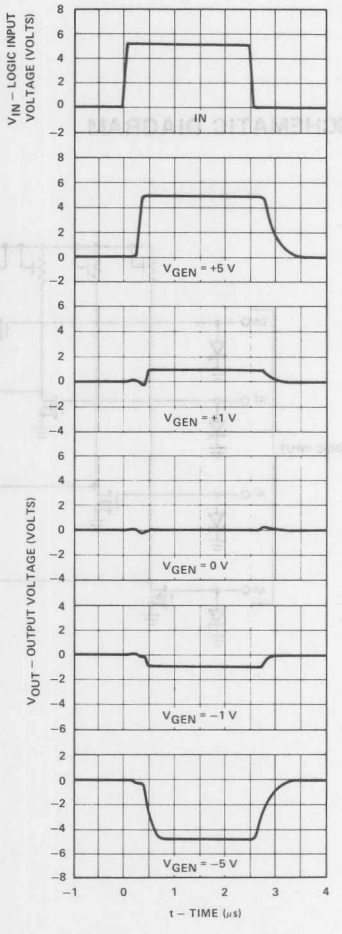


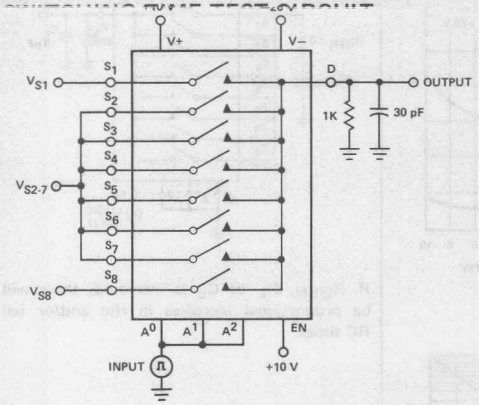


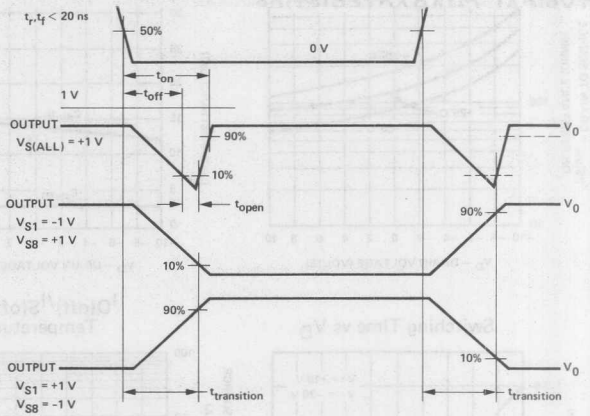
"OFF" ISOLATION = 20 LOG $\frac{|V_{OUT}|}{|V_{IN}|}$



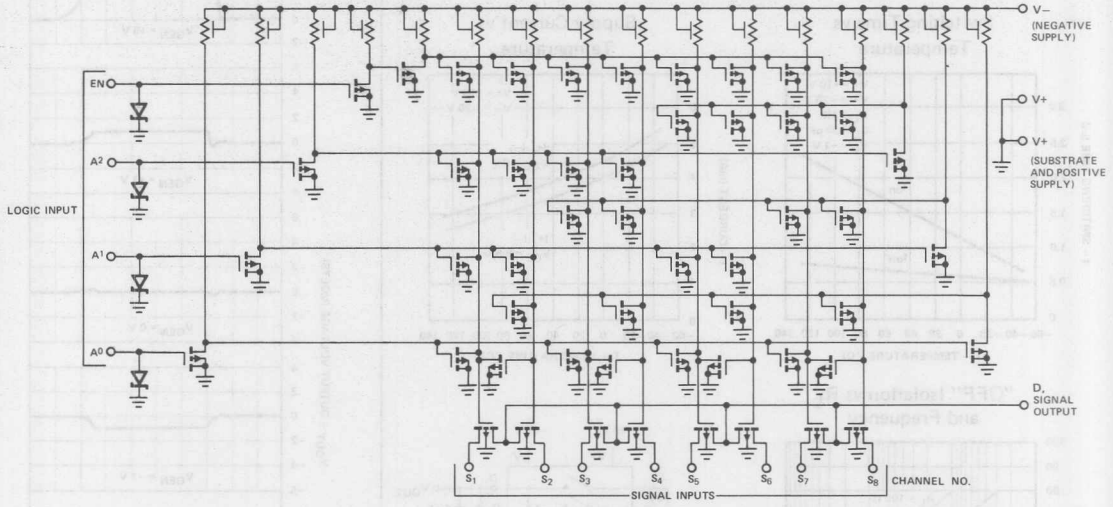
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.







SCHEMATIC DIAGRAM



Differential 8-Channel/ 16-Channel CMOS Analog Multiplexer *designed for...*

- **Data Acquisition Systems**
- **Multiplexing Reference Signals**
- **Communication Systems**

Siliconix

BENEFITS

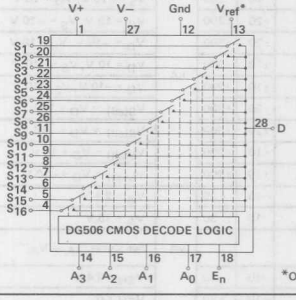
- **Environmentally Rugged**
 - Latchproof CMOS
- **Easily Interfaced**
 - TTL, DTL and CMOS Direct Control Over Military Temperature Range
- **Low Stand-By Power**
 - 36 mW Typical Stand-By Power
- **Reduces System Cross-Talk**
 - Break-Before-Make Switching Action
- **Reduces External Component Requirements**
 - ±15 V Analog Signal Range with ±15 V Supplies

DESCRIPTION

The DG506 is a single-pole 16-position (plus OFF) electronic switch array [DG507 is a double-pole 8-position (plus OFF)] which employs 16 pairs of complementary MOS (CMOS) field-effect transistors designed to function as analog switches. In the ON condition each switch will conduct current in either direction, and in the OFF condition each switch will block voltages up to 30 volts peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 4-bit binary word (DG507 by a 3-bit binary word) input plus an Enable-Inhibit input. The truth table below shows the binary word required to select any one of the 16 switch positions, provided a positive logic "1" is present at the Enable Input. With logic "0" at the Enable input all switches will be OFF. The logic decoder and the Enable inputs will recognize voltages between 0 and 0.8 V as logic "0" voltages, and voltages between 2.4 and 15 V as logic "1" voltages. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make.
For new designs, use the DG506A and DG507A.

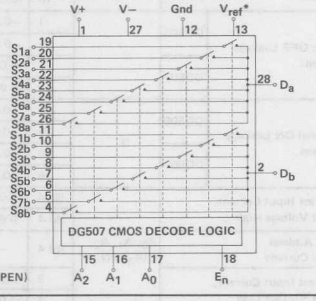
FUNCTIONAL DIAGRAMS

16 Channel MUX DG506



*OPTIONAL (NORMALLY LEFT OPEN)

8 Channel MUX DG507

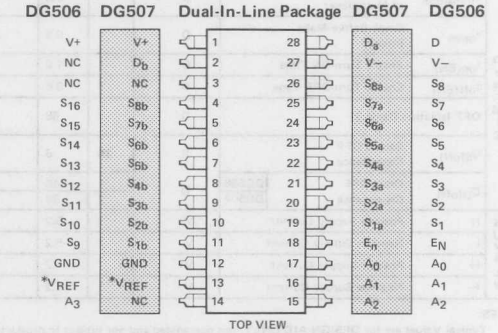


TRUTH TABLE

A_3	A_2	A_1	A_0	E_n	ON SWITCH	
X	X	X	X	0	NONE	DG507 / DG506
0	0	0	0	1	1	
0	0	0	1	1	2	
0	0	1	0	1	3	
0	0	1	1	1	4	
0	1	0	0	1	5	
0	1	0	1	1	6	
0	1	1	0	1	7	
0	1	1	1	1	8	
1	0	0	0	1	9	
1	0	0	1	1	10	
1	0	1	0	1	11	
1	0	1	1	1	12	
1	1	0	0	1	13	
1	1	0	1	1	14	
1	1	1	0	1	15	
1	1	1	1	1	16	

Logic "0" = $V_{AL} \leq 0.8V$, Logic "1" = $V_{AH} \geq 2.4$ V, Screen is DG507

PIN CONFIGURATIONS



TOP VIEW
*OPTIONAL (NORMALLY LEFT OPEN)
V+ COMMON TO SUBSTRATE

ORDER NUMBERS:

DG506AR OR DG506BR	DG506CJ
DG507AR OR DG507BR	DG507C
SEE PACKAGE 13	SEE PACKAGE 14

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, En, or V_{REF}) to Ground −0.3 V, V+
V_S or V_D to V+ 0, −32 V
V_S or V_D to V− 0, 32 V
V+ to Ground 16 V
V− to Ground −16 V
Current (Any Terminal, Except S or D) 30 mA
Continuous Current, S or D 20 mA
Peak Current, S or D
(Pulsed at 1 msec, 10% Duty Cycle Max) 40 mA
Storage Temperature (A & B Suffix) −65 to 150°C
(C Suffix) −65 to 125°C

Operating Temperature (A Suffix) −55 to 125°C
(B Suffix) −20 to 85°C
(C Suffix) 0 to 70°C
Power Dissipation (Package)*
28 Pin DIP** 1200 mW
28 Pin Plastic DIP*** 625 mW

*All leads soldered or welded to PC board.
**Derate 16 mW/°C above 75°C.
***Derate 8.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS

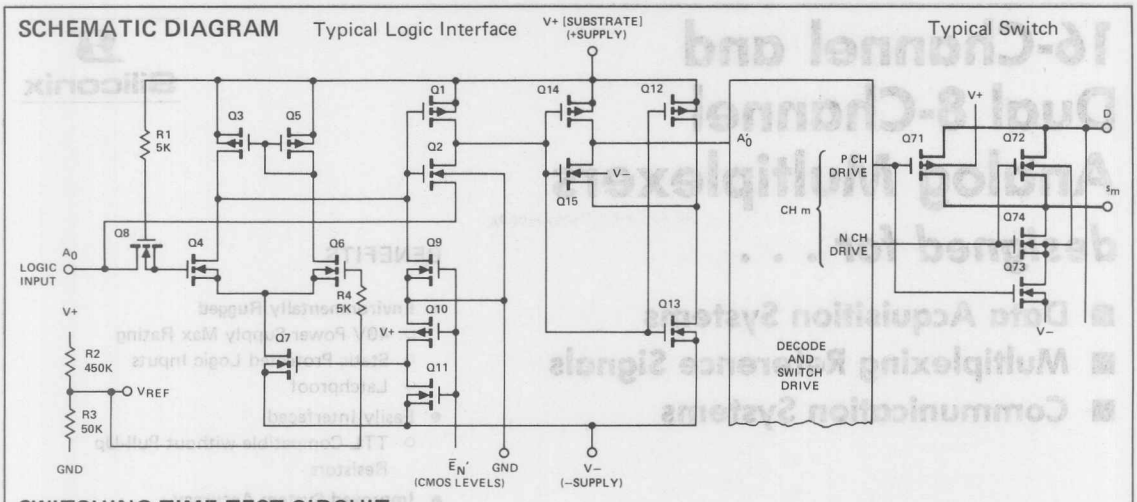
All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC			MEASURED TERMINAL	NO. TESTS PER TEMP	(Note 1) TYP 25°C	MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX −20/0°C	B/C SUFFIX 25°C	B/C SUFFIX 85/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Ground = 0, V_{REF} = Open (Note 4)	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability				±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2		$r_{DS(on)}$	Drain Source ON Resistance		S to D	16	270	400	400	500	450	450	550	Ω	V_D = 10 V, I_S = −200 µA	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V
3						16	230	400	400	500	450	450	550		V_D = −10 V, I_S = −200 µA	
4		$\Delta r_{DS(on)}$	Greatest Change in Drain-Source ON Resistance Between Channels		S to D	16	6							%	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)\,MAX} - r_{DS(on)\,MIN}}{r_{DS(on)\,AVE}}\right)$ −10 V ≤ V_S ≤ 10 V	
5	SWITCH	$I_{S(off)}$	Source OFF Leakage Current		S	16	−0.005		±1	±50		±5	±50	nA	V_S = 10 V, V_D = −10 V	V_{EN} = 0
6						16	−0.005		±1	±50		±5	±50		V_S = −10 V, V_D = 10 V	
7		$I_{D(off)}$	Drain OFF Leakage Current	DG506	D	1	−0.03		±10	±300		±20	±300		V_D = 10 V, V_S = −10 V	
8						1	−0.03		±10	±300		±20	±300		V_D = −10 V, V_S = 10 V	
9				DG507		2	−0.015		±5	±200		±10	±200		V_D = 10 V, V_S = −10 V	
10						2	−0.015		±5	±200		±10	±200		V_D = −10 V, V_S = 10 V	
11		$I_{D(on)}$ (Note 2)	Channel ON Leakage Current	DG506	D	16	−0.06		±10	±300		±20	±300		$V_{S(all)}$ = V_D = 10 V	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V
12						16	−0.06		±10	±300		±20	±300		$V_{S(all)}$ = V_D = −10 V	
13				DG507		16	−0.03		±5	±200		±10	±200		$V_{S(all)}$ = V_D = 10 V	
14						16	−0.03		±5	±200		±10	±200		$V_{S(all)}$ = V_D = −10 V	
15	INPUT	I_{AH}	Address Input Current, Input Voltage High		A_0, A_1, A_2, (A_3) EN	(5) 4	−0.002		−10	−30		−10	−30	µA	V_A = 2.4 V	
16						(5) 4	0.006		10	30		10	30		V_A = 15 V	
17		$I_{A(peak)}$	Peak Address Input Current			(5) 4	−75								See Curve "I_A vs V_A"	
18		I_{AL}	Address Input Current, Input Voltage Low			3	−0.002		−10	−30		−10	−30		V_{EN} = 2.4 V	All V_A = 0
19						1	−0.002		−10	−30		−10	−30		V_{EN} = 0	
20	DYNAMIC	$t_{transition}$	Switching Time of Multiplexer		D		0.6		1					µs	See Figure 1	
21		t_{open}	Break-Before-Make Interval		D		0.2									
22		$t_{on(EN)}$	Enable Turn-ON Time		D	1	1.0		1.5						See Figure 2	
23		$t_{off(EN)}$	Enable Turn-OFF Time		D	1	0.4		1							
24		OFF Isolation (Note 3)			D		68							dB	V_{EN} = 0, R_L = 1K Ω, C_L = 15 pF V_S = 7 VRMS, f = 500 KHz	
25		$C_{S(off)}$	Source OFF Capacitance		S	16	6							pF	V_S = 0	V_{EN} = 0, f = 140 KHz
26		$C_{D(off)}$	Drain OFF Capacitance	DG506	D	1	45								V_D = 0	
27				DG507		2	23									
28	SUPPLY	I+	Positive Supply Current		V+	1	5.2		10				10	mA	V_{EN} = 5 V	All V_A = 0
29		I−	Negative Supply Current		V−	1	−5.2		−10				−10			
30		I+	Positive Supply Current		V+	1	1.2		2.5				2.5		V_{EN} = 0	
31		I−	Negative Supply Current		V−	1	−1.2		−2.5				−2.5			

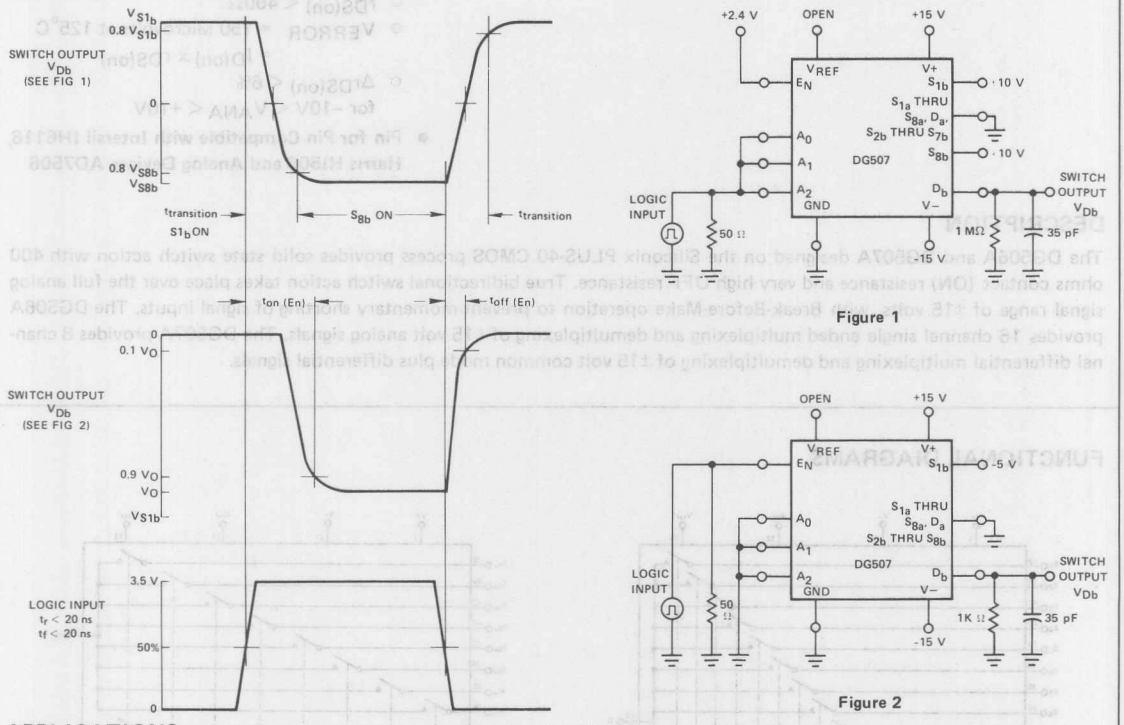
NOTES:
1. Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. OFF Isolation $\triangleq 20 \log \frac{|V_D|}{|V_S|}$ V_S = input to "OFF" switch V_D = output due to V_S.
4. Functional operation is possible for supply voltages less than 15 V, but the input logic threshold will shift. For V+ = |V−| < 10 V, 1.5 V may be applied to the V_{REF} terminal. The V_{REF} terminal has $R_{IN} \cong 45K\ \Omega$ (See the applications section.)

DG506 ICXBA
DG507 ICXBB

SCHEMATIC DIAGRAM



SWITCHING TIME TEST CIRCUIT



APPLICATIONS

Application Hints*

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{REF} Reference Pin Connection (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
+15**	−15	Open	2.4/0.8	−15 to +15
+12	−12	Open or 1.4 V	2.4/0.8	−12 to +12
+10	−10	1.4 V	2.4/0.8	−10 to +10
+8***	−8	1.4 V	2.4/0.8	−8 to +8

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics chart based on V+ = +15 V, V− = −15 V, V_{REF} = Open.

***Operation below ±8 V is not recommended.

Analog Multiplexers

designed for . . .

- **Data Acquisition Systems**
- **Multiplexing Reference Signals**
- **Communication Systems**

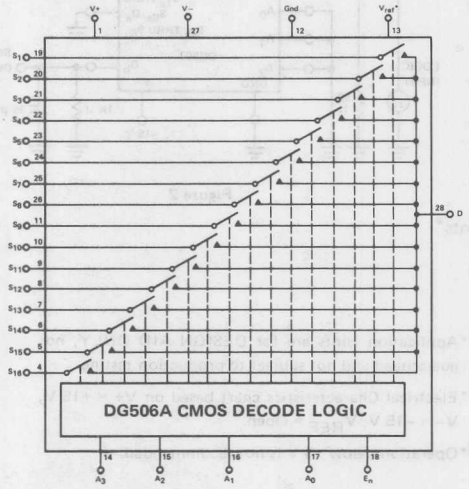
BENEFITS

- **Environmentally Rugged**
 - 40V Power Supply Max Rating
 - Static Protected Logic Inputs
 - Latchproof
- Easily Interfaced
 - TTL Compatible without Pull-Up Resistors
- **Improved System Accuracy**
 - $r_{DS(on)} < 400\Omega$
 - V_{ERROR} = 150 Microvolts at 125°C
 $= I_{D(on)} \times r_{DS(on)}$
 - $\Delta r_{DS(on)} < 6\%$
 for $-10V < V_{ANA} < +10V$
- **Pin for Pin Compatible with Intersil IH6116, Harris HI506 and Analog Devices AD7506**

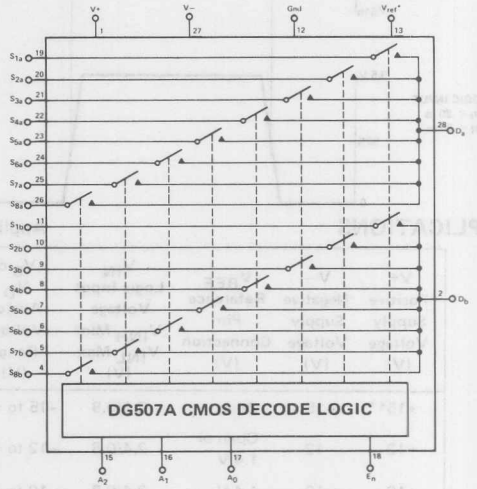
DESCRIPTION

The DG506A and DG507A designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 400 ohms contact (ON) resistance and very high OFF resistance. True bidirectional switch action takes place over the full analog signal range of ±15 volts, with Break-Before-Make operation to prevent momentary shorting of signal inputs. The DG506A provides 16 channel single ended multiplexing and demultiplexing of ±15 volt analog signals. The DG507A provides 8 channel differential multiplexing and demultiplexing of ±15 volt common mode plus differential signals.

FUNCTIONAL DIAGRAMS



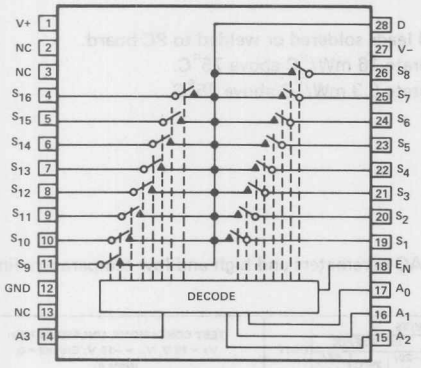
DG506A
16 CHANNEL SINGLE ENDED MULTIPLEXER



DG507A
DIFFERENTIAL 8 CHANNEL MULTIPLEXER

PIN CONFIGURATIONS

Dual-In-Line Package

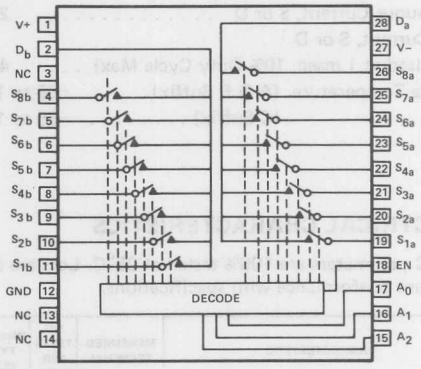


Top View

ORDER NUMBERS:
DG506AAR OR DG506ABR
SEE PACKAGE 13

DG506ACJ
SEE PACKAGE 14

Dual-In-Line Package



Top View

ORDER NUMBERS:
DG507AAR OR DG507ABR
SEE PACKAGE 13

DG507ACJ
SEE PACKAGE 14

TRUTH TABLES

DG506A

A_3	A_2	A_1	A_0	E_n	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG507A

A_2	A_1	A_0	E_n	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} \leq 0.8V$, Logic "1" = $V_{AH} \geq 2.4V$

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–

V+ 44 V
GND 25 V
Digital inputs[5] V_S, V_D −2 V to (V^+ +2 V) or 20 mA, whichever occurs first.
Current (Any Terminal, Except S or D) 30 mA
Continuous Current, S or D 20 mA
Peak Current, S or D
(Pulsed at 1 msec, 10% Duty Cycle Max) 40 mA
Storage Temperature (A & B Suffix) −65 to 150°C
(C Suffix) −65 to 125°C
Operating Temperature (A Suffix) −55 to 125°C
(B Suffix) −20 to 85°C
(C Suffix) 0 to 70°C
Power Dissipation (Package)*
28 Pin DIP** 1200 mW
28 Pin Plastic DIP*** 625 mW

*All leads soldered or welded to PC board.
**Derate 16 mW/°C above 75°C.
***Derate 8.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC			MEASURED TERMINAL	NO. TESTS PER TEMP.	(Note 1) TYP 25°C	MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX −20/0°C	B/C SUFFIX 25°C	B/C SUFFIX 85/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Ground = 0, (Note 4)	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability				±15		±15	±15		±15	±15	V		
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance		S to D	16	270	400	400	500	450	450	550	Ω	V_D = 10 V, I_S = −200 μA	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4V V_{EN} = 2.4 V
3						16	230	400	400	500	450	450	550		V_D = −10 V, I_S = −200 μA	
4		$\Delta r_{DS(on)}$	Greatest Change in Drain-Source ON Resistance Between Channels		S to D	16	6							%	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)\ MAX} - r_{DS(on)\ MIN}}{r_{DS(on)\ AVE}}\right)$ −10 V ≤ V_S ≤ 10 V	
5		$I_{S(off)}$	Source OFF Leakage Current		S	16	0.002		±1	±50		±5	±50	nA	V_S = 10 V, V_D = −10 V	V_{EN} = 0
6						16	−0.005		±1	±50		±5	±50		V_S = −10 V, V_D = 10 V	
7		$I_{D(off)}$	Drain OFF Leakage Current	DG506A	D	1	0.020		±10	±300		±20	±300		V_D = 10 V, V_S = −10 V	
8						1	−0.03		±10	±300		±20	±300		V_D = −10 V, V_S = 10 V	
9				DG507A		2	0.007		±5	±200		±10	±200		V_D = 10 V, V_S = −10 V	
10						2	−0.015		±5	±200		±10	±200		V_D = −10 V, V_S = 10 V	
11		$I_{D(on)}$[2]	Channel ON Leakage Current	DG506A	D	16	0.03		±10	±300		±20	±300		$V_{S(all)}$ = V_D = 10 V	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V V_{EN} = 2.4 V
12						16	−0.06		±10	±300		±20	±300		$V_{S(all)}$ = V_D = −10 V	
13				DG507A		16	0.015		±5	±200		±10	±200		$V_{S(all)}$ = V_D = 10 V	
14						16	−0.03		±5	±200		±10	±200		$V_{S(all)}$ = V_D = −10 V	
15	INPUT	I_{AH}	Address Input Current, Input Voltage High		A_0, A_1, A_2, (A_3) EN	(5) 4	−0.002		−10	−30		−10	−30	μA	V_A = 2.4 V	
16						(5) 4	0.006		10	30		10	30		V_A = 15 V	
17		I_{AL}	Address Input Current, Input Voltage Low			3	−0.002		−10	−30		−10	−30		V_{EN} = 2.4 V	All V_A = 0
18						1	−0.002		−10	−30		−10	−30		V_{EN} = 0	
19	DYNAMIC	$t_{transition}$	Switching Time of Multiplexer		D	1	0.6		1					μs	See Figure 1	
20		t_{open}	Break-Before-Make Interval		D		0.2								See Figure 3	
21		$t_{on(EN)}$	Enable Turn-ON Time		D	1	1.0		1.5						See Figure 2	
22		$t_{off(EN)}$	Enable Turn-OFF Time		D	1	0.4		1							
23		OIRR	OFF Isolation (Note 3)		D		68							dB	V_{EN} = 0, R_L = 1K Ω, C_L = 15 pF, V_S = 7 VRMS, f = 500 KHz	
24		$C_{S(off)}$	Source OFF Capacitance		S	16	6							pF	V_S = 0	V_{EN} = 0, f = 140 KHz
25		$C_{D(off)}$	Drain OFF Capacitance	DG506A	D	1	45								V_D = 0	
26				DG507A		2	23									
27	SUP	I+	Positive Supply Current		V+		1.3		2.4			2.4		mA	V_{EN} = 0 V or 5 V	All V_A = 0
28		I−	Negative Supply Current		V−		−0.7		−1.5			−1.5				

DG506A ICMH-A
DG507A ICMH-B

NOTES:

1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. OFF position = 20 log $\frac{V_D}{V_S}$, V_S = input to "OFF" switch, V_D = output due to V_S.
4. Functional operation is possible for supply voltages less than 15 V, but the input logic threshold will shift.
5. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

SWITCHING TIME TEST CIRCUIT

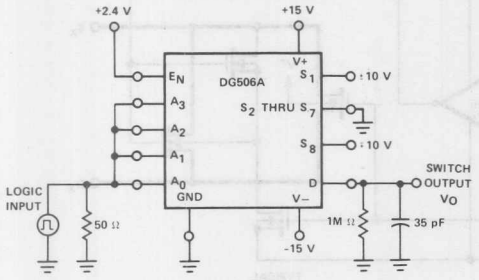


Figure 1(a)

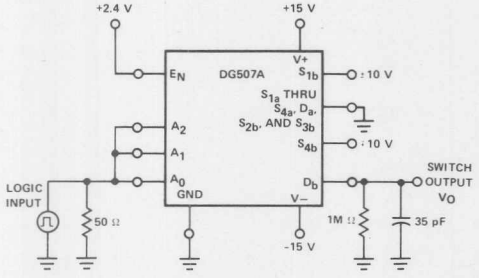
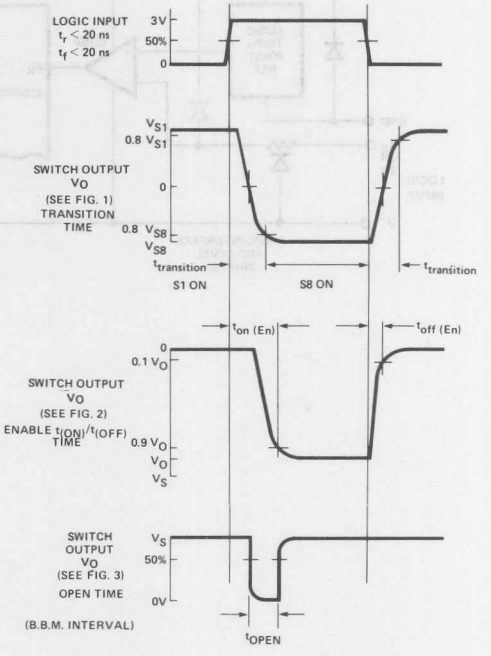


Figure 1(b)



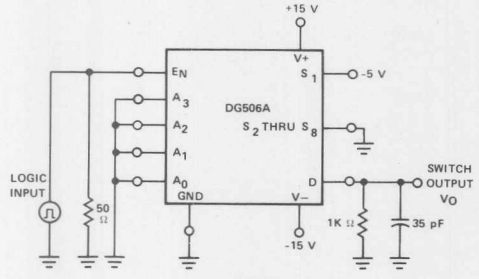


Figure 2(a)

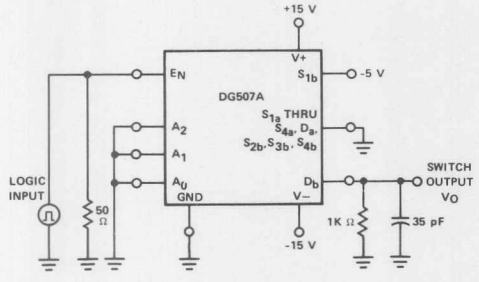


Figure 2(b)

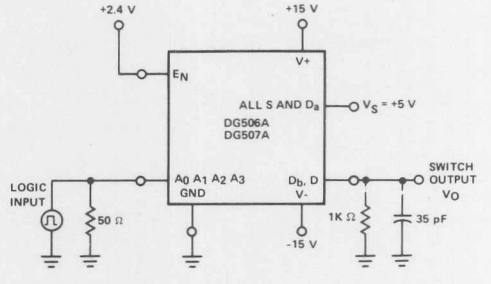
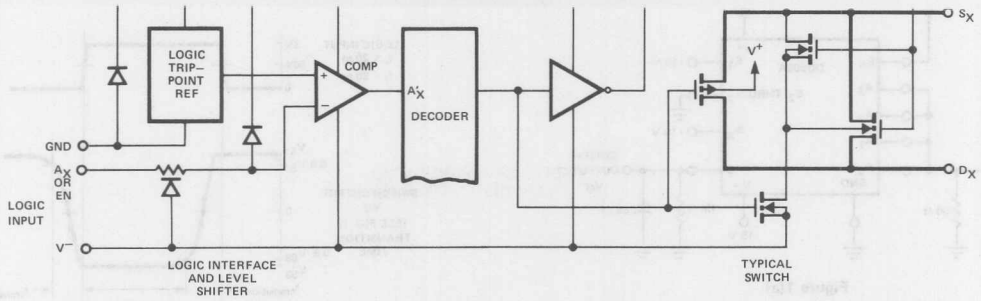


Figure 3


LOGIC TRIP–POINT REF
COMP
DECODER
GND
A_X OR EN
LOGIC INPUT
V^-
V^+
S_X
D_X
LOGIC INTERFACE AND LEVEL SHIFTER
TYPICAL SWITCH

8-Channel / 4-Channel Differential CMOS Analog Multiplexer *designed for...*

- **Data Acquisition Systems**
- **Multiplexing Reference Signals**
- **Communication Systems**

Siliconix

BENEFITS

- **Easily Interfaced**
 - TTL, DTL and CMOS Direct Control Over Military Temperature Range
- **Low Stand-By Power**
 - 36 mW Typical Stand-By Power
- **Reduces System Cross-Talk**
 - Break-Before-Make Switching Action
- **Reduces External Component Requirements**
 - ±15 V Analog Signal Range with ±15 V Supplies
- **Environmentally Rugged**
 - Latch-proof CMOS

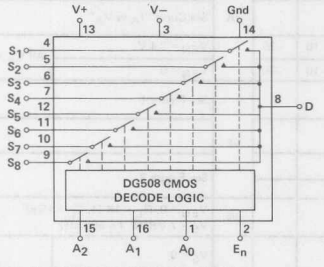
DESCRIPTION

The DG508 is a single-pole 8-position (plus OFF) electronic switch array [DG509 double-pole, 4-position (plus OFF)], which employs 8 pairs of complementary MOS (CMOS) field-effect transistors designed to function as analog switches. In the ON condition each switch will conduct current in either direction, and in the OFF position each switch will block voltages up to 30 V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 3-bit binary word input plus an Enable-Inhibit input. The truth table below shows the binary word required to select any one of the 8 switch positions, provided a positive logic "1" is present at the Enable Input. With logic "0" at the Enable input all switches will be OFF. The logic decoder and the Enable inputs will recognize as logic "0" any voltage between 0 and 0.8 V, and any voltage between 2.4 and 15 V as logic "1" inputs. The inputs can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Delays are designed into logic decode and driver circuits to insure that switch action is break-before-make. For new designs, use DG508A and DG509A.

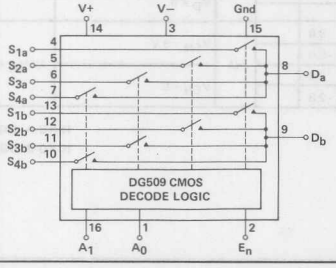
DECODE TRUTH TABLE

	A_2	A_1	A_0	En	ON SWITCH	DG509
DG508	X	X	X	0	NONE	
	0	0	0	1	1	
	0	0	1	1	2	
	0	1	0	1	3	
	0	1	1	1	4	
	1	0	0	1	5	Logic "1" = $V_{AH} \geq 2.4$ V
	1	0	1	1	6	
	1	1	0	1	7	Logic "0" = $V_{AL} \leq 0.8$ V
	1	1	1	1	8	

FUNCTIONAL DIAGRAM DG508

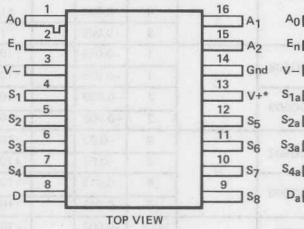


FUNCTIONAL DIAGRAM DG509



PIN CONFIGURATIONS

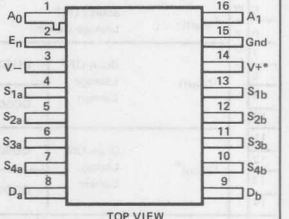
Flat Package



TOP VIEW

ORDER NUMBER:
DG508AL
SEE PACKAGE 17

Flat Package

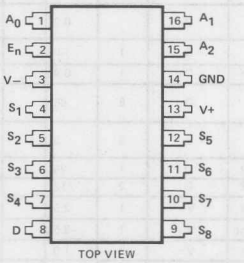


TOP VIEW

ORDER NUMBER:
DG509AL
SEE PACKAGE 17

*Common to Substrate and Base of Package

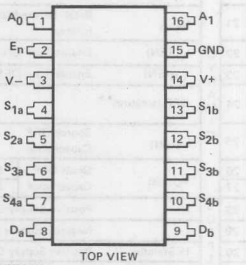
Dual-In-Line Package



TOP VIEW

ORDER NUMBERS:
DG508AP OR DG508BP
SEE PACKAGE 12
DG508CJ
SEE PACKAGE 8

Dual-In-Line Package



TOP VIEW

V+ COMMON TO SUBSTRATE

ORDER NUMBERS:
DG509AP OR DG509BP
SEE PACKAGE 12
DG509CJ
SEE PACKAGE 8

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground −0.3 V, V+
V_S or V_D to V+ 0, −32 V
V_S or V_D to V− 0, 32 V
V+ to Ground 16 V
V− to Ground −16 V
Current (Any Terminal, Except S or D) . . . 30 mA
Continuous Current, S or D 20 mA
Peak Current, S or D
(Pulsed at 1 msec, 10% Duty Cycle Max) . . 40 mA
Operating Temperature (A Suffix) −55 to 125°C
(B Suffix) −20 to 85°C
(C Suffix) 0 to 70°C

Storage Temperature (A & B Suffix) . . −65 to 150°C
(C Suffix) −65 to 125°C
Power Dissipation (Package)*
16 Pin DIP** 900 mW
16 Pin Plastic DIP*** 470 mW
Flat Package**** 750 mW

*All leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C
***Derate 6.3 mW/°C above 25°C
****Derate 10 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MEASURED TERMINAL	NO. TESTS PER TEMP.	TYP† 25°C	MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIXES −20°C 0°C	B/C SUFFIXES 25°C	B/C SUFFIXES 85°C 70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = 15 V, Ground = 0	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability			±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2		$r_{DS(on)}$	Drain-Source ON Resistance	S to D	8	270	400	400	500	450	450	550	Ω	V_D = 10 V, I_S = −200 μA	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V
3					8	230	400	400	500	450	450	500		V_D = −10 V, I_S = −200 μA	
4		$\Delta r_{DS(on)}$	Greatest Change in Drain Source ON Resistance Between Channels	S to D	8	6							%	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}\ MAX - r_{DS(on)}\ MIN}{r_{DS(on)}\ AVE}\right)$ −10 V ≤ V_S ≤ 10 V	
5	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	S	8	−0.005		±1	±50		±5	±50	nA	V_S = 10 V, V_D = −10 V	V_{EN} = 0
6					8	−0.005		±1	±50		±5	±50		V_S = −10 V, V_D = 10 V	
7		$I_{D(off)}$	Drain OFF Leakage Current DG508	D	1	−0.015		±10	±200		±20	±200		V_D = 10 V, V_S = −10 V	
8					1	−0.015		±10	±200		±20	±200		V_D = −10 V, V_S = 10 V	
9			DG509		2	−0.008		±10	±100		±20	±100		V_D = 10 V, V_S = −10 V	
10					2	−0.008		±10	±100		±20	±100		V_D = −10 V, V_S = 10 V	
11		$I_{D(on)}$*	Drain ON Leakage Current DG508	D	8	−0.03		±10	±200		±20	±200		$V_{S(all)}$ = V_D = 10 V	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V
12					8	−0.03		±10	±200		±20	±200		$V_{S(all)}$ = V_D = −10 V	
13			DG509		8	−0.015		±10	±100		±20	±100		$V_{S(all)}$ = V_D = 10 V	
14					8	−0.015		±10	±100		±20	±100		$V_{S(all)}$ = V_D = −10V	
15	INPUT	I_{AH}	Address Input Current, Input Voltage High	A_0, A_1 (A_2) EN	(4) 3	−0.002		−10	−30		−10	−30	μA	V_A = 2.4 V	
16					(4) 3	0.006		10	30		10	30		V_A = 15 V	
17		$I_{A(peak)}$	Peak Address Input Current		(4) 3	−75								See Curve "I_A vs V_A"	
18		I_{AL}	Address Input Current Input Voltage Low	A_0, A_1 (A_2)	(3) 2	−0.002		−10	−30		−10	−30		V_{EN} = 2.4 V	All V_A = 0
19				EN	1	−0.002		−10	−30		−10	−30		V_{EN} = 0	
20	DYNAMIC	$t_{transition}$	Switching Time of Multiplexer	D		0.6		1					μs	See Figure 1	
21		t_{open}	Break-Before-Make Interval	D		0.2									
22		t_{on}(EN)	Enable Turn-ON Time	D	1	1.0		1.5						See Figure 2	
23		t_{off}(EN)	Enable Turn-OFF Time	D	1	0.4		1							
24		OFF Isolation**		D	8	68							dB	V_{EN} = 0, R_L = 1K Ω, C_L = 15 pF V_S = 7 VRMS, f = 500 kHz	
25		$C_{S(off)}$	Source OFF Capacitance	S	8	5							pF	V_S = 0	V_{EN} = 0, f = 140 kHz
26		$C_{D(off)}$	Drain OFF Capacitance DG508	D	1	25								V_D = 0	
27			DG509	D	2	12									
28	SUPPLY	I+	Positive Supply Current	V+	1	3.5		8.0			8.0		mA	V_{EN} = 5 V	All V_A = 0
29		I−	Negative Supply Current	V−	1	−3.5		−8.0			−8.0				
30		I+ Standby	Positive Supply Current	V+	1	1.0		2.4			2.8			V_{EN} = 0	
31		I− Standby	Negative Supply Current	V−	1	−1.0		−2.4			−2.8				

ICXG-A DG508
ICXG-B DG509

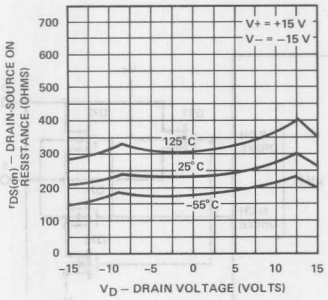
† Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

*$I_{D(on)}$ is leakage from driver into "ON" switch.

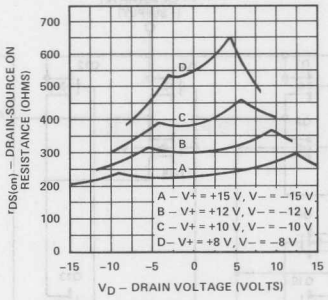
**OFF isolation $\triangleq 20 \log \frac{|V_D|}{|V_S|}$, V_S = input to "OFF" switch, V_D = output due to V_S.

TYPICAL CHARACTERISTICS

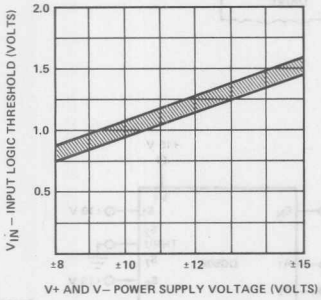
$r_{DS(on)}$ vs V_D and Temperature



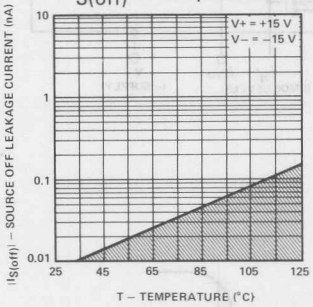
$r_{DS(on)}$ vs V_D and Power Supply Voltage



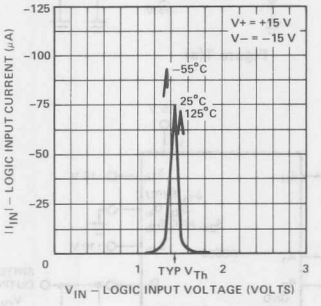
Logic Threshold vs Power Supply Voltage



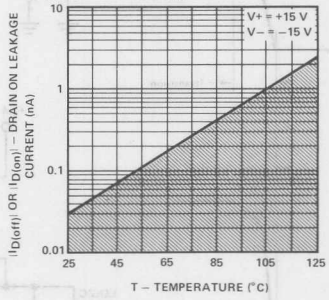
$I_{S(off)}$ vs Temperature*



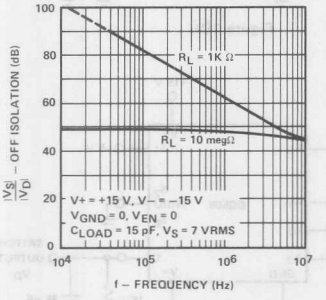
I_A vs V_A (Terminals A_0, A_1, A_2, EN)



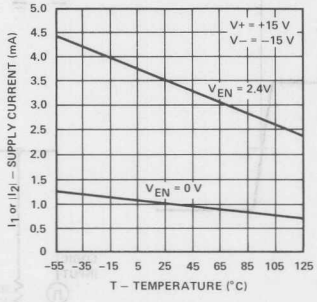
$I_{D(off)}$ and $I_{D(on)}$ vs Temperature*



OFF Isolation vs Frequency

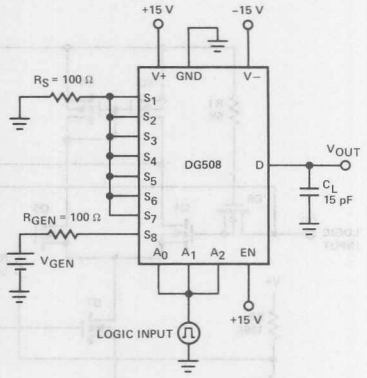


Power Supply Current vs Temperature

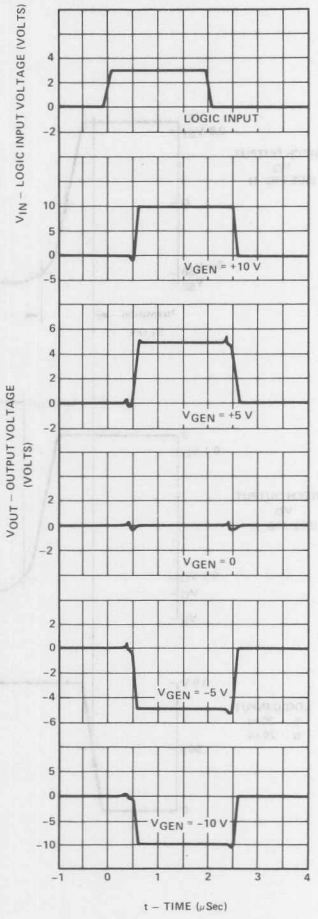


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

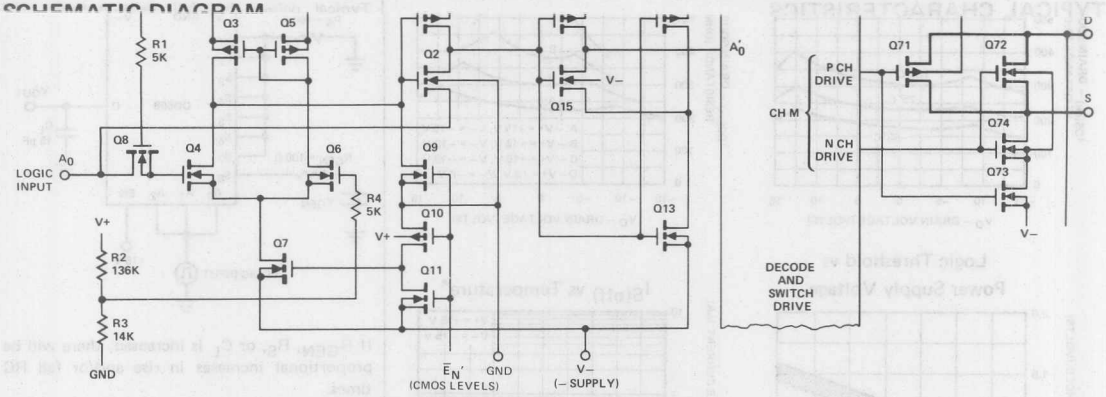
Typical delay, rise, fall, settling times, and switching transients in this circuit (similar circuit for DG509).



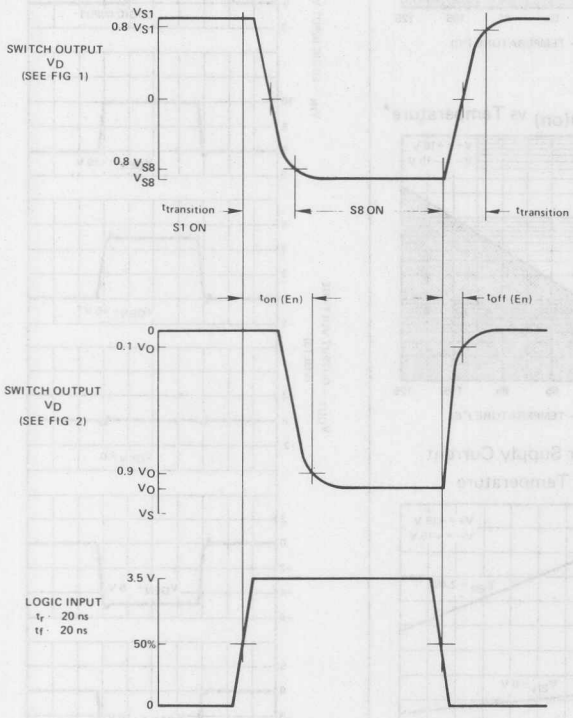
If R_{GEN}, R_S, or C_L is increased, there will be proportional increases in rise and/or fall RC times.



SCHEMATIC DIAGRAM



SWITCHING TIME TEST CIRCUIT



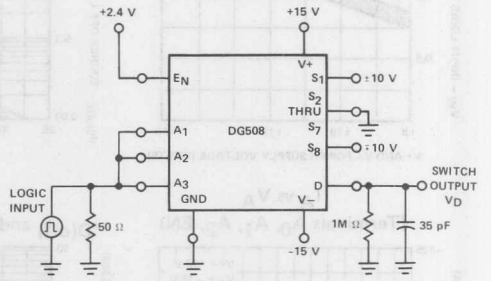


Figure 1(a)

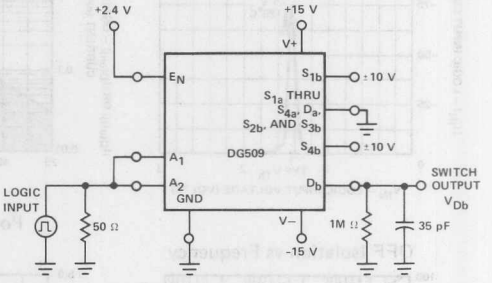


Figure 1(b)

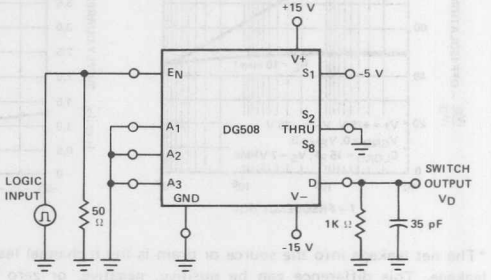


Figure 2

APPLICATIONS

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
+15**	−15	2.4/0.8	−15 to +15
+12	−12	2.4/0.8	−12 to +12
+10	−10	2.4/0.6	−10 to +10
+8***	−8	2.4/0.4	−8 to +8

Application Hints*

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics chart based on V+ = +15 V, V− = −15 V.

***Operation below ±8 V is not recommended due to the shift in $V_{INL(MAX)}$.

Logic Inputs

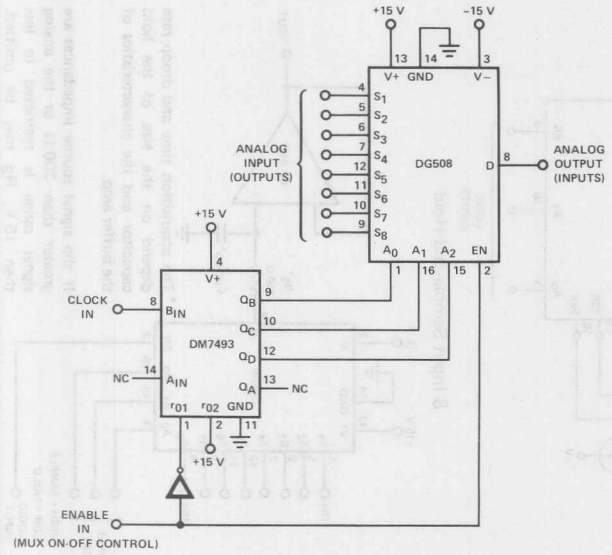
Logic input circuitry protects the input MOS gate from static transients. A series MOS device shuts off when V_{IN} exceeds the positive power supply. Negative transients are clamped to ground by a diode clamp.

The input voltage characteristics have a current spike occurring at the transition voltage when the logic goes from V_{INH} to V_{INL}. If a series resistor is used for additional static protection, it should be limited to less than 9.1K Ω to insure switching with worst case current spikes.

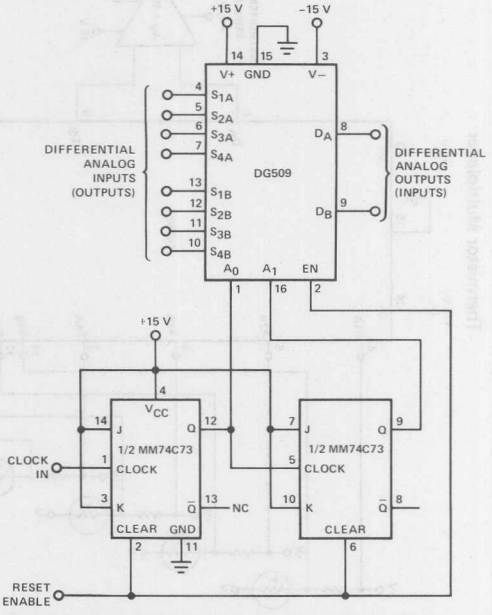
Truth Table

	ENABLE	MUX SEQUENCE RATE	MUX INPUTS A_0	A_1	A_2	DG508 SWITCH PAIR STATES (– DENOTES OFF) S1	S2	S3	S4	S5	S6	S7	S8
DG509	0	0	X	X	X	–	–	–	–	–	–	–	–
	1	0	0	0	0	ON	–	–	–	–	–	–	–
	1	1 pulse	1	0	0	–	ON	–	–	–	–	–	–
	1	2 pulses	0	1	0	–	–	ON	–	–	–	–	–
	1	3 pulses	1	1	0	–	–	–	ON	–	–	–	–
	1	4 pulses	0	0	1	–	–	–	–	ON	–	–	–
	1	5 pulses	1	0	1	–	–	–	–	–	ON	–	–
	1	6 pulses	0	1	1	–	–	–	–	–	–	ON	–
	1	7 pulses	1	1	1	–	–	–	–	–	–	–	ON
	1	8 pulses	0	0	0	ON	–	–	–	–	–	–	–

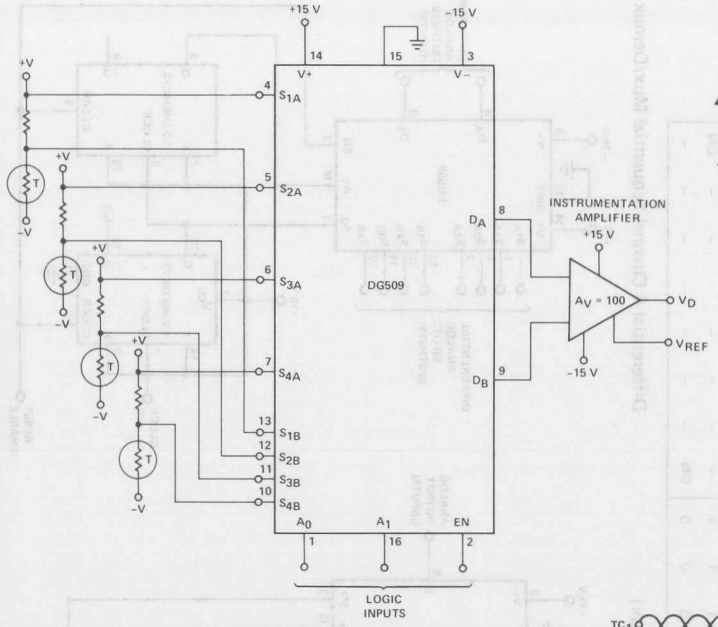
8 Channel Sequential Mux (Demux)



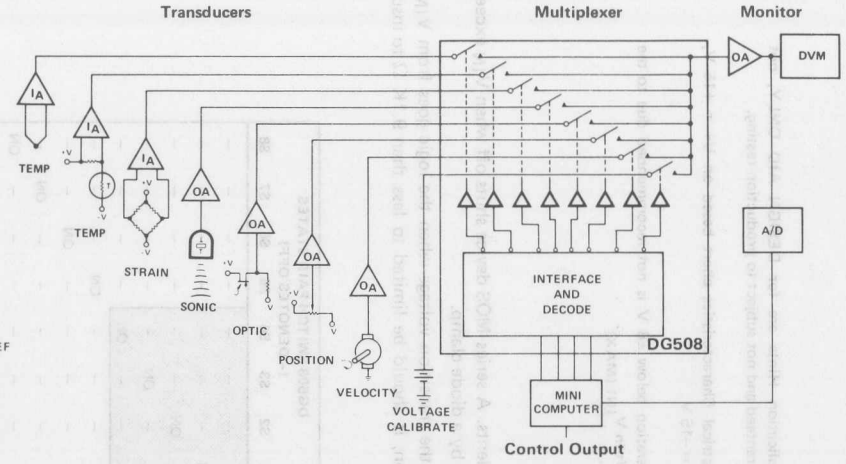
Differential 4 Channel Sequential Mux/Demux.



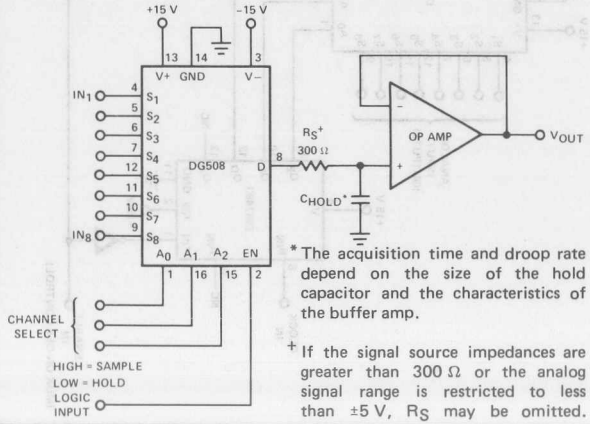
Thermistor Multiplexer



Industrial Control Multiplexing



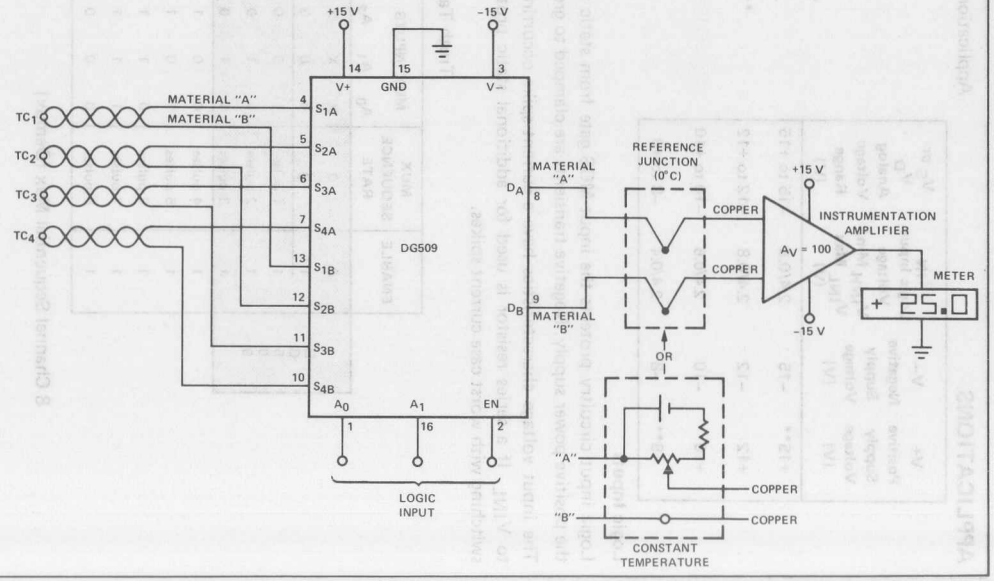
8 Input Sample-and-Hold



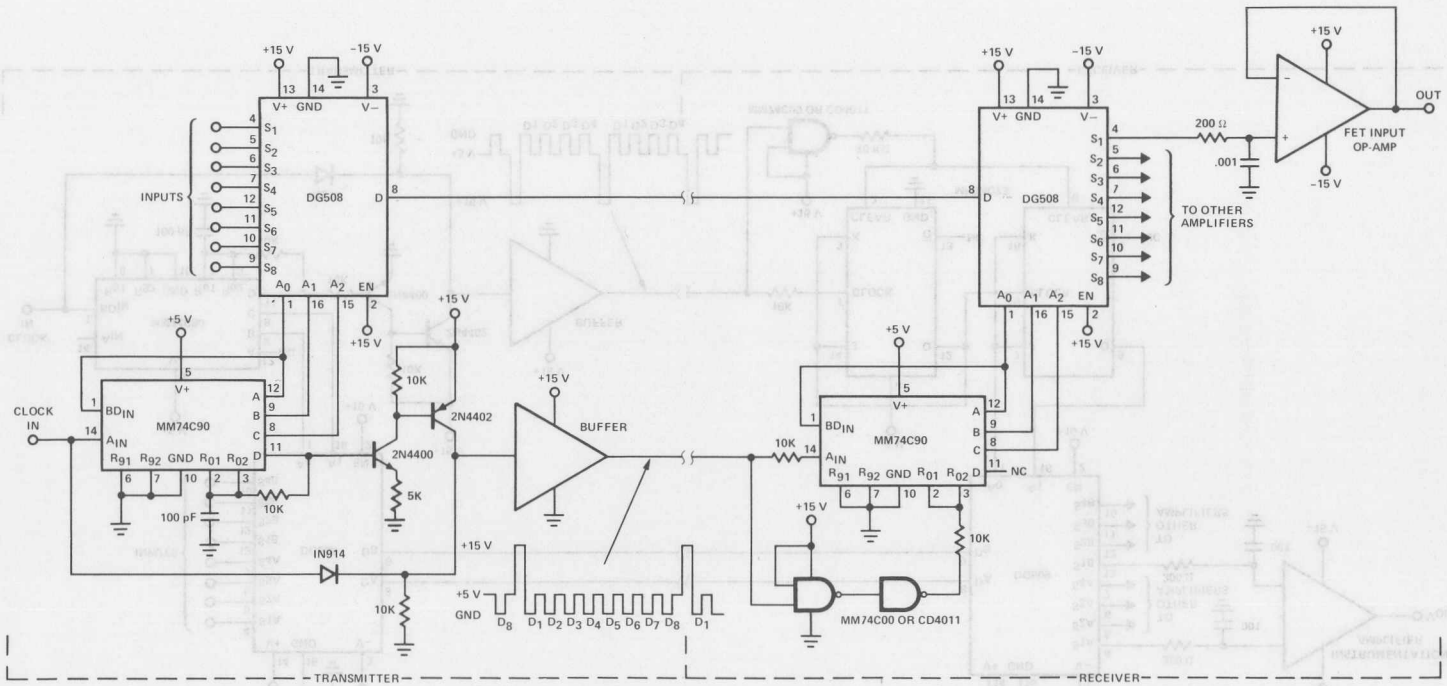
* The acquisition time and droop rate depend on the size of the hold capacitor and the characteristics of the buffer amp.

\+ If the signal source impedances are greater than 300 Ω or the analog signal range is restricted to less than ±5 V, R_S may be omitted.

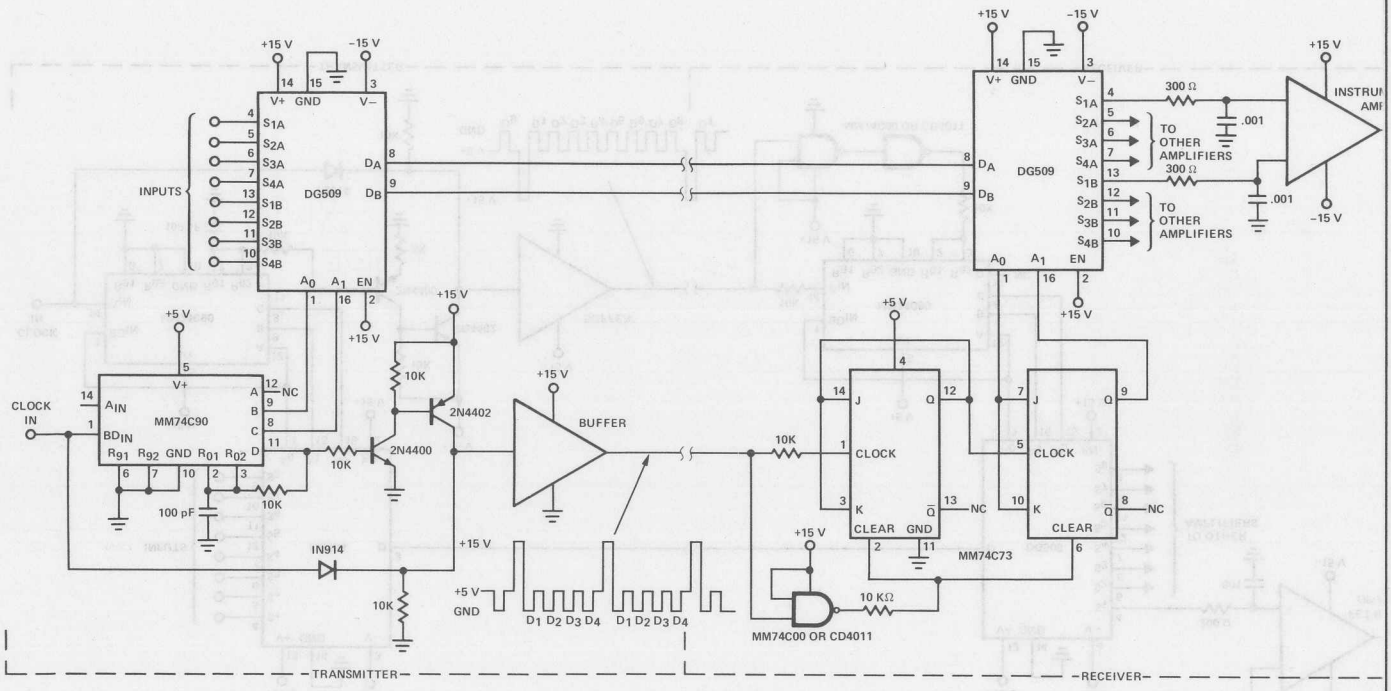
DG509 Thermocouple Multiplexer



An 8 Channel Mux/Demux System



Differential Mux/Demux System



Analog Multiplexer

designed for...

- **Data Acquisition Systems**
- **Multiplexing Reference Signals**
- **Communication Systems**

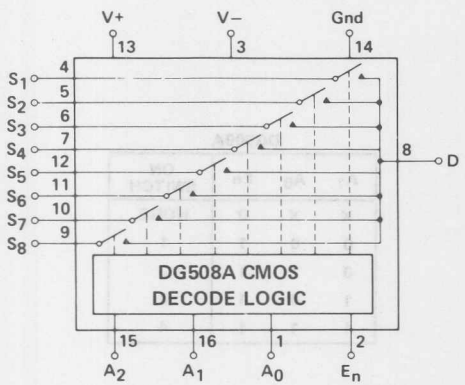
- TTL, DTL and CMOS Direct Control Over Military Temperature Range
- **Low Power**
 - 30 mW Typical Quiescent Power
- **Reduces System Cross-Talk**
 - Break-Before-Make Switching Action
- **Environmentally Rugged**
 - Latchproof PLUS-40 CMOS
 - 44V Power Supply Maximum Rating
 - Static Protection Circuitry on all Inputs

DESCRIPTION

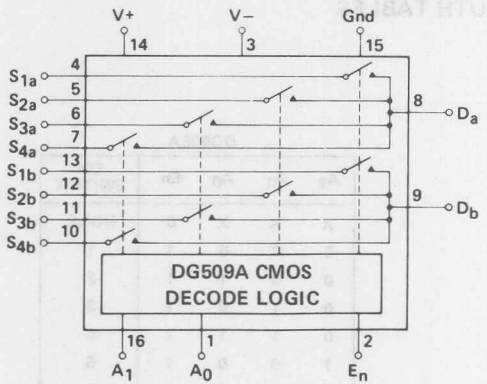
The DG508A a single ended 8 channel analog multiplexer connects 1 of 8 inputs to a common output decoded from 3 binary inputs (A_0, A_1, A_2).

The DG509A a differential input 4 channel analog multiplexer connects 1 of 4 differential inputs to a common differential output decoded from 2 binary inputs (A_0, A_1). In the ON state each switch conducts current in either direction, and in the OFF state blocks voltage up to the power supply rails, generally 30 volts peak-to-peak. Bidirectional current switching also insures equal operation as a demultiplexer. An enable (E_n) input provides a package select function. All control inputs address (A_x) and enable (E_n) are TTL or CMOS compatible over the full operating temperature range of the product. The multiplexers operate in a Break-Before-Make (BBM) switch action between any two decoded switch selections protecting against momentary shorting of the input transducers. Additionally BBM action occurs between package selection. See the DG528 and DG529 for the same function plus latches on the A_2, A_1, A_0, E_n inputs.

FUNCTIONAL DIAGRAMS



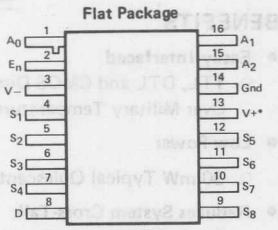
DG508A
8 Channel Single Ended Multiplexer



DG509A
Differential 4 Channel Multiplexer

PIN CONFIGURATIONS

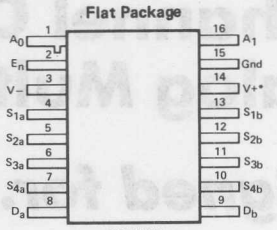
Flat Package



TOP VIEW

ORDER NUMBER:
DG508AAL
SEE PACKAGE 17

Flat Package

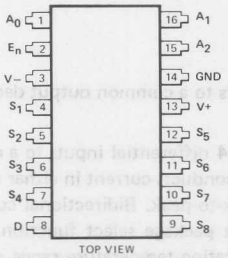


TOP VIEW

ORDER NUMBER:
DG509AAL
SEE PACKAGE 17

***Common to Substrate and Base of Package**

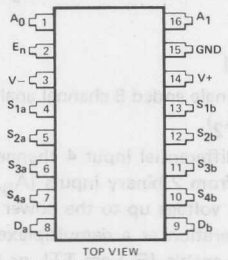
Dual-In-Line Package



TOP VIEW
V+ COMMON TO SUBSTRATE

ORDER NUMBERS:
DG508AAK, DG508ABK or DG508ACK
SEE PACKAGE 10
DG508ACJ
SEE PACKAGE 8

Dual-In-Line Package



TOP VIEW
V+ COMMON TO SUBSTRATE

ORDER NUMBERS:
DG509AAK, DG509ABK or DG509ACK
SEE PACKAGE 10
DG509ACJ
SEE PACKAGE 8

TRUTH TABLES

DG508A

A_2	A_1	A_0	En	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG509A

A_1	A_0	En	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{AL} \leq 0.8V$, Logic "1" = $V_{AH} \geq 2.4V$

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–

V+ 44 V
GND 25 V
Digital inputs[4], V_S, V_D –2 V to (V^+ +2 V) or 20 mA, whichever occurs first.

Current (Any Terminal, Except S or D) . . . 30 mA
Continuous Current, S or D 20 mA
Peak Current, S or D
(Pulsed at 1 msec, 10% Duty Cycle Max) . . 40 mA
Operating Temperature (A Suffix) –55 to 125°C
(B Suffix) –20 to 85°C
(C Suffix) 0 to 70°C

Storage Temperature (A & B Suffix) . . –65 to 150°C
(C Suffix) –65 to 125°C
Power Dissipation (Package)*
16 Pin DIP** 900 mW
16 Pin Plastic DIP*** 470 mW
Flat Package**** 750 mW

*All leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C
***Derate 6.3 mW/°C above 25°C
****Derate 10 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MEASURED TERMINAL	NO. TESTS PER TEMP.	TYP[1] 25°C	MAX LIMITS A SUFFIX –55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIXES –20/0°C	B/C SUFFIXES 25°C	B/C SUFFIXES 85/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V– = 15 V, Ground = 0	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability			±15		±15	±15		±15	±15	V		
2		$r_{DS(on)}$	Drain-Source ON-Resistance	S to D	8	270	400	400	500	450	450	550	Ω	V_D = 10 V, I_S = –200 μA	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V
3					8	230	400	400	500	450	450	500		V_D = –10 V, I_S = –200 μA	
4		$\Delta r_{DS(on)}$	Greatest Change in Drain Source ON Resistance Between Channels	S to D	8	6							%	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)\ MAX} - r_{DS(on)\ MIN}}{r_{DS(on)\ AVE}}\right)$ –10 V ≤ V_S ≤ 10 V	
5	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	S	8	0.002		±1	±50		±5	±50	nA	V_S = 10 V, V_D = –10 V	V_{EN} = 0
6					8	–0.005		±1	±50		±5	±50		V_S = –10 V, V_D = 10 V	
7		$I_{D(off)}$	Drain OFF Leakage Current DG508A	D	1	0.010		±10	±200		±20	±200		V_D = 10 V, V_S = –10 V	
8					1	–0.015		±10	±200		±20	±200		V_D = –10V, V_S = 10 V	
9			DG509A		2	0.005		±10	±100		±20	±100		V_D = 10 V, V_S = –10 V	
10					2	–0.008		±10	±100		±20	±100		V_D = –10 V, V_S = 10 V	
11		$I_{D(on)}$[2]	Drain ON Leakage Current DG508A	D	8	0.015		±10	±200		±20	±200		$V_{S(all)}$ = V_D = 10 V	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V
12					8	–0.030		±10	±200		±20	±200		$V_{S(all)}$ = V_D = –10 V	
13			DG509A		8	0.007		±10	±100		±20	±100		$V_{S(all)}$ = V_D = 10 V	
14					8	–0.015		±10	±100		±20	±100		$V_{S(all)}$ = V_D = –10 V	
15	INPUT	I_{AH}	Address Input Current, Input Voltage High	A_0, A_1, (A_2), EN	(4) 3	–0.002		±10	–30		–10	–30	μA	V_A = 2.4 V	
16					(4) 3	0.006		10	30		10	30		V_A = 15 V	
17		I_{AL}	Address Input Current Input Voltage Low		(3) 2	–0.002		–10	–30		–10	–30		V_{EN} = 2.4 V	All V_A = 0
18					1	–0.002		–10	–30		–10	–30		V_{EN} = 0	
19	DYNAMIC	$t_{transition}$	Switching Time of Multiplexer	D	1	0.6		1					μs	See Figure 1	
20		t_{open}	Break-Before-Make Interval	D		0.2								See Figure 3	
21		$t_{on(EN)}$	Enable Turn-ON Time	D	1	1.0		1.5						See Figure 2	
22		$t_{off(EN)}$	Enable Turn-OFF Time	D	1	0.4		1							
23		OIRR	OFF Isolation (Note 3)	D	8	68							dB	V_{EN} = 0, R_L = 1K Ω, C_L = 15 pF V_S = 7 VRMS, f = 500 kHz	
24		$C_{S(off)}$	Source OFF Capacitance	S	8	5							pF	V_S = 0	V_{EN} = 0, f = 140 kHz
25		$C_{D(off)}$	Drain OFF Capacitance DG508A	D	1	25								V_D = 0	
26			DG509A	D	2	12									
27	SUPPLY	I+	Positive Supply Current	V+	1	1.3		2.4			2.4		mA	V_{EN} = 2.4 V	All V_A = 0, or 2.4 V
28		I–	Negative Supply Current	V–	1	–0.7		–1.5			–1.5				
29		I+ Standby	Positive Supply Current	V+	1	1.3		2.4			2.4			V_{EN} = 0 V	
30		I– Standby	Negative Supply Current	V–	1	–0.7		–1.5			–1.5				

NOTES:

1. Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. OFF isolation = 20 log $\frac{|V_S|}{|V_D|}$, V_S = input to "OFF" switch, V_D = output due to V_S.
4. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ICMG-A DG508A
ICMG-B DG509A

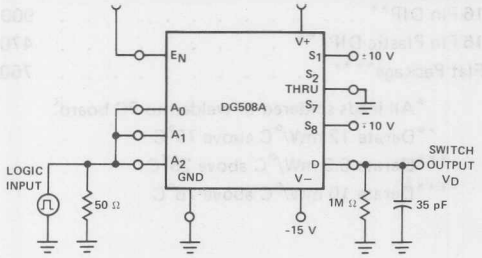
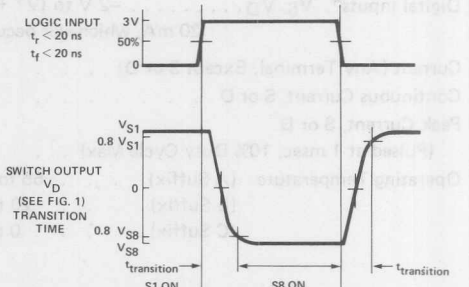


Figure 1(a)



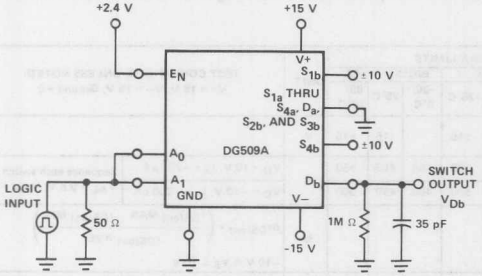
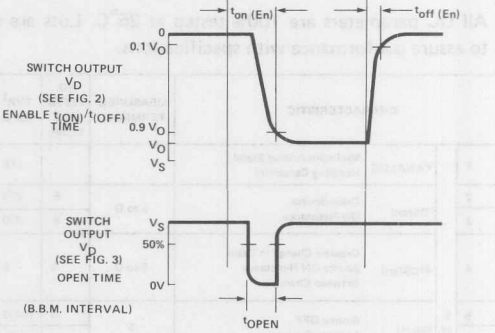


Figure 1(b)



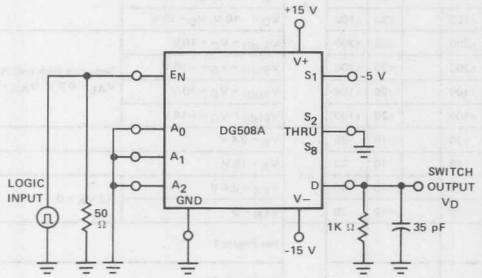


Figure 2(a)

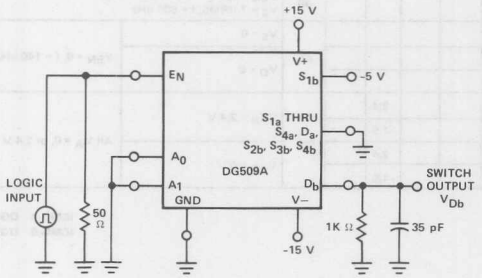


Figure 2(b)

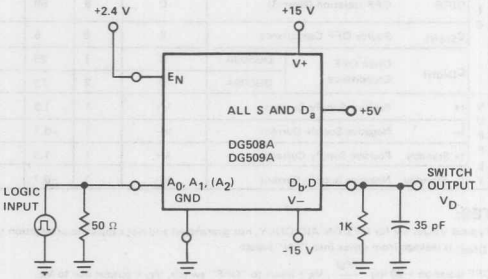


Figure 3

8-Channel and Dual 4-Channel Latchable Multiplexers

designed for . . .

- **Data Acquisition Systems**
- **Automatic Test Equipment**
- **Communication Systems**
- **Microprocessor Controlled Systems**

Siliconix

BENEFITS

- **Microprocessor Bus Compatible**
 - Accepts 300 nsec WRITE Pulse Width
 - Direct RESET
- **Environmentally Rugged**
 - 44V Power Supply Rating
 - Static Protected Logic Inputs
 - Latch-Proof
- **Easily Interfaced**
 - TTL Compatible Without Pullup Resistors $V_{INH} = 2.4V$
- **Improved System Accuracy**
 - $r_{DS(on)} < 400\Omega$
 - $V_{error} = 80\,\mu V$ Max at 125°C $= I_{D(on)} \times r_{DS(on)}$
 - $\Delta r_{DS(on)}$ Channel to Channel is Less Than 6%

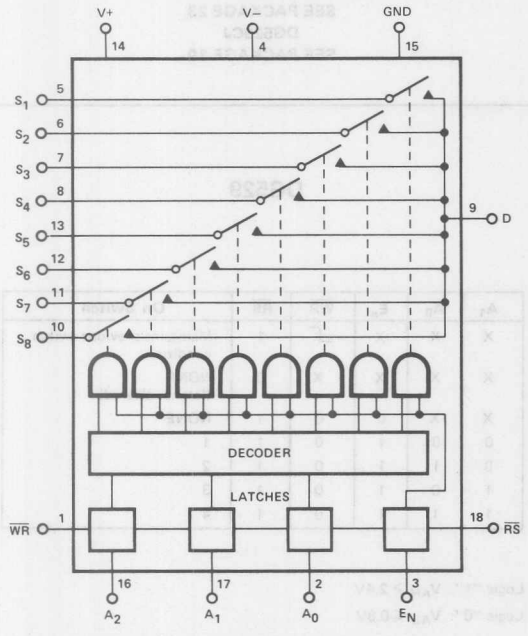
DESCRIPTION

The DG528 and DG529 designed on the Siliconix PLUS–40 CMOS Process provides solid state switch action with 400 ohms contact (ON) resistance and very high OFF resistance. True bidirectional switch action takes place over the full analog signal range of ±15 volts, with break-before-make operation to prevent momentary shorting of signal inputs. The DG528 provides 8-channel single-ended multiplexing and demultiplexing of ±15 volt analog signals. The DG529 provides 4-channel differential multiplexing and demultiplexing of ±15 volt common mode plus differential mode signals.

Four input latches on the binary coded switch-state inputs (A_0, A_1, A_2, E_n) result in microprocessor bus compatibility. Two control lines, $\overline{WR}$ and $\overline{RS}$, store or clear the the switch-state input (A_0, A_1, A_2, E_n) latches. Programming the enable input (E_n) latch with a logic zero turns all analog switches OFF. The direct chip reset $\overline{RS}$ simplifies switch turn OFF during system power up or system reset.

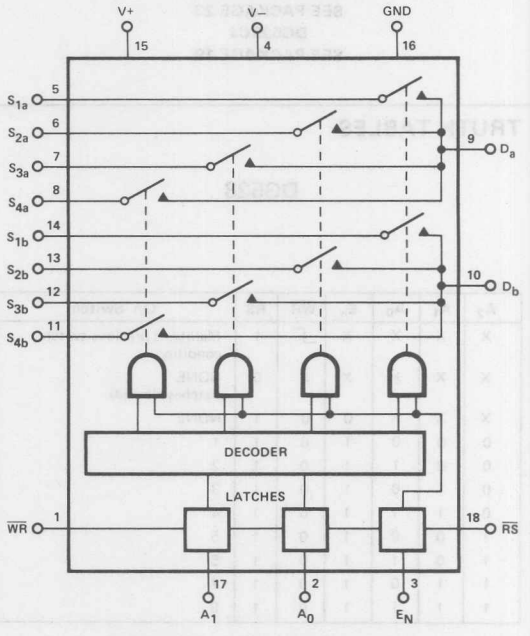
FUNCTIONAL DIAGRAMS

DG528



8 Channel Single Ended Multiplexer

DG529

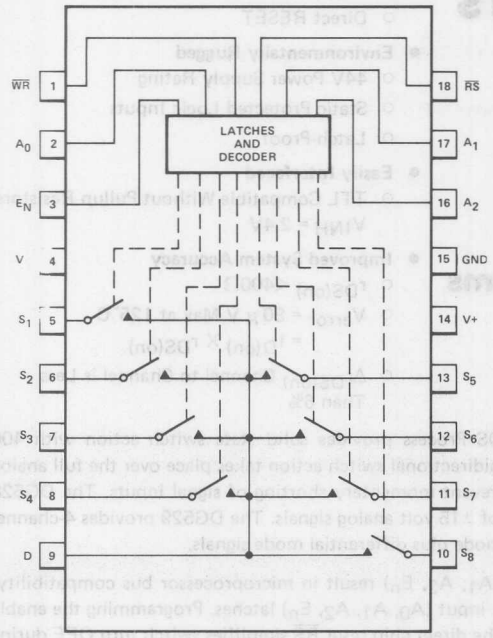


Differential 4 Channel Multiplexer

PIN CONFIGURATIONS

DG528

Dual–In–Line Package

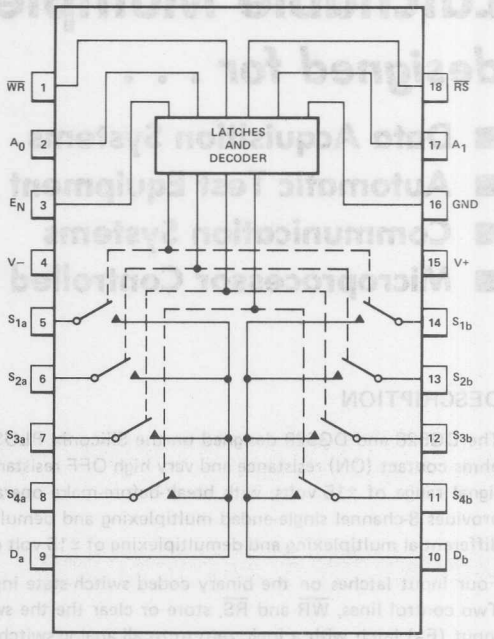


Top View

ORDER NUMBERS:
DG528AK OR DG528BK
SEE PACKAGE 23
DG528CJ
SEE PACKAGE 19

DG529

Dual–In–Line Package



Top View

ORDER NUMBERS:
DG529AK OR DG529BK
SEE PACKAGE 23
DG529CJ
SEE PACKAGE 19

TRUTH TABLES

DG528

A_2	A_1	A_0	E_n	$\overline{WR}$	$\overline{RS}$	On Switch
X	X	X	X	↓	1	Maintains previous switch condition
X	X	X	X	X	0	NONE (latches cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

DG529

A_1	A_0	E_n	$\overline{WR}$	$\overline{RS}$	On Switch
X	X	X	↓	1	Maintains previous switch condition
X	X	X	X	0	NONE (latches cleared)
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "1": $V_{AH} \geq 2.4V$
Logic "0": $V_{AL} \leq 0.8V$

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Voltages referenced to V–
V+ 44 V
GND 25 V
Digital inputs[5], V_S, V_D –2 V to (V^+ +2 V) or 20 mA, whichever occurs first.

Current (Any Terminal Except S or D) 30 mA
Continuous Current, S or D 20 mA
Peak Current, S or D
(Pulsed at 1 msec, 10% Duty Cycle Max) . 40 mA

Operating Temperature (A Suffix) –55 to 125°C
(B Suffix) –20 to 85°C
(C Suffix) 0 to 70°C
Storage Temperature (A & B Suffix) –65 to 150°C
(C Suffix) –65 to 125°C
Power Dissipation (Package)*
18 Pin DIP** 900 mW
18 Pin Plastic DIP*** 470 mW

*All leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6.3 mW/°C above 50°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample–tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		Characteristic			Measured Terminal	No. Tests Per Temp.	Typ 25°C Note 1	Max Limits A Suffix –55°C	Max Limits A Suffix 25°C	Max Limits A Suffix 125°C	Max Limits B/C Suffixes –20°C 0°C	Max Limits B/C Suffixes 25°C	Max Limits B/C Suffixes 85°C	Unit	Test Conditions, Unless Noted: V+ = 15, V– = –15, Ground = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 2.4V	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability				±15		±15	±15		±15	±15	V		
2	SWITCH	$r_{DS(on)}$	Drain–Source ON Resistance		S to D	8	270	400	400	500	450	450	550	Ω	V_D = 10V, I_S = –200 μA	Sequence each switch on V_{AL} = 0.8V, V_{AH} = 2.4V
3						8	230	400	400	500	450	450	500		V_D = –10V, I_S = –200 μA	
4		$\Delta r_{DS(on)}$	Greatest Change in Drain Source ON Resistance Between Channels		S to D	8	6							%	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}^{MAX} - r_{DS(on)}^{MIN}}{r_{DS(on)}^{AVE}}\right)$ –10V ≤ V_S ≤ 10V	
5		$I_{S(off)}$	Source OFF Leakage Current		S	8	–0.005		±1	±50		±5	±50	nA	V_S = 10V, V_D = –10V	V_{EN} = 0
6						8	–0.005		±1	±50		±5	±50		V_S = –10V, V_D = 10V	
7		$I_{D(off)}$	Drain OFF Leakage Current	DG528	D	1	–0.015		±10	±200		±20	±200		V_D = 10V, V_S = –10V	
8						1	–0.015		±10	±200		±20	±200		V_D = –10V, V_S = 10V	
9				DG529		2	–0.008		±10	±100		±20	±100		V_D = 10V, V_S = –10V	
10						2	–0.008		±10	±100		±20	±100		V_D = –10, V_S = 10V	
11		$I_{D(on)}$	Drain ON Leakage Current Note 2	DG528	D	8	–0.03		±10	±200		±20	±200		$V_{S(all)}$ = V_D = 10V	Sequence each switch on V_{AL} = 0.8V, V_{AH} = 2.4V
12						8	–0.03		±10	±200		±20	±200		$V_{S(all)}$ = V_D = –10V	
13				DG529		8	–0.015		±10	±100		±20	±100		$V_{S(all)}$ = V_D = 10V	
14						8	–0.015		±10	±100		±20	±100		$V_{S(all)}$ = V_D = –10V	
15	INPUT	I_{AH}	Logic Input Current, Input Voltage High		A_0, A_1, (A_2), E_n, $\overline{WR}$, $\overline{RS}$	5 (6)	–0.002		±10	–30		–10	–30	μA	V_A = 2.4V	
16						5 (6)	0.006		10	30		10	30		V_A = 15V	
17		I_{AL}	Logic Input Current, Input Voltage Low			5 (6)	–0.002		–10	–30		–10	–30		V_{EN} = 0	All V_A = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 0
18		$t_{transition}$	Switching Time of Multiplexer		D	1	0.6		1					μs	See Figure 3	
19		t_{open}	Break–Before–Make Interval		D		0.2								See Figure 5	
20	DYNAMIC	t_{on}(EN, $\overline{WR}$)	Enable Turn–ON Time		D	1	1.0		1						See Figures 4 and 6	
21		t_{off}(EN, $\overline{RS}$)	Enable and RS Reset Turn–OFF Time		D	1	0.4		1						See Figure 4 and 7	
22		Q	Charge Coupling		D		4.0							pC	See Figure 8	
23		OFF Isolation	Note 3		D	8	68							dB	V_{EN} = 0, R_L = 1KΩ, C_L = 15 pF V_S = 7 VRMS, f = 500 kHz	
24	SUPPLY	C_{in}	Logic Input Capacitance		A_0, A_1, (A_2) E_n, $\overline{WR}$, $\overline{RS}$		2.5							pF	f = 1 MHz	
25		$C_{S(off)}$	Source OFF Capacitance		S	8	5								V_S = 0	V_{EN} = 0, f = 140 kHz
26		$C_{D(off)}$	Drain OFF Capacitance	DG528	D	1	25								V_D = 0	
27				DG529	D	2	12									
28		I+	Positive Supply Current		V+	1			2.5			2.5		mA	V_{EN} = 0V	All V_A = 0
29		I–	Negative Supply Current		V–	1			–1.5			–1.5				

NOTES:
1. Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. OFF isolation=20 log $\frac{|V_S|}{|V_D|}$, V_S=input to "OFF" switch, V_D= output due to V_S.
4. Period of Reset ($\overline{RS}$) pulse must be at least 50 μsec during or after power ON.
5. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ICML–A DG528
ICML–B DG529

TIMING DIAGRAMS

over full temp range

30	t_{WW}	WRITE Pulse Width	$\overline{WR}$	300	ns	See Figure 1
31	t_{Dw}	A, E_n Data Valid to WRITE (Stabilization Time)	A_0, A_1, (A_2), E_n $\overline{WR}$	180		
32	t_{WD}	A, E_n Data Valid after WRITE (Hold Time)	$\overline{WR}$ A_0, A_1, (A_2), E_n	30		
33	$t_{\overline{RS}}$	RESET Pulse Width Note 4	$\overline{RS}$	500		See Figure 2 V_S = 5V

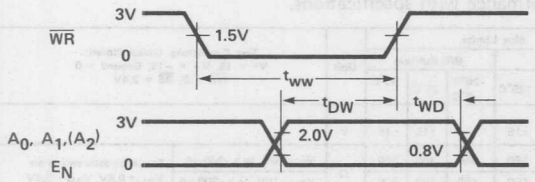


Figure 1.

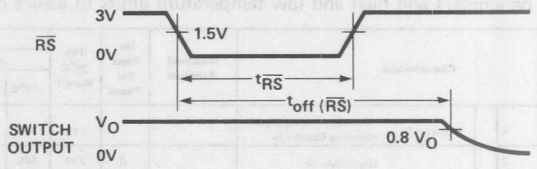
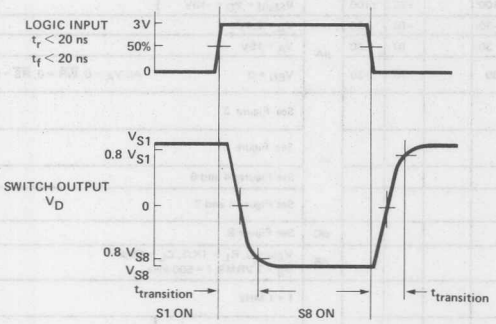
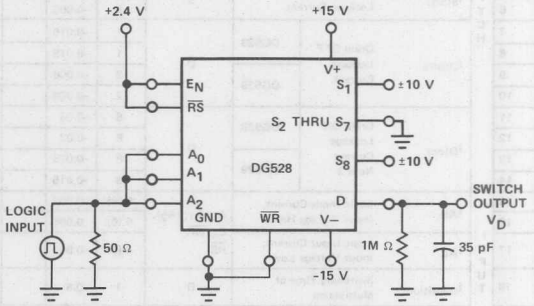


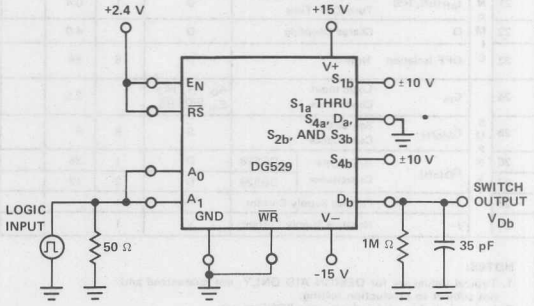
Figure 2.

SWITCHING TIME TEST CIRCUITS





(a)



(b)

Figure 3. Transition Time Test Circuit

SWITCHING TIME TEST CIRCUITS (Cont'd)

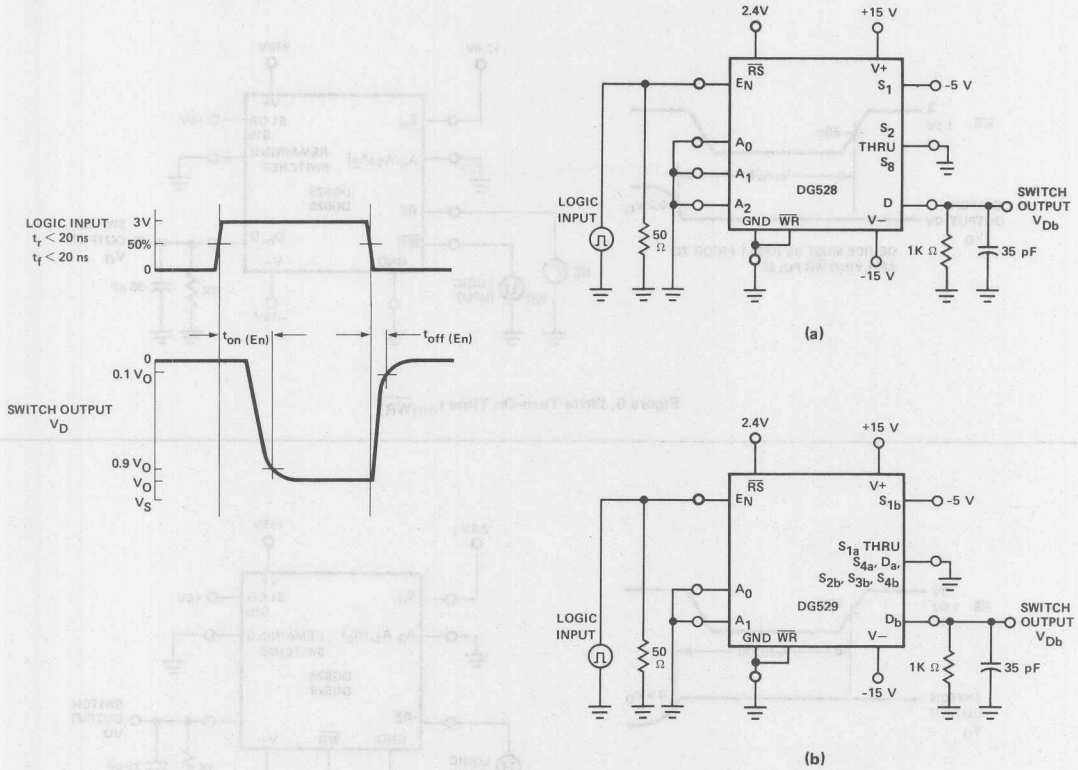


Figure 4. Enable t_{on}/t_{off} Time

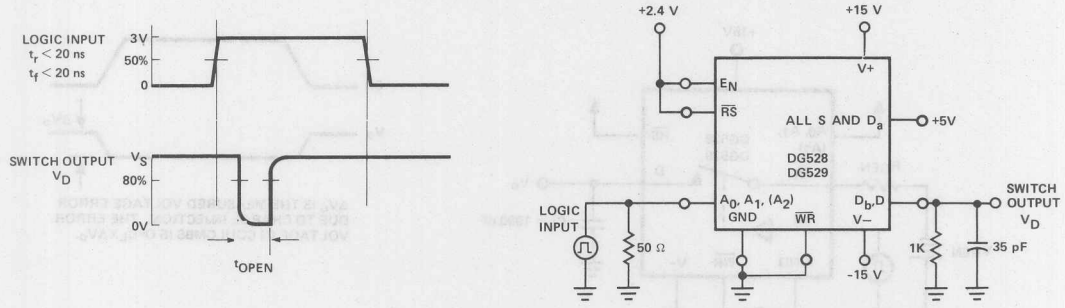


Figure 5. Open Time (B.B.M. Interval)

SWITCHING TIME TEST CIRCUITS (Cont'd)

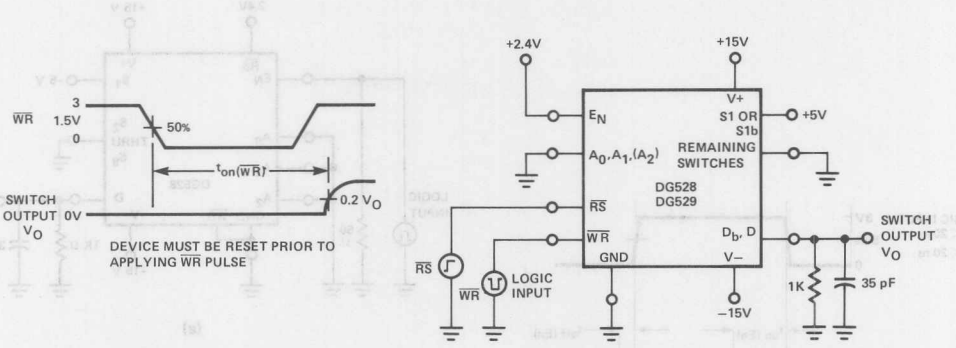


Figure 6. Write Turn-On Time $t_{on(\overline{WR})}$

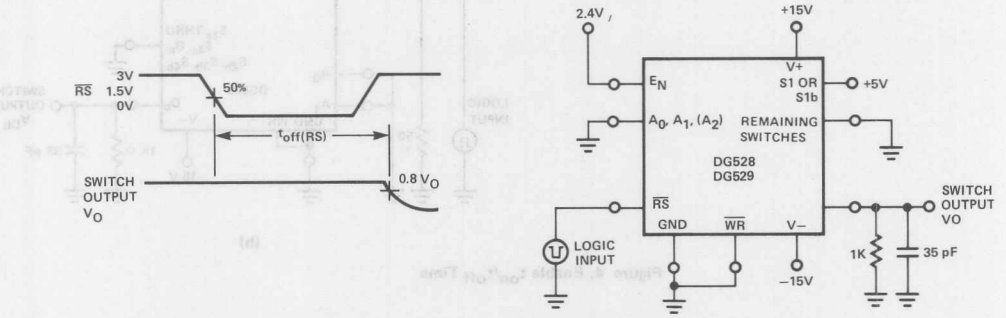


Figure 7. Reset Turn-Off Time $t_{off(\overline{RS})}$

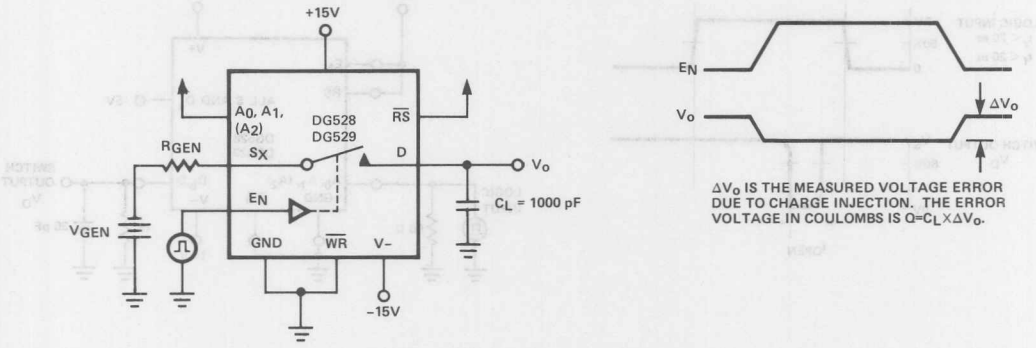


Figure 8. Charge Injection Test Circuit

DETAILED DESCRIPTION

The internal structure of the DG528 and DG529 provides a 5 volt logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel N and P channel MOSFETs (see figure 9).

Looking at figure 9, the input protection on the logic lines A_0, A_1, A_2, E_n and control lines $\overline{WR}$, $\overline{RS}$ minimize susceptibility to static encountered during handling and operational transients.

The logic interface circuit compares the TTL input signal against a TTL threshold reference voltage. The output of the comparator feeds the data input of a D-type latch. The level sensitive D latch continuously places the D_X input signal on the Q_X output when the CLK ($\overline{WR}$) input is low, resulting in transparent operation. As soon as CLK ($\overline{WR}$) returns high the latch holds the data last present on the D_X input at the Q_X output, subject to the "Minimum Input Timing Requirements" table.

Following the latches the Q_X signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting insures full ON/OFF switch operation for any analog signal present between the V+ and V- supply pins.

Power Supplies

The final data sheet will provide graphs showing the effect on power supply sensitive parameters.

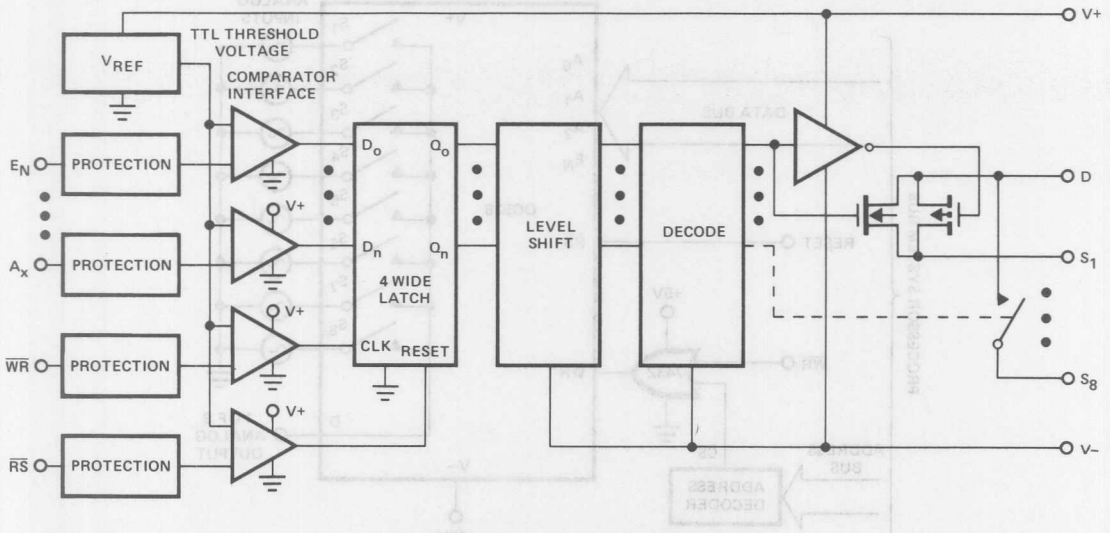


Figure 9. DG528 Simplified Internal Structure

bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers memory, that is, they can be programmed to stay in a particular switch state (e.g., switch 1 ON) until the microprocessor determines it is necessary to turn a different switch ON or turn all switches OFF.

The input latches become transparent when $\overline{WR}$ is held low; therefore, these multiplexers operate by direct command of the coded switch state on A_2, A_1, A_0. In this mode the DG528 is identical to the very popular DG508 even sharing the same pin locations. The same is true of the DG529 versus the popular DG509.

Circuit Operation: (See Figure 10)

Initially during system power-up $\overline{RS}$ would be all switches in the OFF state. As soon as the system program was ready to perform a write operation to the address assigned to the DG528, the address decoder would provide a $\overline{CS}$ active low signal which is gated with the WRITE ($\overline{WR}$) control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the $\overline{WR}$ signal returns to the high state, (positive edge) the input latches of the DG528 save the data from the DATA bus. The coded information in the A_0, A_1, A_2 and E_n latches is decoded and the appropriate switch is turned ON.

The E_n latch allows all switches to be turned OFF under program control. This becomes useful when two or more DG528s are cascaded to build 16-line and larger analog signal input multiplexers.

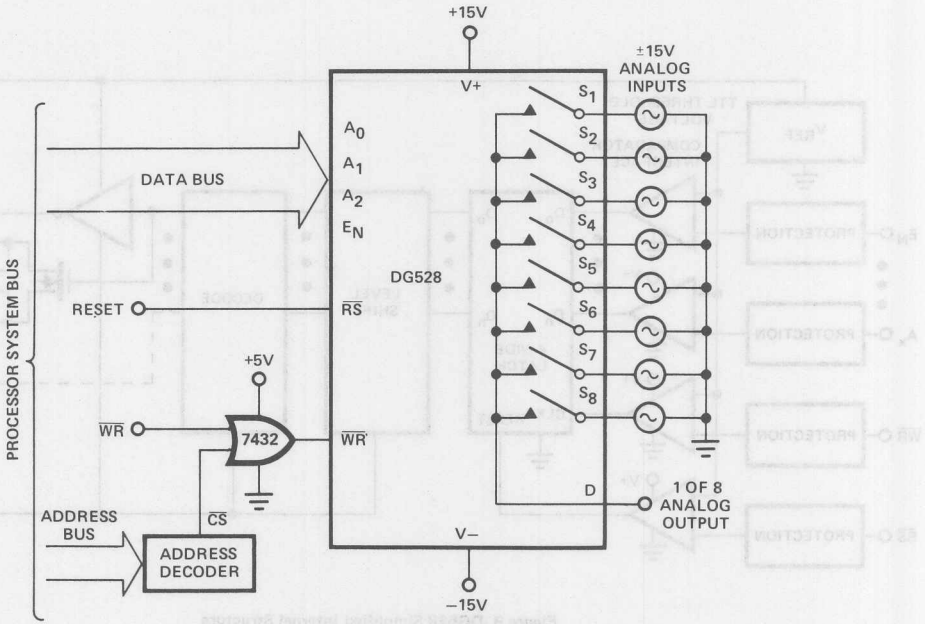


Figure 10

Monolithic 8-Channel Multiplex Switch with Decode

Siliconix

designed for . . .

■ Multiplexing Analog Signals

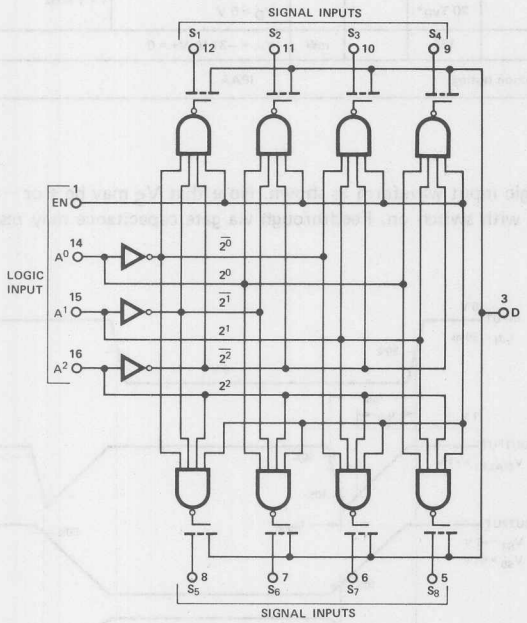
BENEFITS

- **Reduces External Component Requirements**
 - On Board Decoding
 - Internal Zener Diodes Protect MOS Gates
- **Minimizes Channel Cross-Talk Problems**
 - Break-Before-Make Switching

DESCRIPTION

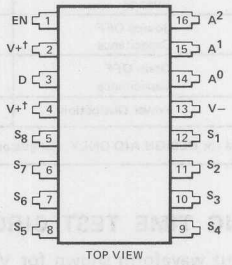
The Si3705 is designed to function as a single-pole, 8-position (plus OFF) electronic switch. The function is implemented by using eight P-channel MOS field-effect transistors as analog switches. In the ON state, each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 5 V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 3-bit binary word plus an Enable-Inhibit input. The truth table shown below indicates the binary word required to select any one of the eight switch positions. Logic input levels "L" and "H" correspond to positive logic "0" and "1". Assuming supply voltages of 5 and −20 V, logic "L" ≤ 0.6 V and logic "H" ≥ 3.5 V. The rise and fall times of the drivers are designed to provide break-before-make switch action.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

ORDER NUMBERS: Si3705142K, Si3705143K, Si3705192K OR Si3705193K
SEE PACKAGE 10

ORDER NUMBER: Si3705192P
SEE PACKAGE 12

†Both V+ lines are internally connected, either one or both may be used. V+ common to substrate.

TRUTH TABLE

LOGIC INPUTS				CHANNEL
A^0	A^1	A^2	En	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

ABSOLUTE MAXIMUM RATINGS

V+ to V−	−0.3, 35 V	Current (Any Terminal)	−20 mA
V+ to V_A, V_{En}	−0.3, 35 V	Storage Temperature	−65 to 150°C
V+ to V_D or V_S	−0.3, 35 V	Operating Temperature (A Suffix)	−55 to 125°C
V_D to V_S	±25 V	(C Suffix)	0 to 70°C
V_A, V_{En} to V−	35 V	Power Dissipation*	900 mW
V_D or V_S to V−	35 V		

*All leads soldered or welded to PC board. Derate 12 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

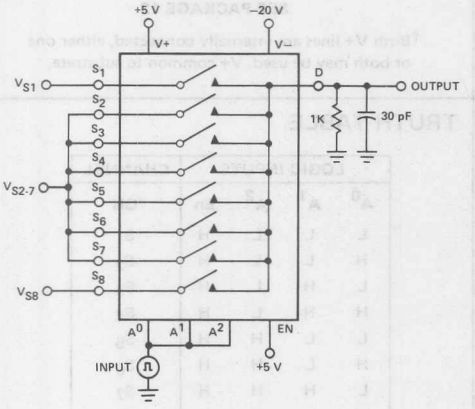
		CHARACTERISTIC		MAX LIMITS SI3705142/SI3705143 −55°C	25°C	85°C	SI3705192/SI3705193 0°C	25°C	70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V− = −20 V, V+ = 5 V, V_{En} = 3.5 V, V_{AL} = 0.6 V, V_{AH} = 3.5 V	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	150	150	225	150	150	200	Ω	V_D = 5 V	I_S = −1 mA
2				200	200	300	200	200	300		V_D = 0	
3				400	400	400	400	400	400		V_D = −5 V −142 and −192 only	
4		$I_{S(off)}$	Source OFF Leakage Current		−1	−100		−3	−150	nA	V_S = −5 V, V_D = 5 V	V_{En} = 0.6 V
5		$I_{D(off)}$	Drain OFF Leakage Current		−8	−500		−10	−500		V_D = −5 V, V_S = 5 V	
6	IN	I_{INL}	Input Current, Input Voltage Low		−1			−1		μA	V_{AL} = 0	
7		$t_{transition}$	Switching Time Of Multiplexer		2.0			2.0		μs	See Switching Time Test circuit V_{S1} = ±1 V, V_{S8} = ∓1 V, V_{S2-7} = gnd	
8		t_{on}	Turn-ON Time		1.2 Typ*			1.2 Typ*			See Switching Time Test Circuit $V_{S(all)}$ = 1 V	
9	DYNAMIC	t_{off}	Turn-OFF Time		0.8 Typ*			0.8 Typ*				
10		t_{open}	Break-Before-Make Interval		0.05 Typ*			0.05 Typ*				
11		$C_{S(off)}$	Source OFF Capacitance		10 Typ*			10 Typ*		pF	V_S = V_D = 5 V	V_{En} = 0.6 V, f = 1 MHz
12		$C_{D(off)}$	Drain OFF Capacitance		20 Typ*			20 Typ*			V_D = 5 V	
13		P_D	Power Dissipation		175			175		mW	V− = −31 V, V+ = 0	

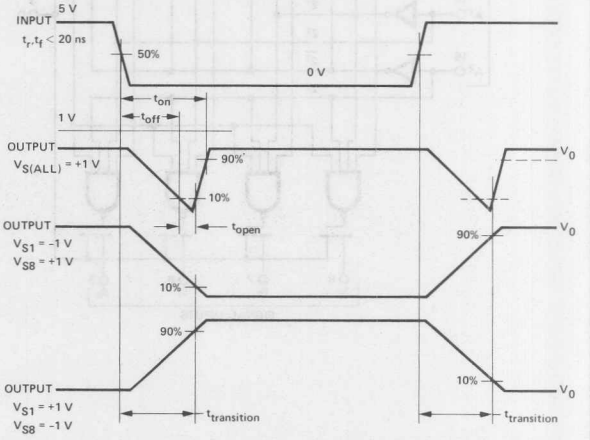
*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

IPAA

SWITCHING TIME TEST CIRCUIT

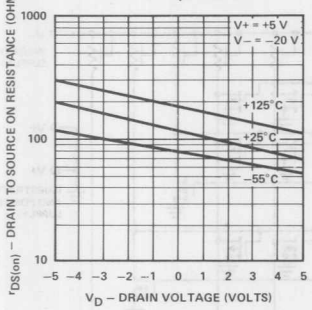
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



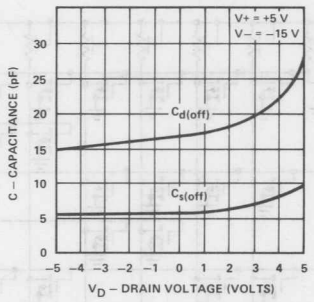


TYPICAL CHARACTERISTICS

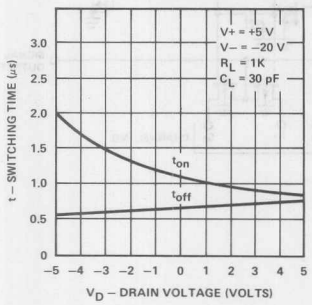
$r_{DS(on)}$ vs V_D and Temperature



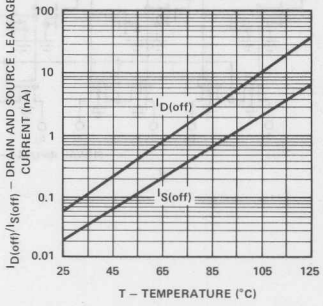
$C_{D(off)}$, $C_{S(off)}$ vs V_D



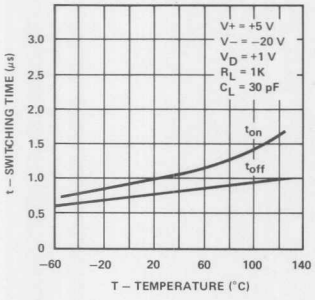
Switching Time vs V_D



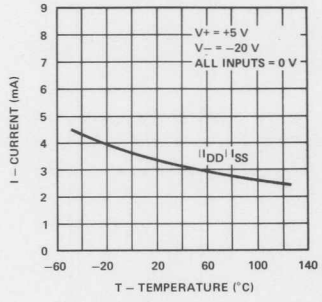
$I_{D(off)}/I_{S(off)}$ vs Temperature



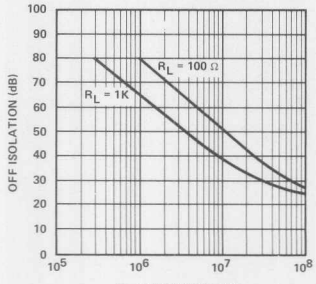
Switching Time vs Temperature

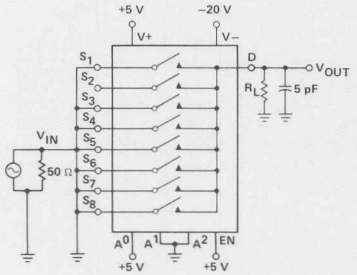


Supply Current vs Temperature

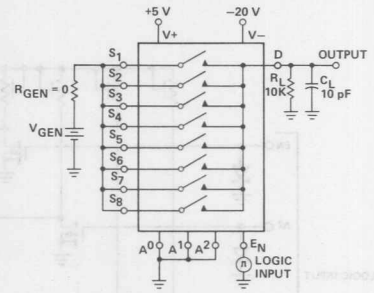


"OFF" Isolation vs R_L and Frequency

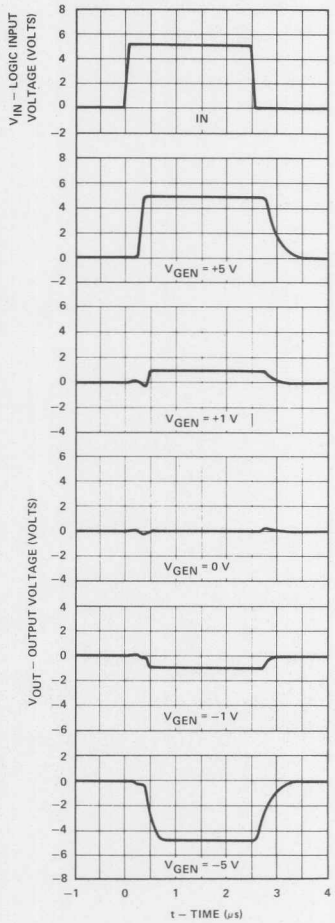


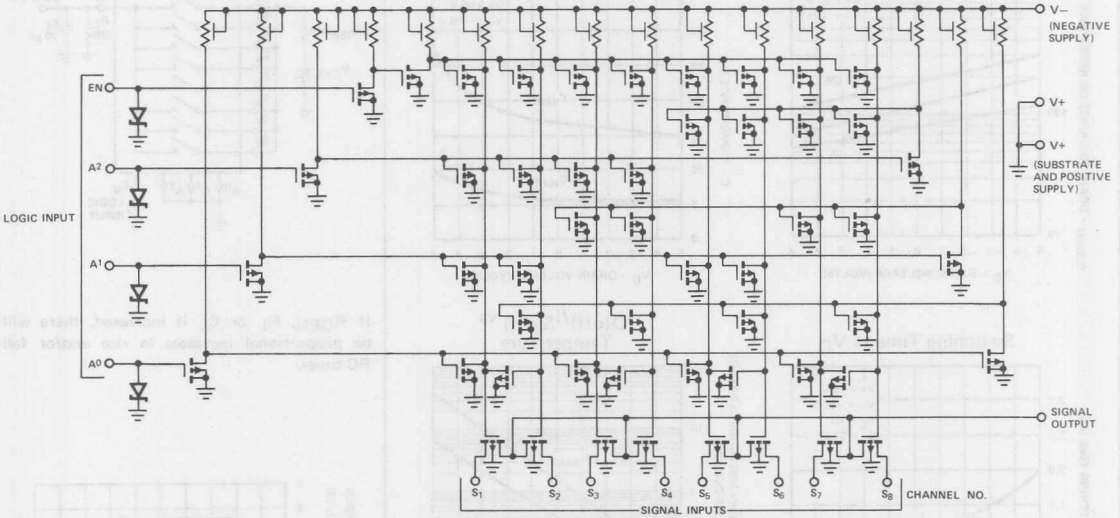


"OFF" ISOLATION = 20 LOG $\frac{|V_{OUT}|}{|V_{IN}|}$



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.




V–
(NEGATIVE
SUPPLY)
V+
V+
(SUBSTRATE
AND POSITIVE
SUPPLY)
EN
A2
A1
A0
LOGIC INPUT
SIGNAL
OUTPUT
S1
S2
S3
S4
S5
S6
S7
S8
CHANNEL NO.
SIGNAL INPUTS

Siliconix

Introduction 0
Interface 1
Telecommunications 2
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Analog Multiplexers 4
Multi-Channel FETs 5
Linear 6
A/D Converters 7
D/A Converters 8
Die Process & Topography 9
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Package Data 11
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MULTI-CHANNEL FETs

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G118	5-7
G119	5-9
G122	5-11
G123	5-13

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Monolithic 6-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals**
- **Multiplexing**

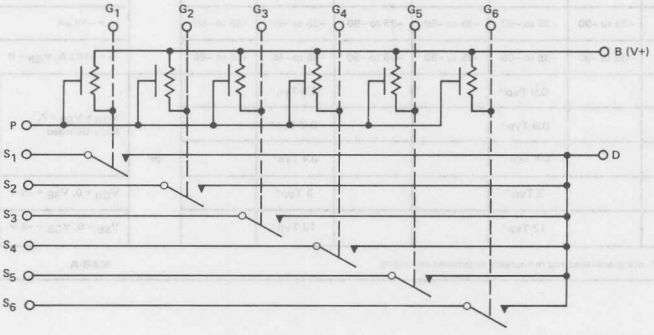
BENEFITS

- **Reduces External Component Requirements**
 - Internal Zener Diode Protects the Gate
 - Six Switches Per Chip
 - Integrated MOS FET for Each Gate to Provide "Pull-Up" Current for Gate-Driver Circuit

DESCRIPTION

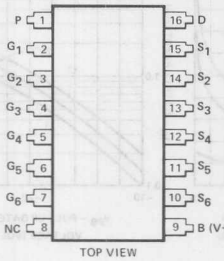
The G115 contains six enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 30 V peak-to-peak. The switches are integrated on a silicon substrate (body). The switches have a common drain terminal (D) which will function equally well as a common source. In the same manner, the source terminals (S) will function equally well as drains. Each gate (G) is provided with a normally OFF "pull-up" MOS FET which may be turned ON to provide a current source to the gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

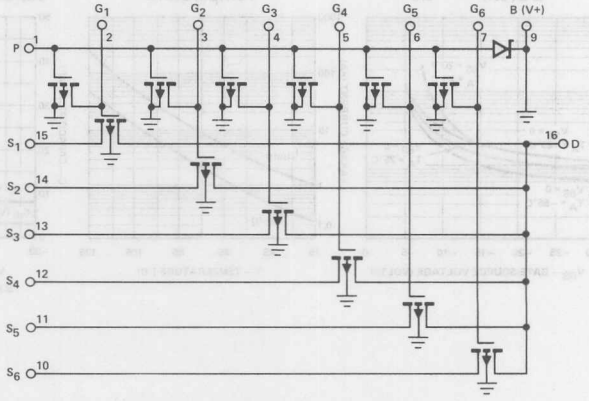
Dual-In-Line Package



TOP VIEW

ORDER NUMBERS: G115AP OR G115BP
SEE PACKAGE 12

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

I_G 5 mA above 75°C.

I_P 100 μA

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

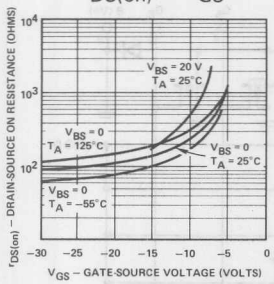
		CHARACTERISTIC		MAX LIMITS G115A −55°C	MAX LIMITS G115A 25°C	MAX LIMITS G115A 125°C	MAX LIMITS G115B −20°C	MAX LIMITS G115B 25°C	MAX LIMITS G115B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0, V_{PB} = 0	
1		$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V	I_S = −1 mA
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V	
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current		−0.5	−500		−5	−500	nA	V_{SD} = −20 V, V_{GD} = 0	
5		$I_{D(off)}$	Drain OFF Leakage Current		−2.5	−2500		−10	−1000		V_{DS} = −20 V, V_{GS} = 0, V_{SB} = 0	
6	STATIC	$I_{G(on)}$	Gate ON Current		−0.8 to −2.4			−0.8 to −2.4		mA	V_{GB} = −30 V, V_{PB} = −30 V	
7	STATIC	I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500	nA	V_{GB} = −20 V	
8	STATIC	$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_D = −10 μA, V_{DG} = 0, V_{SB} = 0	
9		BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −50 μA, V_{GS} = 0, V_{SB} = 0	
10		BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0	
11		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_G = −10 μA	
12		BV_{PBS} Min	Pull-Up Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_P = −10 μA, V_{GB} = 0	
13	DYNAMIC	C_{gs}	Gate-Source Capacitance		0.9 Typ*			0.9 Typ*		pF	V_{DB} = V_{SB} = 0, Body Guarded	Drain Guarded; V_{GB} = 0, f = 1 MHz
14	DYNAMIC	C_{gd}	Gate-Drain Capacitance		0.9 Typ*			0.9 Typ*				Source Guarded; V_{GB} = 0, f = 1 MHz
15	DYNAMIC	$C_{ds(off)}$	Drain-Source OFF Capacitance		0.4 Typ*			0.4 Typ*				Gate Guarded; V_{GB} = 0, f = 1 MHz
16	DYNAMIC	C_{sb}	Source-Body Capacitance		2 Typ*			2 Typ*			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded; V_{GB} = 0, f = 1 MHz
17	DYNAMIC	C_{db}	Drain-Body Capacitance		12 Typ*			12 Typ*			V_{SB} = 0, V_{DB} = −5 V	Gate and Source Guarded; V_{GB} = 0, f = 1 MHz

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

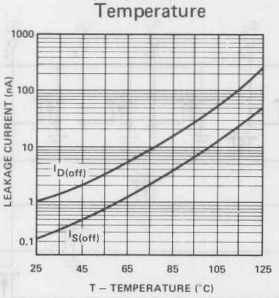
MAB-A

TYPICAL CHARACTERISTICS

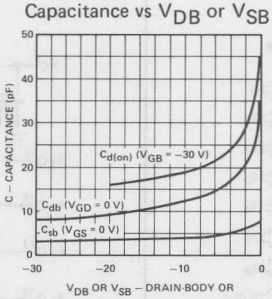
$r_{DS(on)}$ vs V_{GS}



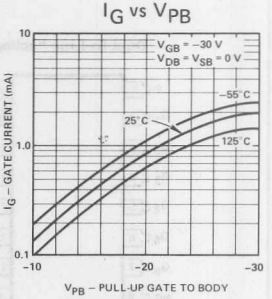
$I_{S(off)}$, $I_{D(off)}$ vs Temperature



Capacitance vs V_{DB} or V_{SB}



I_G vs V_{PB}



Monolithic 5-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals**
- **Multiplexing**

BENEFITS

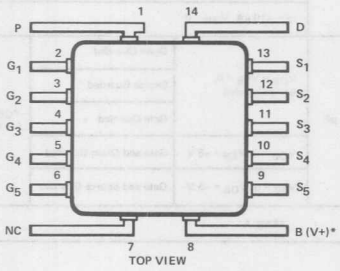
- **Reduces External Component Requirements**
 - Internal Zener Diode Protects the Gate
 - Five Switches Per Chip
 - Integrated MOS FET for Each Gate to Provide "Pull-Up" Current for Gate-Driver Circuit

DESCRIPTION

The G116 contains five enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 30 V peak-to-peak. The switches are integrated on a silicon substrate (body). The switches have a common drain terminal (D) which will function equally well as a common source. In the same manner, the source terminals (S) will function equally well as drains. Each gate (G) is provided with a normally OFF "pull-up" MOS FET which may be turned ON to provide a current source to the gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively. It is recommended that the G115 be used for new designs.

PIN CONFIGURATIONS

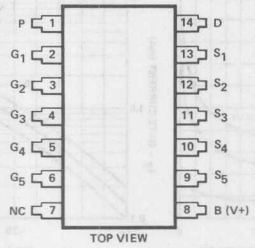
Flat Package



ORDER NUMBER: G116AL
SEE PACKAGE 5

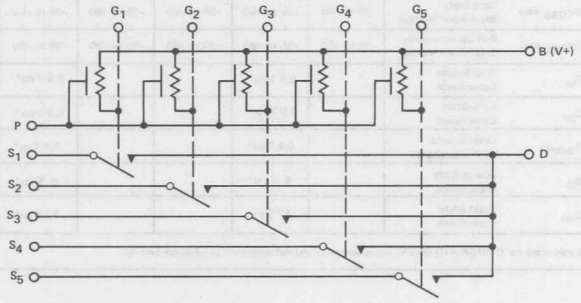
*Common to Substrate and Base of Package

Dual-In-Line Package

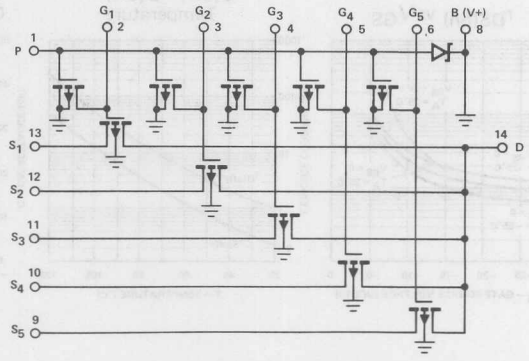


ORDER NUMBER: G116AP
SEE PACKAGE 11

FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_B to V_S −2 to 30 V
V_B to V_D −2 to 30 V
V_D to V_S ±30 V
V_B to V_G, V_B to V_P 35 V
I_S, I_D 100 mA
I_G 5 mA
I_P 100 μA
Storage Temperature. −65 to 150°C
Operating Temperature −55 to 125°C
Power Dissipation*
Flat Package** 750 mW
14 Pin DIP*** 825 mW

*All leads soldered or welded to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

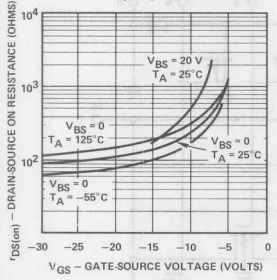
		CHARACTERISTIC		MAX LIMITS G116A −55°C	G116A 25°C	G116A 125°C	G116B −20°C	G116B 25°C	G116B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0, V_{PB} = 0		
1	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V	I_S = −1 mA	
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V		
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V		
4		$I_{S(off)}$	Source OFF Leakage Current		−0.5	−500		−5	−500	nA	V_{SD} = −20 V, V_{GD} = 0		
5		$I_{D(off)}$	Drain OFF Leakage Current		−2.5	−2500		−10	−1000		V_{DS} = −20 V, V_{GS} = 0, V_{SB} = 0		
6		$I_{G(on)}$	Gate ON Current		−0.8 to −2.4			−0.8 to −2.4		mA	V_{GB} = −30 V, V_{PB} = −30 V		
7		I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500	nA	V_{GB} = −20 V		
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.4 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_D = −10 μA, V_{SB} = 0, V_{DG} = 0		
9		BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −50 μA, V_{GS} = 0, V_{SB} = 0		
10		BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0		
11		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_G = −10 μA		
12		BV_{PBS} Min	Pull-Up Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_P = −10 μA, V_{GB} = 0		
13	DYNAMIC	C_{gs}	Gate-Source Capacitance		0.9 Typ*			0.9 Typ*		pF	V_{DB} = V_{SB} = 0, Body Guarded	Drain Guarded	V_{GB} = 0 f = 1 MHz
14		C_{gd}	Gate-Drain Capacitance		0.9 Typ*			0.9 Typ*				Source Guarded	
15		$C_{ds(off)}$	Drain-Source OFF Capacitance		0.4 Typ*			0.4 Typ*				Gate Guarded	
16		C_{sb}	Source-Body Capacitance		6 Typ*			6 Typ*			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded	
17		C_{db}	Drain-Body Capacitance		12 Typ*			12 Typ*			V_{SB} = 0, V_{DB} = −5 V	Gate and Source Guarded	

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

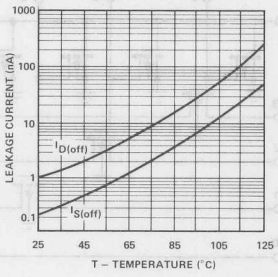
MAB-A

TYPICAL CHARACTERISTICS

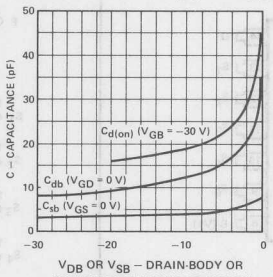
$r_{DS(on)}$ vs V_{GS}



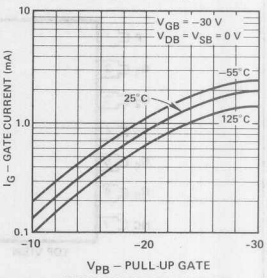
$I_{S(off)}$, $I_{D(off)}$ vs Temperature



Capacitance vs V_{DB} or V_{SB}



I_G vs V_{PB}



Monolithic 5-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals**
- **Multiplexing with Enable Switch**

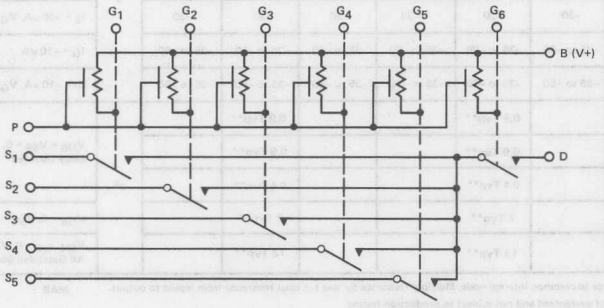
BENEFITS

- **Reduces External Component Requirements**
 - Internal Zener Diode Protects the Gate
 - Five Switches Per Chip
 - Integrated MOS FET for Each Gate to Provide "Pull-Up" Current for Gate-Driver Circuit

DESCRIPTION

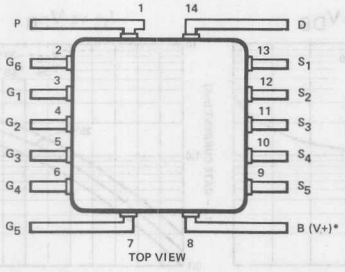
The G117 contains six enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. The switches are integrated on a silicon substrate (body). The drains of five of the switches are internally connected to the source of the sixth switch. This arrangement is intended for use of the device as a 5-channel first-level and one-channel second-level multiplexer. Each of the six gates are provided with an internal "pull-up" current which may be turned ON or OFF by connecting the pull-up control terminal (P) to a negative supply or to the body (B) terminal.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

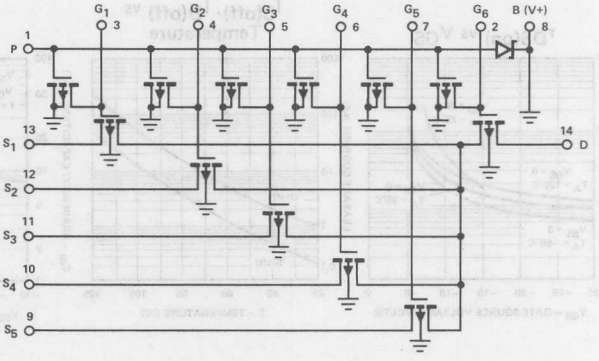
Flat Package



ORDER NUMBER: G117AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

SCHEMATIC DIAGRAM



I_S, I_D	100 mA	*All leads soldered or welded to PC board. Derate
I_G	5 mA	10 mW/°C above 75°C.
I_P	100 μA	

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

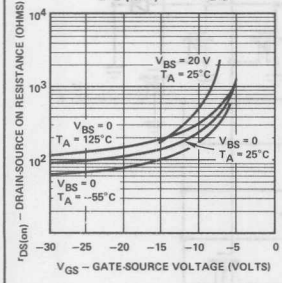
		CHARACTERISTIC		MAX LIMITS G117A −55°C	G117A 25°C	G117A 125°C	G117B −20°C	G117B 25°C	G117B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0, V_{PB} = 0	
1		$r_{DS(on)}$*	Drain-Source ON Capacitance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V	I_S = −1 mA, V_{G6D} = V_{GD}
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V	
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V	
4	STATIC	$I_{S(off)}$	Source OFF Leakage Current		−0.5	−500		−5	−10	nA	V_{SD} = −20 V, V_{GD} = 0	
5		$I_{D(off)}$	Drain OFF Leakage Current		−2.5	−2500		−10	−500		V_{DS} = −20 V, V_{GS} = 0, V_{G6S} = −30 V, V_{SB} = 0	
6		$I_{D(off)}$	Drain OFF Leakage Current		−0.5	−500		−5	−100		V_{DS} = −20 V, V_{GS} = −30 V, V_{G6B} = 0, V_{SB} = 0	
7		$I_{G(on)}$	Gate ON Current		−0.8 to −2.4			−0.8 to −2.4		mA	V_{GB} = −30 V, V_{DB} = −30 V	
8		I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500	nA	V_{GB} = −20 V	
9		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_S = 10 μA, V_{DG1-5} = 0, V_{GB6} = −20 V	
10		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0		I_{S1} = 10 μA, V_{DG6} = 0, V_{GB1} = −20 V	
11		BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −50 μA, V_{GS} = 0, V_{SB} = 0	
12		BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0	
13		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_G = −10 μA	
14		BV_{PBS} Min	Pull-Up Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_P = −10 μA, V_{GB} = 0	
15	DYNAMIC	C_{gs}	Gate-Source Capacitance		0.9 Typ**			0.9 Typ**		pF	V_{DB} = V_{SB} = 0, Body Guarded	Drain Guarded; V_{GB} = 0, f = 1 MHz
16		C_{gd}	Gate-Drain Capacitance		0.9 Typ**			0.9 Typ**				Source Guarded
17		$C_{ds(off)}$*	Drain-Source OFF Capacitance		0.4 Typ**			0.4 Typ**				Gate Guarded
18		C_{sb}	Source-Body Capacitance		2 Typ**			2 Typ**			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded
19		C_{db}	Drain-Body Capacitance		12 Typ**			12 Typ**			$V_{S(1-5)B}$ = 0, $V_{G(1-5)B}$ = 0, V_{G6B} = −30 V, V_{DB} = −5 V, All Gates and Sources Guarded	

*This is resistance (capacitance) from each source to common internal node. Multiply resistance by two for total resistance from inputs to output.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

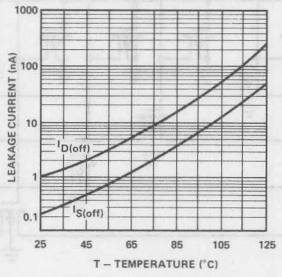
MAB

TYPICAL CHARACTERISTICS

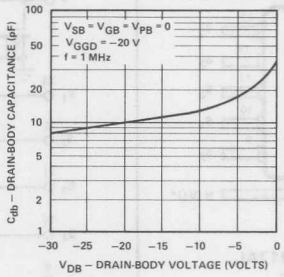
$r_{DS(on)}$ vs V_{GS}



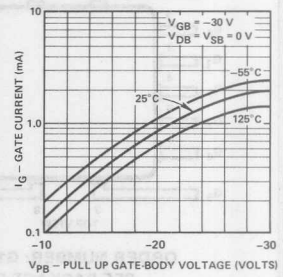
$I_{S(off)}$, $I_{D(off)}$ vs Temperature



C_d vs V_{DB}



I_G vs V_{PB}



Monolithic 6-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals**
- **Multiplexing**

BENEFITS

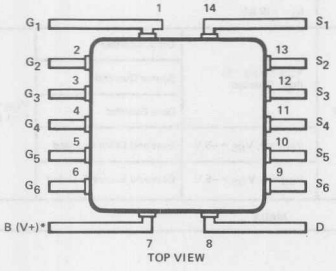
- **Reduces External Component Requirements**
 - Internal Zener Diode Protects the Gate
 - Six Switches Per Chip

DESCRIPTION

The G118 contains six enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. The switches are integrated on a common substrate (body). They have a common drain terminal (D) which will function equally well as a common source; likewise, the source terminals will function as drains.

PIN CONFIGURATIONS

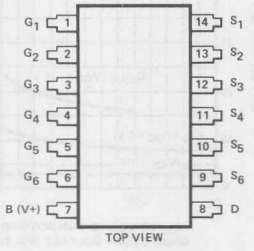
Flat Package



ORDER NUMBER: G118AL
SEE PACKAGE 5

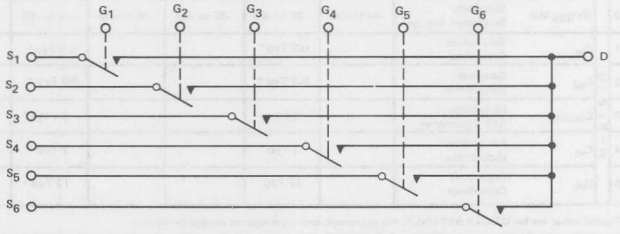
*Common to Substrate and Base of Package

Dual-In-Line Package

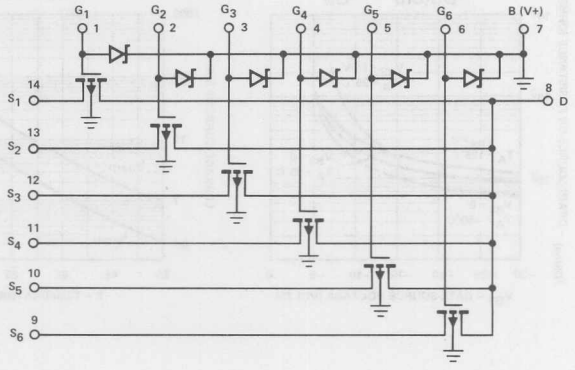


ORDER NUMBER: G118AP
SEE PACKAGE 11

FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_B to V_S −2 to 30 V
V_B to V_D −2 to 30 V
V_D to V_S ±30 V
V_B to V_G 35 V
I_S, I_D 100 mA
I_G 5 mA
Storage Temperature −65 to 150°C

Operating Temperature (A Suffix) −55 to 125°C
(B Suffix) −20 to 85°C
Power Dissipation*
Flat Package** 750 mW
14 Pin DIP*** 825 mW
*All leads soldered or welded to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

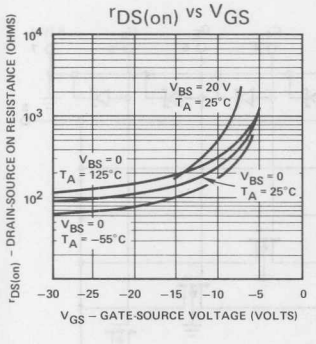
		CHARACTERISTIC		MAX LIMITS G118A −55°C	G118A 25°C	G118A 125°C	G118B −20°C	G118B 25°C	G118B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0		
1	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V		
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V	I_S = −1 mA	
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V		
4		$I_{S(off)}$	Source OFF Leakage Current		−0.5	−500		−5	−500	nA	V_{SD} = −20 V, V_{GD} = 0		
5		$I_{D(off)}$	Drain OFF Leakage Current		−3	−3000		−10	−1000		V_{DS} = −20 V, V_{GS} = 0, V_{SB} = 0		
6		I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500		V_{GB} = −20 V		
7		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_D = −10 μA, V_{GD} = 0, V_{SB} = 0		
8		BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −50 μA, V_{GS} = 0, V_{SB} = 0		
9		BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0		
10		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_G = −10 μA		
11	DYNAMIC	C_{gs}	Gate-Source Capacitance		0.9 Typ*			0.9 Typ*		pF	V_{DB} = V_{SB} = 0, Body Guarded	Drain Guarded	V_{GB} = 0 f = 1 MHz
12		C_{gd}	Gate-Drain Capacitance		0.9 Typ*			0.9 Typ*				Source Guarded	
13		$C_{ds(off)}$	Drain-Source OFF Capacitance		0.4 Typ*			0.4 Typ*				Gate Guarded	
14		C_{sb}	Source-Body Capacitance		2 Typ*			2 Typ*			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded	
15		C_{db}	Drain-Body Capacitance		12 Typ*			12 Typ*			V_{SB} = 0, V_{DB} = −5 V	Gate and Source Guarded	

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

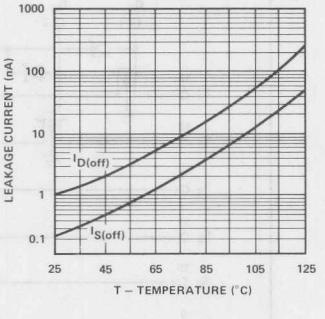
MABA

TYPICAL CHARACTERISTICS

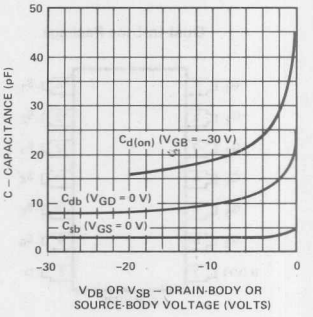
$r_{DS(on)}$ vs V_{GS}



$I_{S(off)}$, $I_{D(off)}$ vs Temperature



Capacitance vs V_{DB} or V_{SB}



Monolithic 6-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals such as Differential Inputs**
- **Multiplexing**

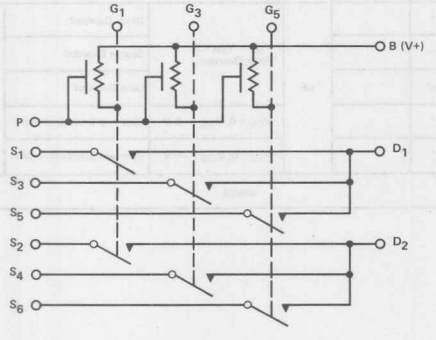
BENEFITS

- **Reduces External Component Requirements**
 - Internal Zener Diode Protects the Gate
 - Six Switches Per Chip
 - Integrated MOS FET for Each Gate to Provide "Pull-Up" Current for Gate-Driver Circuit

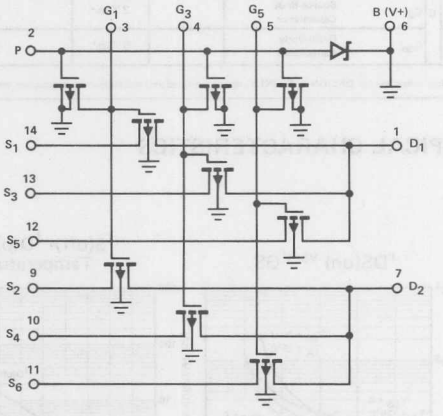
DESCRIPTION

The G119 contains six enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 30 V peak-to-peak. The switches are integrated onto a silicon substrate (body) and are internally connected into two groups of three switches per group. This arrangement facilitates the switching or multiplexing of differential analog signals. Each group has a common drain terminal (D_1 and D_2) which will function equally well as a common source. Each gate terminal (G) controls a pair of switches and is provided with a normally-OFF "pull-up" MOS FET which may be turned ON to provide a current source to the gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively.

FUNCTIONAL DIAGRAM



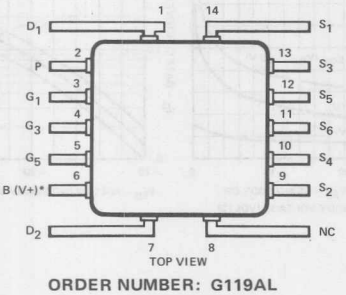
SCHEMATIC DIAGRAM



PIN CONFIGURATION

Flat Package

PIN CONFIGURATION



ORDER NUMBER: G119AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

V_B to V_G, V_B to V_P	35 V
I_S, I_D	100 mA
I_G	5 mA

*All leads soldered or welded to PC board. Derate 10 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

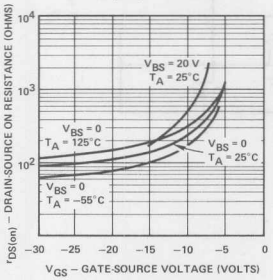
		CHARACTERISTIC		MAX LIMITS G119A −55°C	G119A 25°C	G119A 125°C	G119B −20°C	G119B 25°C	G119B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0, V_{PB} = 0		
1		$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V	I_S = −1 mA	
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V		
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V		
4	STATIC	$I_{S(off)}$	Source OFF Leakage Current		−0.5	−500		−5	−500	nA	V_{SD} = −20 V, V_{GD} = 0		
5		$I_{D(off)}$	Drain OFF Leakage Current		−1.5	−1500		−10	−1000		V_{DS} = −20 V, V_{GS} = 0, V_{SB} = 0		
6		$I_{G(on)}$	Gate ON Current		−0.8 to −2.4			−0.8 to −2.4		mA	V_{GB} = −30 V, V_{PB} = −30 V		
7		I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500	nA	V_{GB} = −20 V		
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_D = −10 μA, V_{SB} = 0, V_{GD} = 0		
9	SUPPLY	BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −50 μA, V_{GS} = 0, V_{SB} = 0		
10		BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0		
11		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_G = −10 μA		
12		BV_{PBS} Min	Pull-Up Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_P = −10 μA, V_{GB} = 0		
13	DYNAMIC	C_{gs}	Gate-Source Capacitance		1.8 Typ*			1.8 Typ*		pF	V_{DB} = V_{SB} = 0, Body Guarded	Drain Guarded	V_{GB} = 0 f = 1 MHz
14		C_{gd}	Gate-Drain Capacitance		1.8 Typ*			1.8 Typ*				Source Guarded	
15		$C_{ds(off)}$	Drain-Source OFF Capacitance		0.4 Typ*			0.4 Typ*				Gate Guarded	
16		C_{sb}	Source-Body Capacitance		2 Typ*			2 Typ*			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded	
17		C_{db}	Drain-Body Capacitance		6 Typ*			6 Typ*			V_{SB} = 0, V_{DB} = −5 V	Gate and Source Guarded	

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

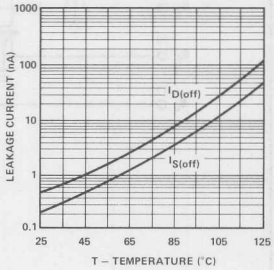
MABB

TYPICAL CHARACTERISTICS

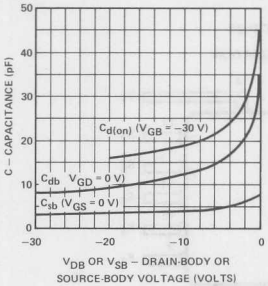
$r_{DS(on)}$ vs V_{GS}



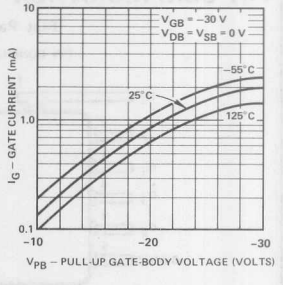
$I_{S(off)}$, $I_{D(off)}$ vs Temperature



Capacitance vs V_{DB} or V_{SB}



I_G vs V_{PB}



Monolithic 4-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals such as Differential Inputs**
- **Multiplexing**

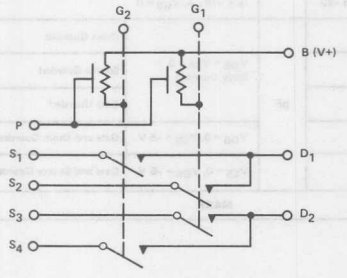
BENEFITS

- **Reduces External Component Requirements**
 - Internal Zener Diode Protects the Gate
 - Four Switches Per Chip
 - Integrated MOS FET for Each Gate to Provide "Pull-Up" Current for Gate-Driver Circuit

DESCRIPTION

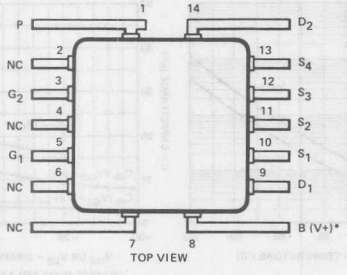
The G122 contains four enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 30 V peak-to-peak. The switches are integrated onto a silicon substrate (body) and are internally connected into two groups of two switches per group. This arrangement facilitates the switching or multiplexing of differential analog signals. Each group has a common drain terminal (D_1 and D_2) which will function equally well as a common source. Each gate terminal (G) controls a pair of switches and is provided with a normally-OFF "pull-up" MOS FET which may be turned ON to provide a current source to a gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

Flat Package

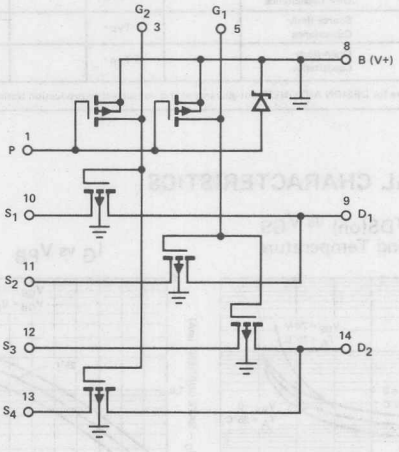


TOP VIEW

ORDER NUMBER: G122AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_B to V_S	−2 to 30 V
V_B to V_D	−2 to 30 V
V_D to V_S	±30 V
V_B to V_G or V_P	35 V
I_S, I_D	100 mA
I_G	5 mA
I_P	100 μA

Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	750 mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

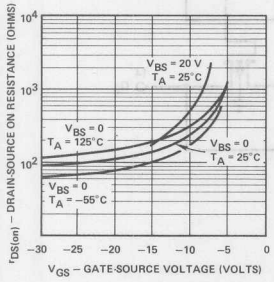
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX −20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0, V_{PB} = 0		
1	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V		
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V	I_S = −1 mA	
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V		
4		$I_{S(off)}$	Source OFF Leakage Current		0.5	−500		−5	−500	nA	V_{SD} = −20 V, V_{GD} = 0		
5		$I_{D(off)}$	Drain OFF Leakage Current		−1	−1000		−10	−1000		V_{DS} = −20 V, V_{GS} = 0, V_{SB} = 0		
6		$I_{G(on)}$	Gate ON Current		−0.8 to −2.4			−0.8 to −2.4		mA	V_{GB} = −30 V, V_{PB} = −30 V		
7		I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500	nA	V_{GB} = −20 V		
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_D = −10 μA, V_{GD} = 0, V_{SB} = 0		
9		BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −10 μA, V_{GS} = 0, V_{SB} = 0		
10		BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0		
11		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_S = −10 μA		
12		BV_{PBS} Min	Pull-Up Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_P = −10 μA, V_{GB} = 0		
13	DYNAMIC	C_{gs}	Gate-Source Capacitance		1.8 Typ*			1.8 Typ*		pF	V_{DB} = V_{SB} = 0 Body Guarded	Drain Guarded	V_{GB} = 0 f = 1 MHz
14		C_{gd}	Gate-Drain Capacitance		1.8 Typ*			1.8 Typ*				Source Guarded	
15		$C_{ds(off)}$	Drain-Source OFF Capacitance		0.4 Typ*			0.4 Typ*				Gate Guarded	
16		C_{sb}	Source-Body Capacitance		2 Typ*			2 Typ*			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded	
17		C_{db}	Drain-Body Capacitance		6 Typ*			6 Typ*			V_{SB} = 0, V_{DB} = −5 V	Gate and Source Guarded	

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

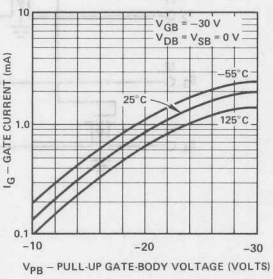
MABB

TYPICAL CHARACTERISTICS

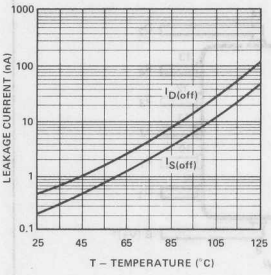
$r_{DS(on)}$ vs V_{GS} and Temperature



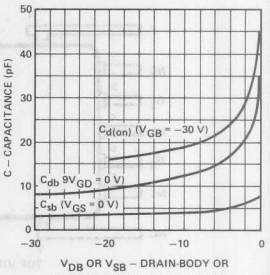
I_G vs V_{PB}



$I_{S(off)}$ vs Temperature



Capacitance vs V_{DB} and V_{GS}



Monolithic 4-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals**
- **Multiplexing**

BENEFITS

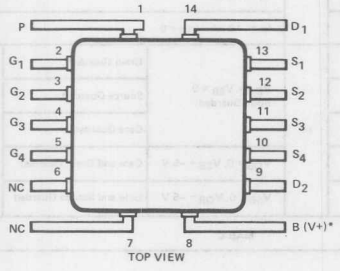
- **Reduces External Component Requirements**
 - Internal Zener Diode Protects the Gate
 - Four Switches Per Chip
 - Intergrated MOS FET for Each Gate to Provide "Pull-Up" Current for Gate-Driver Circuit

DESCRIPTION

The G123 contains four enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. The switches are integrated on a silicon substrate (body). Separate source and gate connections are provided for each switch; the drains are connected in pairs to two drain terminals. Functions of the drain and source terminals may be interchanged with comparable performance. Each gate terminal (G) is provided with a normally-OFF "pull-up" MOS FET which may be turned ON to provide a current source to a gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively.

PIN CONFIGURATIONS

Flat Package

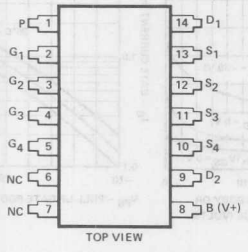


TOP VIEW

ORDER NUMBER: G123AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

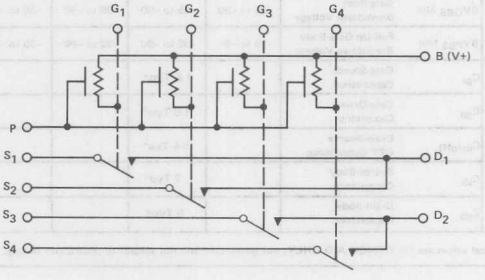
Dual-In-Line Package



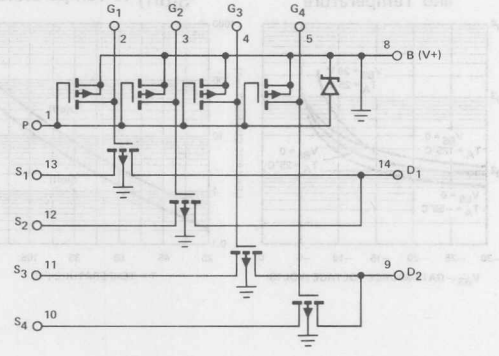
TOP VIEW

ORDER NUMBERS: G123AP OR G123BP
SEE PACKAGE 11

FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM



V_D to V_S	±30 V
V_B to V_G or V_P	35 V
I_S, I_D	100 mA
I_G	5 mA
I_P	100 μA
Storage Temperature	−65 to 150°C

14 Pin DIP***	825 mW

*All leads soldered or welded or PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

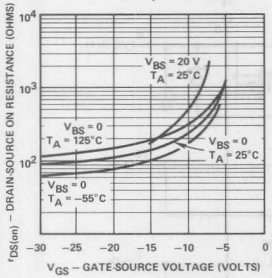
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX −20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0, V_{PB} = 0		
1		$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V		
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V	I_S = −1 mA	
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V		
4		$I_{S(off)}$	Source OFF Leakage Current		−0.5	−500		−5	−500	nA	V_{SD} = −20 V, V_{GD} = 0		
5		$I_{D(off)}$	Drain OFF Leakage Current		−1	−1000		−10	−1000		V_{DS} = −20 V, V_{GS} = 0, V_{SB} = 0		
6	STATIC	$I_{G(on)}$	Gate ON Current		−0.8 to −2.4			−0.8 to −2.4		mA	V_{GB} = −30 V, V_{PB} = −30 V		
7		I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500	nA	V_{GB} = −20 V		
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_D = −10 μA, V_{GD} = 0, V_{SB} = 0		
9		BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −10 μA, V_{GS} = 0, V_{SB} = 0		
10		BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0		
11		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_G = −10 μA		
12		BV_{PBS} Min	Pull-Up Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_P = −10 μA, V_{GB} = 0		
13		C_{gs}	Gate-Source Capacitance		1.8 Typ*			1.8 Typ*		pF	V_{DB} = V_{SB} = 0 Body Guarded	Drain Guarded	V_{GB} = 0 f = 1 MHz
14	DYNAMIC	C_{gd}	Gate-Drain Capacitance		1.8 Typ*			1.8 Typ*				Source Guarded	
15		$C_{ds(off)}$	Drain-Source OFF Capacitance		0.4 Typ*			0.4 Typ*				Gate Guarded	
16		C_{sb}	Source-Body Capacitance		2 Typ*			2 Typ*			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded	
17		C_{db}	Drain-Body Capacitance		6 Typ*			6 Typ*			V_{SB} = 0, V_{DB} = −5 V	Gate and Source Guarded	

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

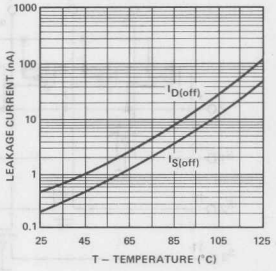
MAB-C

TYPICAL CHARACTERISTICS

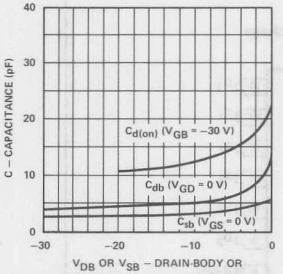
$r_{DS(on)}$ vs V_{GS} and Temperature



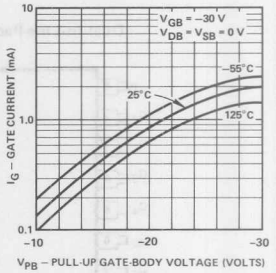
$I_{S(off)}$ vs Temperature



Capacitance vs V_{DB} and V_{GS}



I_G vs V_{PB}



Siliconix

Introduction 0
Interface 1
Telecommunications 2
Analog Switches 3
Analog Multiplexers 4
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LINEAR

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Si1525B/27B, Si2525B/27B, Si3525B/27B	6-22

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Low-Power Triple Operational Amplifier

Siliconix

designed for . . .

- **Instrumentation Amplifiers**
- **Buffer Amplifiers**
- **Voltage Comparators**
- **Low-Drift Sample and Hold Circuits**
- **Active Filters**
- **Battery-Powered Circuits**

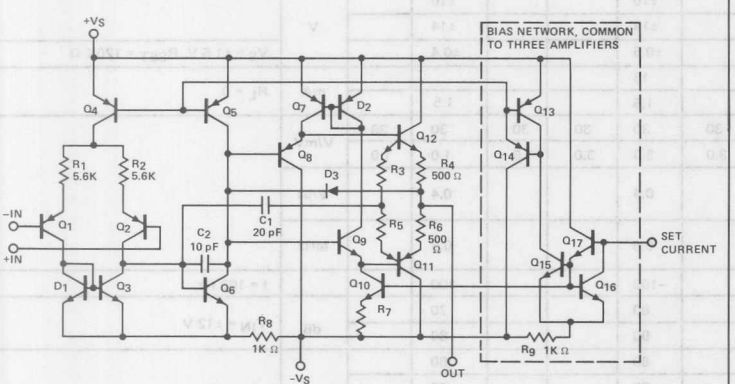
BENEFITS

- **Low Cost and Compact**
 - 3 Amplifiers in One Package
- **Easily Tailored to Optimize Circuit Performance**
 - Programmed Supply Current
 - Operates with ±1.5 V to ±15 V
- **Very Rugged**
 - ±30 V Differential Input Voltage Range
 - Drives Large Capacitive Loads < 1000 pF
 - Continuous Short Circuit Protection

DESCRIPTION

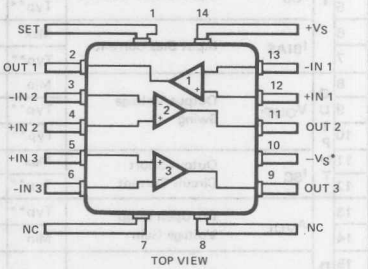
The L144 is a monolithic low-power triple operational amplifier stabilized for all feedback configurations and capacitive loads by internal gain compensation. Low power requirements permit high voltage operation across the rated temperature range, as well as battery operation from ±1.5 V.

SCHEMATIC DIAGRAM (One Amplifier)



PIN CONFIGURATIONS

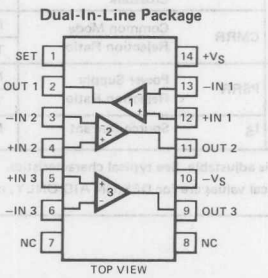
Flat Package



*COMMON TO SUBSTRATE AND BASE OF PACKAGE

ORDER NUMBERS: L144AL OR L144BL
SEE PACKAGE 5

Dual-In-Line Package



ORDER NUMBERS: L144AP OR L144BP
SEE PACKAGE 11

L144CJ
SEE PACKAGE 7

ABSOLUTE MAXIMUM RATINGS

Output Short Circuit Duration Indefinite
Operating Temperature (A Suffix) . . . −55 to +125°C
(B Suffix) −20 to +85°C
(C Suffix) 0 to +70°C
Storage Temperature (A and B Suffix). . . −65 to 150°C
(C Suffix) −65 to 125°C
Lead Temperature (Soldering, 60 Sec) 300°C
Power Dissipation (Package)***
Flat Package 750 mW
14 Pin DIP 825 mW
Plastic DIP 470 mW

***All leads welded or soldered to P.C. board. Derate 10 mW/°C for the flat package, 11 mW/°C for the 14 pin DIP above +75°C and 6.3 mW/°C above 25°C for the plastic DIP.

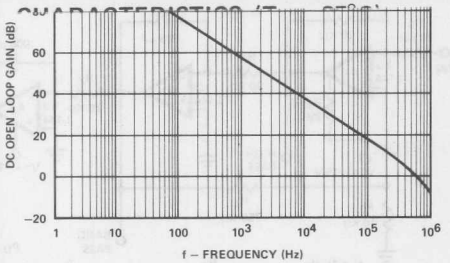
ELECTRICAL CHARACTERISTICS

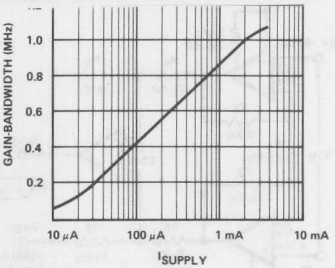
All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC			L144A/B			L144C			UNIT	TEST CONDITIONS, UNLESS NOTED: $V_S = \pm 15$ V, $R_L = 50$ KΩ, $R_{SET} = 3$ MΩ* Pin 1 to Pin 14
					−55°C/ −20°C	25°C	125°C/ 85°C	0°C	25°C	70°C		
1	INPUT	V_{OS}	Input Offset Voltage	Max	6	5	6		10		mV	$R_S \leq 50K\ \Omega$
2				Typ**		1			1			
3		dV_{OS}/dT	Average Temperature Coefficient of Input Offset Voltage	Typ**		3.3			3.3		µV/°C	$R_S \leq 50K\ \Omega$
4		I_{OS}	Input Offset Current	Max		50			70		nA	
5				Typ**		2			5			
6		I_{BIAS}	Input Bias Current	Max	−200	−200		−250	−250			
7				Typ**		−100			−125			
8	OUTPUT	V_{OUT}	Output Voltage Swing	Min		±10			±10		V	
9				Typ**		±14			±14			
10				Typ**		±0.5			±0.4			$V_S = \pm 1.5$ V, $R_{SET} = 120K\ \Omega$
11		I_{SC}	Output Short Circuit Current	Max		15					mA	$R_L = 0$
12				Typ**		1.5			1.5			
13	DYNAMIC	A_{VOL}	DC Open Loop Voltage Gain	Typ**	30	30	30	30	30	30	V/mV	
14				Min	3.0	3.0	3.0	1.0	1.0	1.0		
15		S_r	Slew Rate	Typ**		0.4			0.4		V/µs	
16												
17			Unity Gain Bandwidth	Typ**		0.6			0.6		MHz	
18												
19			Crosstalk	Typ**		−100			−100			f = 100 Hz
20		CMRR	Common Mode Rejection Ratio	Min		80			70		dB	$V_{IN} = \pm 12$ V
21				Typ**		90			80			
22	SUP	PSRR	Power Supply Rejection Ratio	Min		80			80			
23				Typ**		90			90			
24		I_S	Source Current	Max		350			400		µA	Unity Gain $V_{IN+} = 0$ on all amps

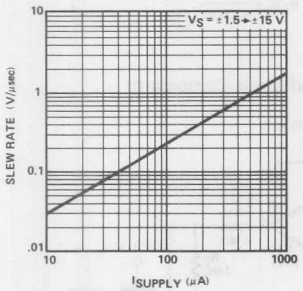
*I_{CC} is adjustable. See typical characteristics.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

CMAC

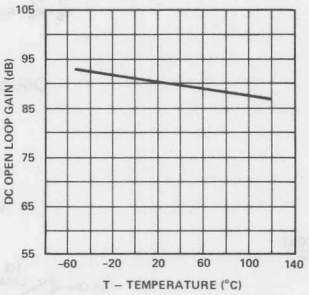




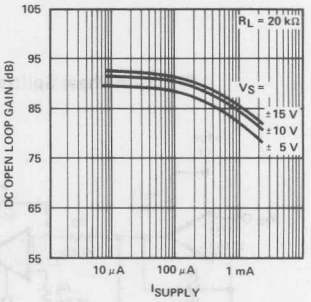
Slew Rate vs
Supply Current



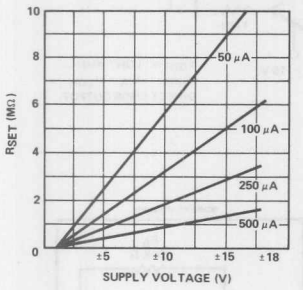
DC Open Loop Gain
vs Temperature



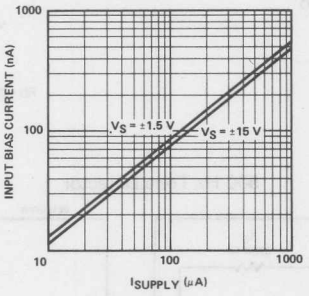
DC Open Loop Gain
vs Supply Current



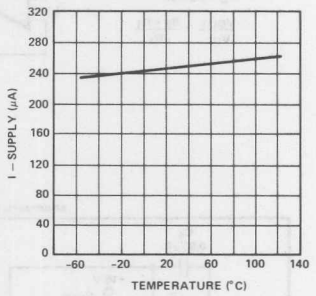
Supply Current vs Set
Resistor and Supply Voltage



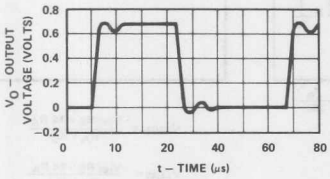
Input Bias Current vs
Supply Current



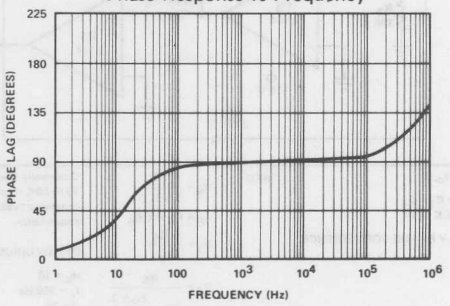
Supply Current vs
Temperature



Voltage Follower
Small Signal Pulse Response

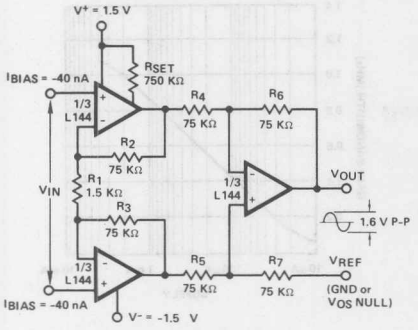


Phase Response vs Frequency



APPLICATIONS

Instrumentation Amplifier

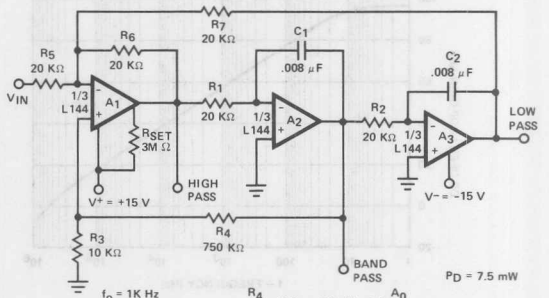


$A_V = 1 + \frac{2R_2}{R_1}$

$P_D = 135\ \mu W$

V_{OS} (TYP) RTI = 0.45 mV

Active Filter



$P_D = 7.5$ mW

$f_o = 1$K Hz
$Q = 26$
$H_o = 26$

$Q_{max} < \frac{A_0}{5}$

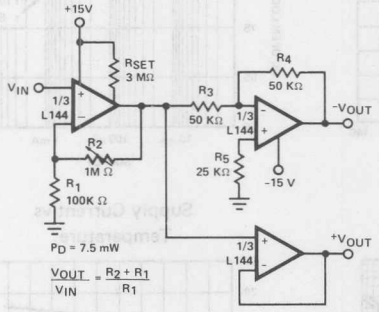
$C_1 = C_2$
$R_5 = R_6 = R_7$

$\frac{R_4}{R_3} = 3 H_o - 1\ f_o, H_o << \frac{A_0}{3}$

$R_2 C_2 = \frac{H_o}{2\pi f_o Q}$

$R_1 C_1 = \frac{Q}{2\pi f_o H_o}$

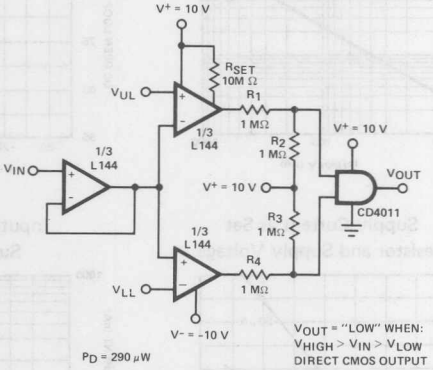
Precision Phase Splitter



$P_D = 7.5$ mW

$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_1}{R_1}$

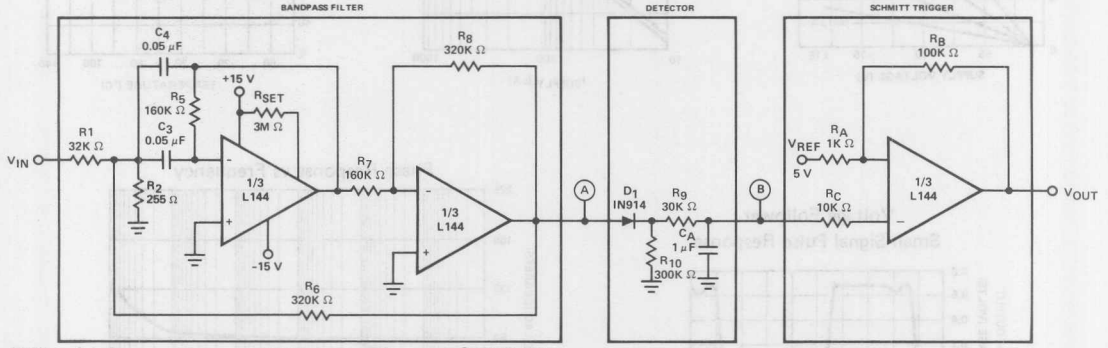
Double-Ended Limit Comparator



$P_D = 290\ \mu W$

V_{OUT} = "LOW" WHEN:
$V_{HIGH} > V_{IN} > V_{LOW}$
DIRECT CMOS OUTPUT

500 Hz Tone Detector



GIVEN Q, f_o, C

LET $C = C_3 = C_4$, $1 \leq K \leq 10$

THEN $R_7 = R_5$ FOR CONVENIENCE

THEN

$R_5 = \frac{Q}{2\pi f_o C}$

$R_8 = R_6 = K R_5$

$R_1 = \frac{K R_5}{H_o}$

$R_2 = \frac{R_5}{Q2 - \frac{H_o + 1}{K}}$

Q normally from 10 to 50K chosen for component value convenience.

IN THIS CIRCUIT:

$H_o = 10$
$f_o = 500$ Hz
$Q = 25$

$f_{3db} = \frac{f_o}{100}$

$V_{HIGH} = \frac{V_{ref} R_B + 14 R_A}{R_A + R_B}$

$V_{LOW} = \frac{V_{ref} R_B - 14 R_A}{R_A + R_B}$

Siliconix

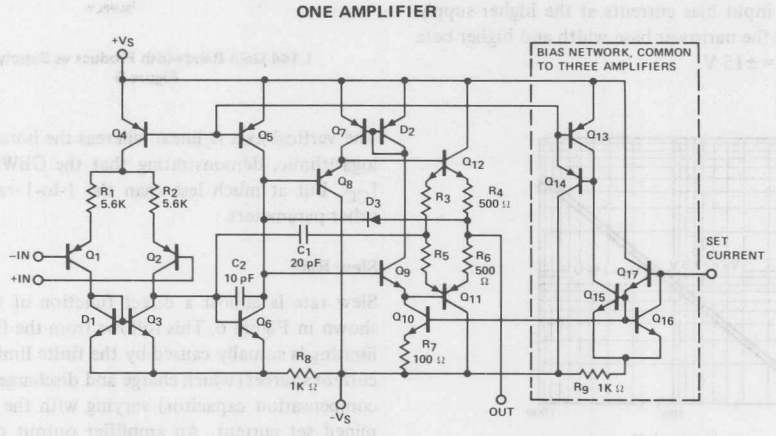
Function/Application of the L144 Programmable Micropower Triple Op Amp

INTRODUCTION

The L144 is a monolithic triple operational amplifier circuit with an external programming feature for power dissipation and input bias current control. It finds application in RC active filters, instrumentation amplifiers, micropower comparators, and numerous general signal processing circuits. The L144 is a practical industry standard op amp wherever low current drain, low voltage, low power, or very small physical size are the controlling criteria.

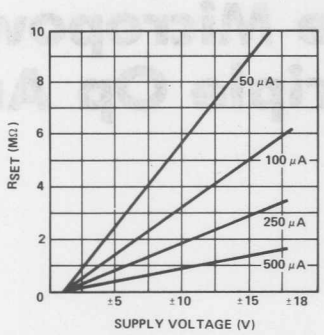
This Application Note describes the L144, how to program it, what the effects of slew rate limiting are, and some practical circuit applications.

The L144 has three operational amplifiers programmed by one external current setting resistor. It operates from power supplies ranging from ±18 V to as low as ±1.5 V with quiescent supply currents of from 10.μA to greater than 1 mA independent of supply voltage. The schematic shown in Figure 1 reveals a general-purpose PNP input transistor op amp with an outstanding difference. The master bias current is not set by an internal resistor strung from V^+ to V^-, but is brought out to an external pin. This allows the user to determine the operating currents of each stage through a system of current mirrors. Of special interest to the designer are the equal collector currents of Q_1 and Q_2, which are derived from the output of Q_4. These collector currents, divided by a beta of approximately 50, determine the input bias currents for each amplifier. The ratio between the set current and the collector current of Q_4 is unity, which allows one to program the input bias current simply by changing the set current input of the device.

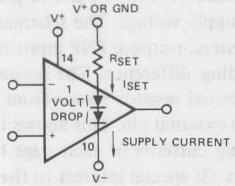


L144 Schematic
Figure 1

6 Linear



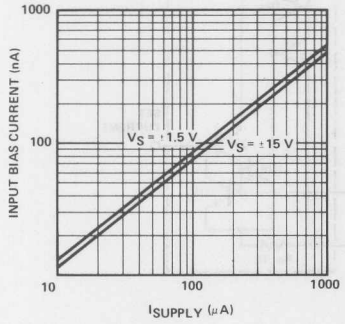
L144 SET CURRENT MODEL



Supply Current vs Bias Resistor and Supply Voltage
Figure 2

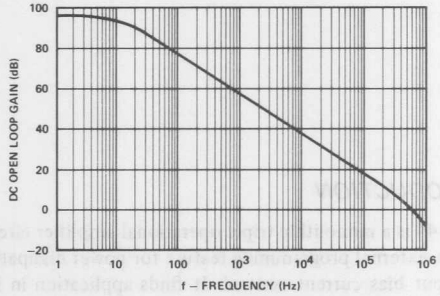
Figure 3 shows the essentially linear relationship between input bias current and total quiescent supply current for the L144. The low input bias currents at low supply current levels allow the L144 to maintain good input specifications even with the large feedback and load resistor values normally encountered in micropower applications.

The slightly lower input bias currents at the higher supply voltages are due to the narrower base width and higher beta encountered at $V_S = \pm 15$ V.

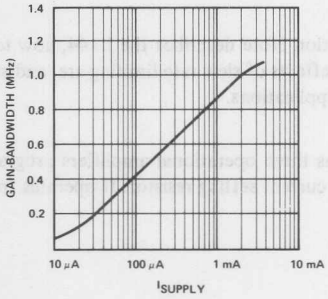


Input Bias Current vs Supply Current
Figure 3

variation of open loop gain with temperature is typically −2 dB per 100°C of temperature rise. The 600 kHz unity gain crossover gives a gain bandwidth product (GBWP) of 600,000. Figure 5 shows the variation of GBWP with supply current.



L144 Open Loop Gain vs Frequency
Figure 4

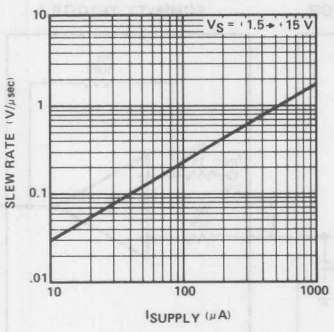


L144 Gain Bandwidth Product vs Supply Current
Figure 5

The vertical axis is linear whereas the horizontal I_{CC} axis is logarithmic, demonstrating that the GBWP does vary with I_{CC}, but at much less than the 1-to-1 ratio observed for other parameters.

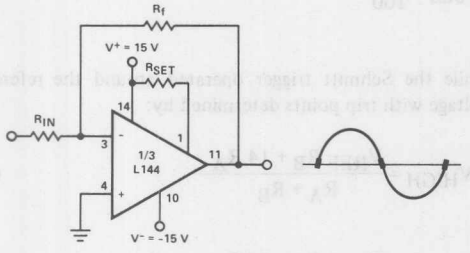
Slew Rate

Slew rate is almost a direct function of supply current as shown in Figure 6. This follows from the fact that slew rate limiting is actually caused by the finite limits of the internal current sources (which charge and discharge the second stage compensation capacitor) varying with the externally-determined set current. An amplifier output changes from the small signal response shown on the Bode plot to a slew-rate-limited response when the rate of change of the output voltage exceeds the rate of change determined by slew rate limit of the amplifier. Since the maximum rate of change of



Slew Rate Limits vs Supply Current
Figure 6

a sine wave is a function of peak amplitude it is possible to trade maximum frequency for peak signal amplitude when operating at low power dissipation levels. Figure 7 shows the derivation[1] of an equation relating slew rate S_r, sine wave amplitude V_{PEAK}, and frequency. The zero crossing of a sine wave is the point of maximum rate of change as shown after the derivative is taken and maximized. In both of the examples shown the maximum undistorted operating frequency is kept constant while juggling power dissipation, slew rate, and peak amplitude in an engineering tradeoff.



$$V_{OUT} = V_{peak} \sin 2\pi ft$$

$$\frac{dV_{OUT}}{dt} = V_{peak}\, 2\pi f \cos 2\pi ft$$

$$\left.\frac{dV_{OUT}}{dt}\right|_{t=0} = V_{peak}\, 2\pi f$$

$$S_r = \left.\frac{dV_{OUT}}{dt}\right|_{max} = V_{peak}\, 2\pi f_{max}$$

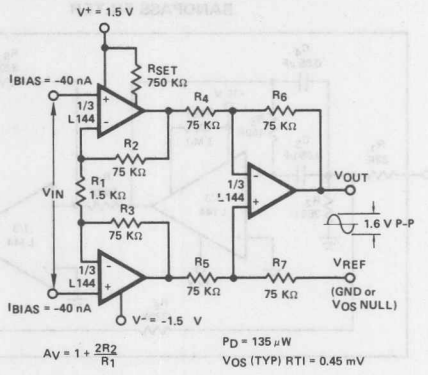
I_{SUPPLY} = 820 μA, S_r = 1.5 V/μsec
P_D = 24 mW, V_{peak} = 10 V
$f_{max} = \frac{S_r}{V_{peak}\, 2\pi}$ = 24 KHz

I_{SUPPLY} = 60 μA, S_r = 0.15 V/μsec
P_D = 1.8 mW, V_{peak} = 1 V
$f_{max} = \frac{S_r}{V_{peak}\, 2\pi}$ = 24 KHz

Slew Rate Limiting
Figure 7

Instrumentation Amplifier

Figure 8 shows a single L144 chip used to construct a three-amplifier classical instrumentation amplifier. The entire circuit consumes only 135 μW of power from a ±1.5 V power supply. With a gain of 101 the instrumentation amplifier is ideal in sensor interface and biomedical preamplifier applications.

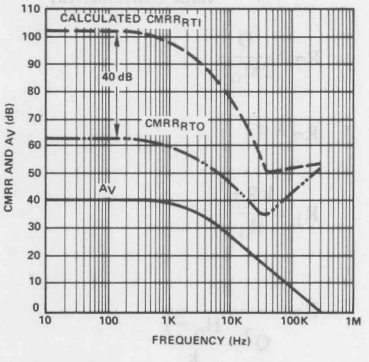


L144 Instrumentation Amplifier
Figure 8

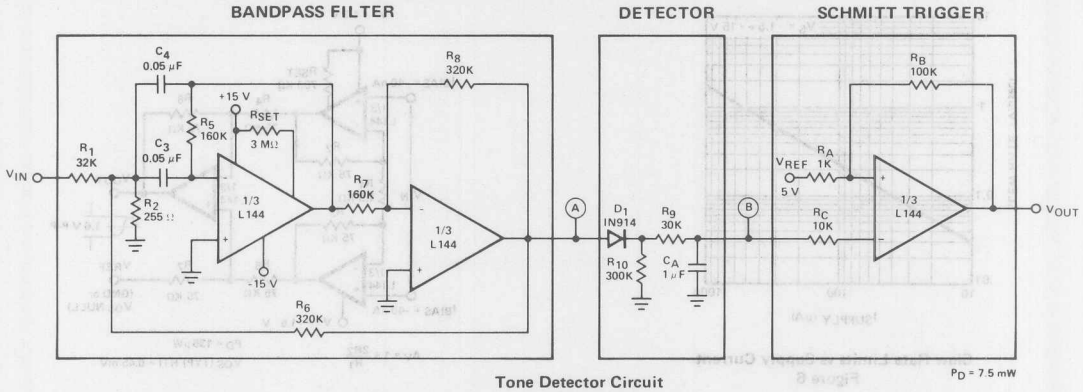
The first stage provides all of the gain while the second stage is used to provide common mode rejection and double-ended to single-ended conversion. The resistor R_1 determines the gain of the circuit according to the equation:

$$A_V = 1 + \frac{2R_2}{R_1} \qquad (1)$$

The reference point at the base of R_7 can be used to determine the quiescent output voltage when there is no differential input voltage. This provides an easy single point to zero any net offset voltage (typically 0.45 mV referred to input) and/or to insert a trim resistor to improve common mode rejection ratio (CMRR). The CMRR depends heavily on the match between R_4/R_6 and R_5/R_7 and can be nulled if R_7 is broken into a resistor and a small-value trim potentiometer. Figure 9 shows the voltage gain and CMRR versus frequency for a typical instrumentation amplifier. The upper curve shows a calculated CMRR referred to input. The falloff and final rise in CMRR is due to the mismatch in gain rolloff between amplifiers in the first stage followed by a falloff in gain and consequent increase in rejection of the second stage.



Common Mode Rejection Ratio and Gain vs Frequency
Figure 9



Tone Detector Circuit
Figure 10

Tone Detector

Another example of a single L144 providing the amplifiers for an entire system is shown in Figure 10. This tone detector circuit is made up of a two-amplifier multiple feedback bandpass filter followed by an AC-to-DC detector section and a Schmitt Trigger. The bandpass filter (with a Q of 25) passes only 500 Hz inputs which are in turn rectified by D_1 and filtered by R_9 and C_A. This filtering action in combination with the trigger level of 5 V for the Schmitt device insures that at least 55 cycles of 500 Hz input must be present before the output will react to a tone input. The actual integrating capacitor waveform shown in Figure 11 was taken with a 1 volt peak 500 Hz sine wave input. The ratio between capacitor C_A charge and discharge is 1:11, due to resistors R_9 and R_{10}.

For frequencies other than the 500 Hz center frequency shown in the example the relevant bandpass filter[2] equations are:

GIVEN: Q, f_o, H_o (Q normally from 10 to 50) (2)

LET: $C = C_3 = C_4$

$1 \leqslant k \leqslant 10$ (k chosen for component value convenience) (3)

THEN:

$$R_7 = \frac{Q}{2\pi f_o C} \quad (4)$$

$$R_7 = R_5 \quad (5)$$

$$R_1 = \frac{kR_7}{H_o} \quad (6)$$

$$R_2 = \frac{R_7}{Q^2 - \frac{H_o + 1}{k}} \quad (7)$$

$$R_8 = kR_7 = R_6 \quad (8)$$

In the example shown in Figure 10 the chosen value of k = 2 and the passive components used resulted in a measured Q of 23.1. The center frequency of 495.7 Hz and H_o of 9.9 were close to the calculated values of 500 Hz and 10.

The detector RC was designed to have a 3 dB down frequency of:

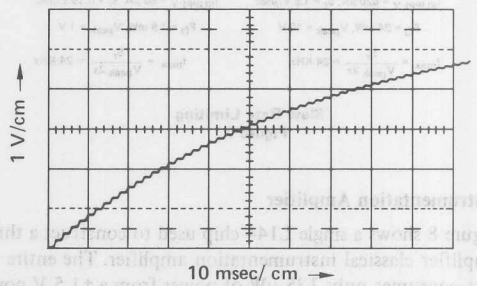
$$f_{3dB} = \frac{f_o}{100} \quad (9)$$

while the Schmitt trigger operated around the reference voltage with trip points determined by:

$$V_{HIGH} = \frac{V_{REF} R_B + 14 R_A}{R_A + R_B} \quad (10)$$

$$V_{LOW} = \frac{V_{REF} R_B - 14 R_A}{R_A + R_B} \quad (11)$$

where ±14 V is the output swing with ±15 V supplies. The measured trip points agreed with the calculated values of 5.089 V and 4.81 V within 0.2% in the circuit of Figure 10.



Detector Output Voltage vs Time
Figure 11

3 Amplifier Active Filter

The active filter shown in Figure 12 is a state variable filter with band-pass, high-pass and low-pass outputs. It is a classical analog computer method of implementing a filter using three amplifiers and only two capacitors. With the L144 triple op amp it becomes cost-effective to use this configuration with its attendant high Q values and low sensitivities.[3] The practical maximum value of Q is:

$$Q_{max} = \frac{A_{fo}}{3} \qquad (12)$$

where A_{fo} is the open loop gain of amplifier A_1 at the resonant frequency.

The controlling design equations are:

GIVEN: Q, f_o, and H_o (bandpass output) (13)

LET: $R_5 = R_6 = R_7$ (Chosen for component value convenience) (14)
$C_1 = C_2$

THEN: $$\frac{R_4}{R_3} = 3H_o - 1 \text{ for } H_o << \frac{A_{fo}}{3} \qquad (15)$$

$$R_2C_2 = \frac{H_o}{2\pi f_o Q} \qquad (16)$$

$$R_1C_1 = \frac{Q}{2\pi f_o H_o} \qquad (17)$$

The design example shown in Figure 12 was calculated as follows:

LET: $Q = 26$
$f_o = 1$ kHz
$H_o = 26$
$R_5 = R_6 = R_7 = 20$k (18)
$C_1 = C_2 = .008\ \mu$F
$R_3 = 10$k

THEN: $$R_4 = (3H_o - 1)\,R_3 = 770\text{k} \approx 750\text{k} \qquad (19)$$

$$R_2 = \frac{H_o}{2\pi f_o Q C_2} = 19.9\text{k} \approx 20\text{k} \qquad (20)$$

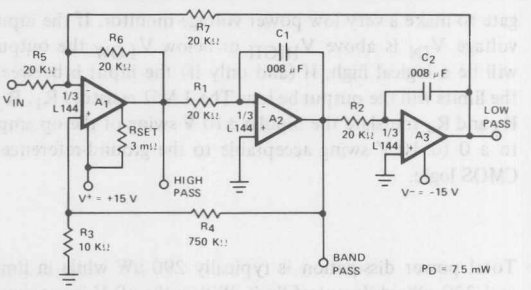
$$R_1 = \frac{Q}{2\pi f_o H_o C_1} = 19.9\text{k} \approx 20\text{k} \qquad (21)$$

giving an actual calculated f_o and H_o of

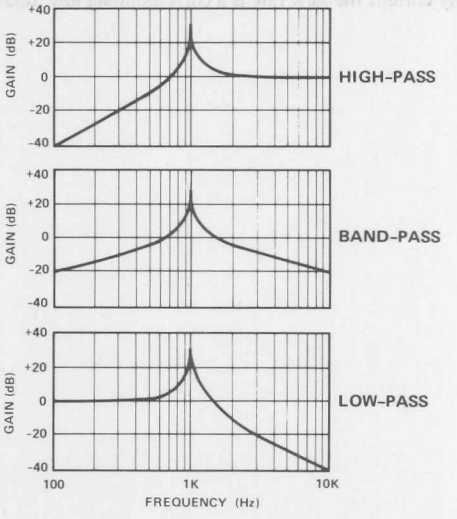
$$H_o = 1/3\,(1 + \frac{R_4}{R_3}) = 25.3 \qquad (22)$$

$$f_o = \frac{Q}{2\pi R_1 C_1 H_o} = \frac{H_o}{2\pi R_2 C_2 Q} = 994.7 \text{ Hz} \qquad (23)$$

The measured values of Q, H_o, and f_o using 1% components were 26.9, 26.3 and 996 respectively. Figure 13 shows the Bode plots of the high-pass, band-pass, and low pass outputs.



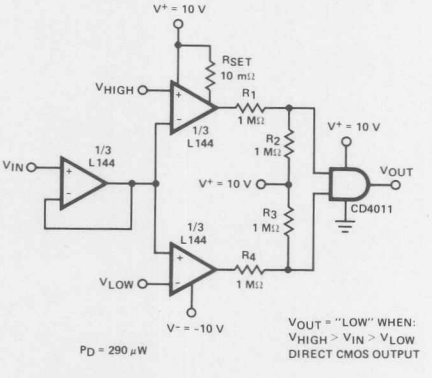
3 Amplifier Active Filter
Figure 12



Bode plots of Active Filter Output
Figure 13

Micropower Double-Ended Limit Detector

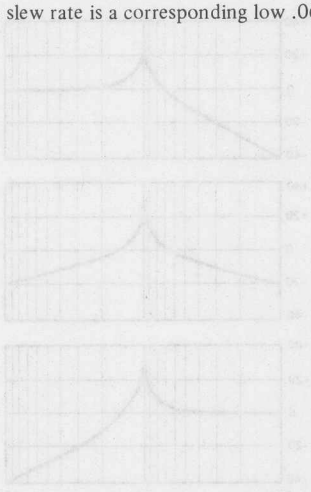
The double-ended limit detector shown in Figure 14 uses three sections of an L144 and a DC4011 type CMOS NAND

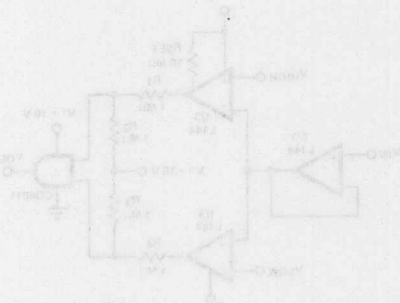


Micropower Double-Ended Limit Detector
Figure 14

R_3 and R_4 translate the bipolar ±10 V swing of the op amps to a 0 to 10 V swing acceptable to the ground-referenced CMOS logic.

Total power dissipation is typically 290 μW while in limit and 330 μW while out of limit. Within the ±9 V input range of the circuit the comparator resolution is typically 2 mV with the offset adjust determined by trimming V_{HIGH} and V_{LOW}. Since the L144 is operating at only 14.5 μA of supply current the slew rate is a corresponding low .063V/μsec.





REFERENCES

1. M.K. Vander Kooi, "Slew Rate Limiting of IC Op Amp is Easy to Predict and to Avoid," EDN, October, 1972; pp. 36-37.
2. J.G. Graema, G.E. Tobey, and L.P. Huelsman; "Operational Amplifiers Design and Application," McGraw-Hill Co., New York, N.Y., 1971, pp.293-295.
3. S.K. Mitra, "Active Inductorless Filters," IEEE Inc., New York, N.Y., 1971, pp. 74-78.

Micropower Quad

- **Voltage Comparators**
- **Window Comparators**
- **Level Detectors**
- **CMOS Line Receivers**
- **Oscillators**
- **Ramp Generators**
- **Phase Comparators**
- **Battery Powered Circuits**

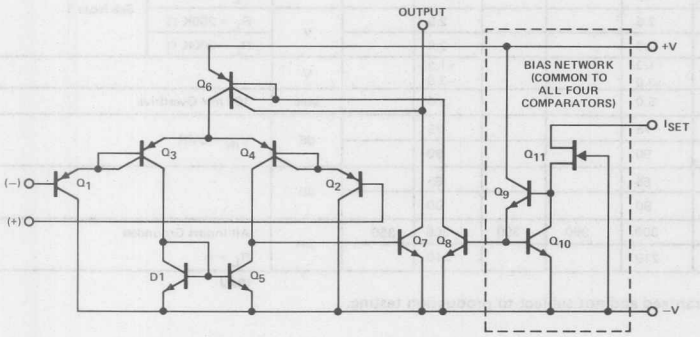
BENEFITS

- **Minimizes System Power Requirements**
 - Operates on 15 μW
- **Reduces External Component Requirements**
 - Programmable Output Drive Capability
 - Direct Wire-OR of Output
 - Input Sensing Near Ground
 - Direct CMOS Logic Compatibility
- **Easily Tailored to Your System**
 - Single Programming Resistor Simultaneously Alters Supply Current, Input Bias Current, Slew Rate and Power Consumption
- **Minimizes Number of Supply Voltages in Your System**
 - Operates with ±1.0 V to ±18 V
 - Single Supply Operation

DESCRIPTION

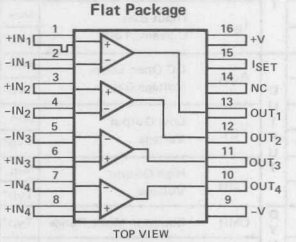
The L161 is a monolithic quad micropower comparator circuit, with an external control for varying supply current, input bias current and output current drive. This is accomplished by a single resistor connected to V^+ which controls the bias current to Q_{10} which, via a series of current mirrors, supplies bias to the differential amplifier. The L161 finds applications in areas where low powered battery operation and CMOS compatibility are required. The ability to control comparator characteristics makes this a very versatile device.

SCHEMATIC DIAGRAM (ONE COMPARATOR)



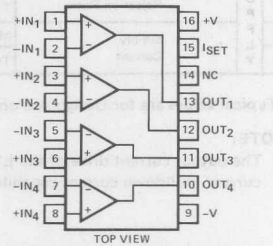
PIN CONFIGURATIONS

Flat Package



ORDER NUMBERS L161AL OR L161BL
SEE PACKAGE 17

Dual-In-Line Package



ORDER NUMBERS L161AP OR L161BP
SEE PACKAGE 12
ORDER NUMBER L161CJ
SEE PACKAGE 8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ±18 V
Differential Input Voltage ±30 V
Input Voltage* (A Suffix) ±18 V
(B Suffix) ±18 V
Output Short Circuit Duration** (Indefinite)
Operating Temperature (A Suffix) . . . −55 to +125°C
(B Suffix) . . . −20 to +85°C
(C Suffix) 0 to +70°C
Storage Temperature (A and B Suffix) . . −65 to +150°C
(C Suffix) −65 to +125°C
Power Dissipation***
Flat Package 750 mW
16 Pin DIP (Side Braze) 900 mW
16 Pin Plastic DIP 470 mW

*For supply voltages < ±18 V, maximum input voltage is equal to supply voltage

**Continuous short circuit current is allowed for case temperature to +125°C and ambient temperature to +70°C

***All leads welded or soldered to PC board. Derate 10 mW/°C above 75°C for the flat package, 12 mW/°C above 75°C for the sidebraze DIP and 6.3 mW/°C above 25°C for the plastic DIP.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

Low Power Characteristics

			Characteristics		L161A −55°C	L161A 25°C	L161A +125°C	L161B/C −20°C/0°C	L161B/C 25°C	L161B/C +85°C/70°C	Unit	Test Conditions, Unless Otherwise Noted: V_S = ±3 V, I_{SET} = 10 µA, R_L = 10M Ω, C_L = 10 pF
1	INPUT	V_{OS}	Input Offset Voltage	Max	5.0	3.0	5.0		6.0		mV	
2				Typ*		1.0			1.0			
3		I_{OS}	Input Offset Current	Max		20			25		nA	
4				Typ*		1.0			1.0			
5		I_{BT}	Input Bias Current, Total	Max		100			200		nA	
6				Typ*		20			20			
7	OUTPUT	A_{VOL}	DC Open Loop Voltage Gain	Min	10	20	20	5	10	10	V/mV	
8				Typ*	25	30	35	25	30	35		
9		V_{OL}	Low Output Voltage	Min		−2.6			−2.6		V	R_L = 20K Ω; See Note 1
10				Typ*		−2.95			−2.95			R_L = 20K Ω
11		V_{OH}	High Output Voltage	Min		2.5			2.5		V	R_L = 200K Ω
12				Typ*		2.9			2.9			R_L = 200K Ω
13	DYNAMIC	CMR	Common Mode Range	Typ*		+1.3/−3.0			+1.3/−3.0		V	
14		t_r	Response Time	Typ*		5.0			5.0		µsec	100 mV Overdrive
15		CMRR	Common Mode Rejection Ratio	Min		75			75		dB	V_{IN} = CMR
16				Typ*		90			90			
17	SUPPLY	PSRR	Power Supply Rejection Ratio	Min		65			65		dB	
18				Typ*		80			80			
19		I_S	Supply Current	Max	300	300	350	300	300	350	µA	All Inputs Grounded
20				Typ*		210			210			R_L = ∞

IBAJ

*Typical values are for Design Aid only, not guaranteed and not subject to production testing.

NOTE:

1. The output current drive of the L161 is non-symmetrical. This facilitates the wire-ORing of two comparator outputs. The output pulldown current pulldown current capability is typically 75—150 times the pullup current.

ELECTRICAL CHARACTERISTICS (Cont'd)

High Power Characteristics

		Characteristics			L161A			L161B/C			Unit	Test Conditions, Unless Otherwise Noted: $V_S = \pm 15$ V, $I_{SET} = 100\ \mu A$, $R_L = 2M\ \Omega$, $C_L = 10$ pF
					−55°C	25°C	+125°C	0°C/ −20°C	25°C	70°C/ +85°C		
1	INPUT	V_{OS}	Input Offset Voltage	Max	6.0	3.0	6.0		6.0		mV	
2				Typ*		1.5			1.5			
3		I_{OS}	Input Offset Current	Max		60			90		nA	
4				Typ*		5.0			5.0			
5		I_{BT}	Input Bias Current, Total	Max		400	500		800		nA	
6				Typ*		100			100			
7	OUTPUT	A_V	Voltage Gain	Min	25.0	50	50	15	30	30	V/mV	
8				Typ*	75.0	100	100	75	100	100		
9		V_{OL}	Low Output Voltage	Min		−14.6			−14.6		V	$R_L = 20K\ \Omega$
10				Typ*		−14.9			−14.9			$R_L = 20K\ \Omega$
11		V_{OH}	High Output Voltage	Min		14.5			14.5		V	$R_L = 200K\ \Omega$
12				Typ*		14.9			14.9			$R_L = 200K\ \Omega$
13	DYNAMIC	CMR	Common Mode Range	Typ*		+13/ −15.0			+13/ −15.0		V	
14		t_r	Response Time	Typ*		1.0			1.0		μsec	100 mV Overdrive, $C_L = 10$ pF
15		CMRR	Common Mode Rejection Ratio	Min		75			75		dB	V_{IN} = CMR
16				Typ*		90			90			
17	SUPPLY	PSRR	Power Supply Rejection Ratio	Min		65			65		dB	
18				Typ*		80			80			
19		I_S	Supply Current	Max	4000	3500	3750	4000	3500	3750	μA	All Inputs Grounded
20				Typ*		2100			2100			$R_L = \infty$

See Note 1

IBAJ

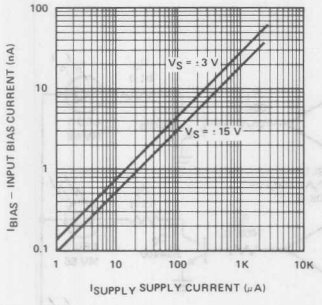
*Typical values are for Design Aid only, not guaranteed and not subject to production testing.

NOTE:

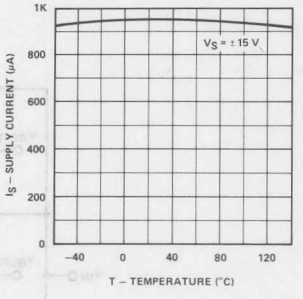
1. Set current (I_{SET}) and supply current (I_{SUPPLY}) can be determined by the following formulas: $I_{SET} = \frac{[(+V) - (2V_{BE}) - (-V)]}{R_{SET}}$; $I_{SUPPLY} \simeq 21 \times I_{SET}$.

TYPICAL CHARACTERISTICS ($T_A = 25°C$, $V_{SUPPLY} = \pm 15$ V unless otherwise noted)

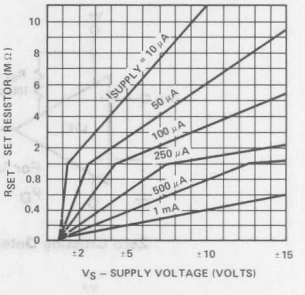
Input Bias Current vs Supply Current



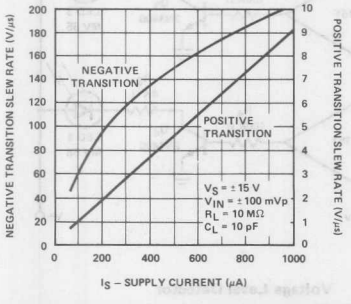
Supply Current vs Temperature



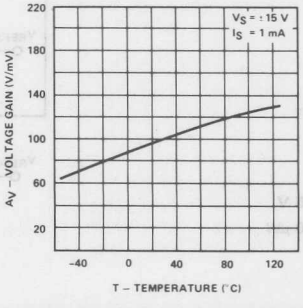
R_{SET} vs V_{SUPPLY} for Various $I_{SUPPLIES}$



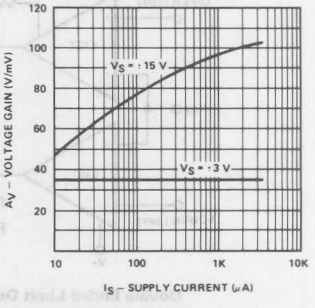
Slew Rate vs Supply Current



Voltage Gain vs Temperature

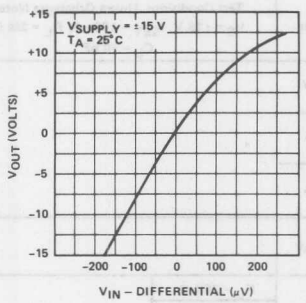


Voltage Gain vs Supply Current

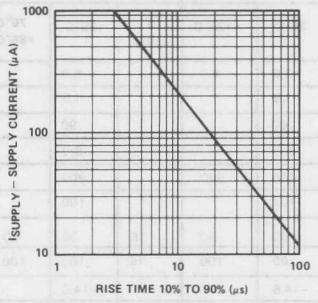


TYPICAL CHARACTERISTICS (Cont'd) (T_A = 25°C, V_{SUPPLY} = ±15 V unless otherwise noted)

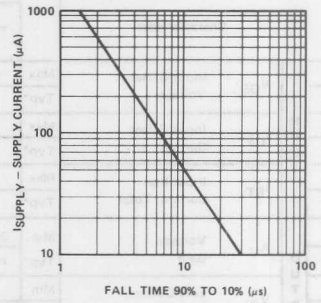
Transfer Characteristic



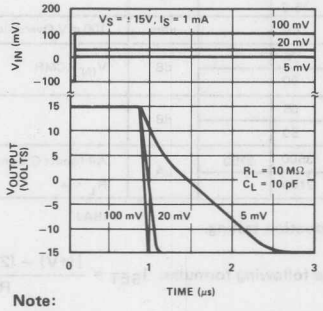
Rise Time vs Supply Current with One CMOS Load



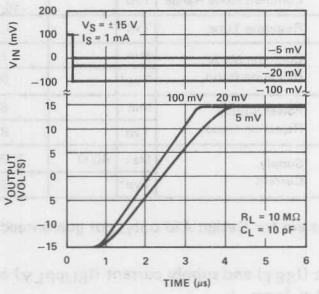
Fall Time vs Supply Current with One CMOS Load



Response Time vs Input Overdrive Negative Transition



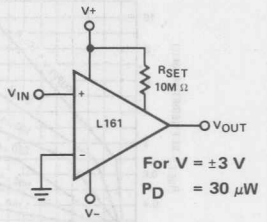
Response Time vs Input Overdrive Positive Transition



Note:

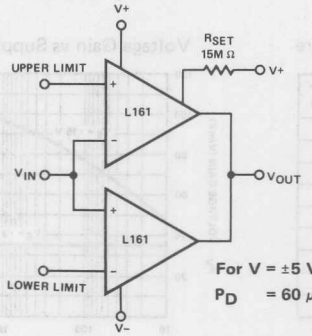
The output current drive of each comparator in the L161 is non-symmetrical. The pull-up current is typically 2 [V+ – 1 – (V–)/R_{SET}] and the pull-down current capability is typically from 75 to 150 times the pull-up current.

APPLICATIONS



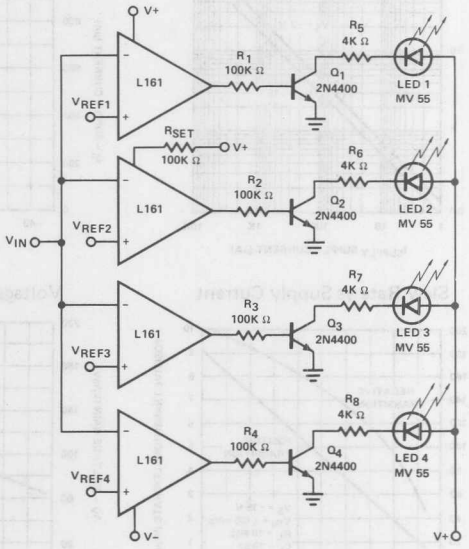
For V = ±3 V
P_D = 30 μW

Zero Crossing Detector



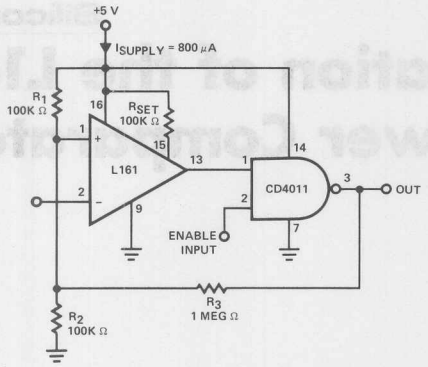
For V = ±5 V
P_D = 60 μW

Double Ended Limit Detector

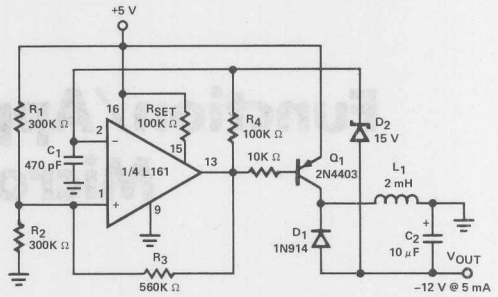


Voltage Level Detector

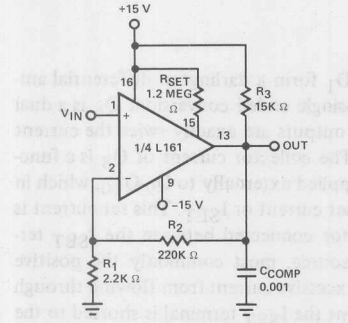
APPLICATIONS (Cont'd)



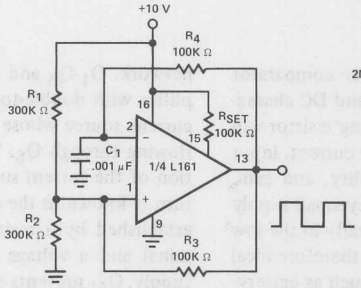
CMOS Line Receiver



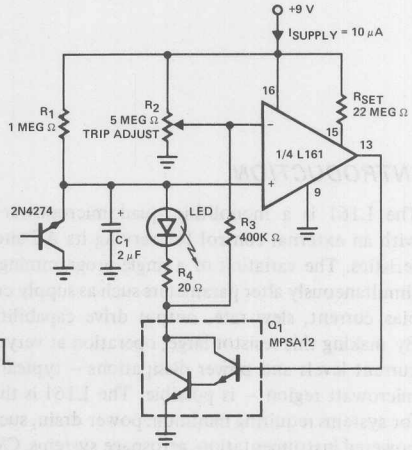
A Regulated DC to DC Converter



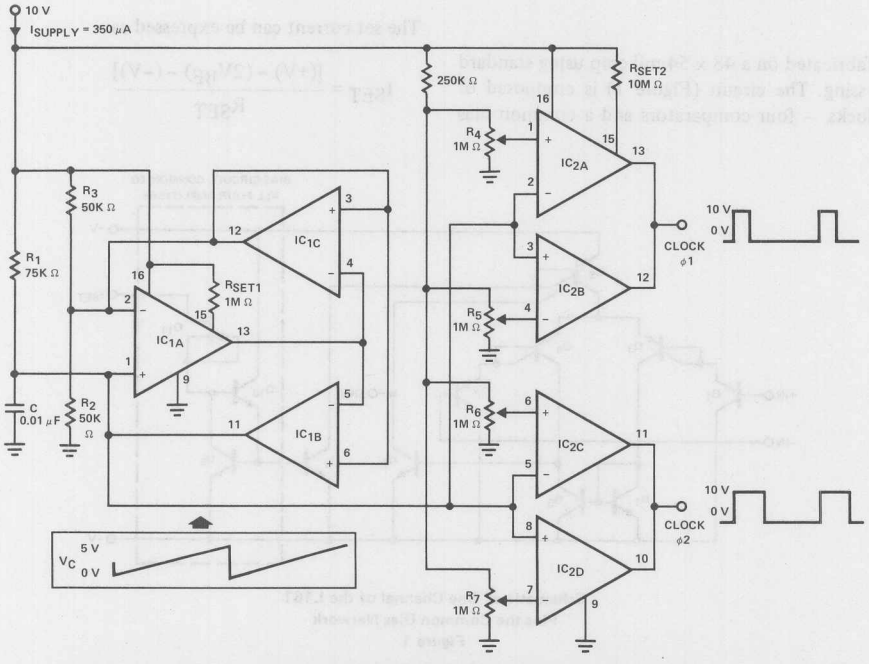
The L161 as an X100 Operational Amplifier



Squarewave Oscillator



A Low Battery Indicator



A Versatile 2ϕ Pulse Generator

Siliconix

Function/Application of the L161 Micropower Comparator

INTRODUCTION

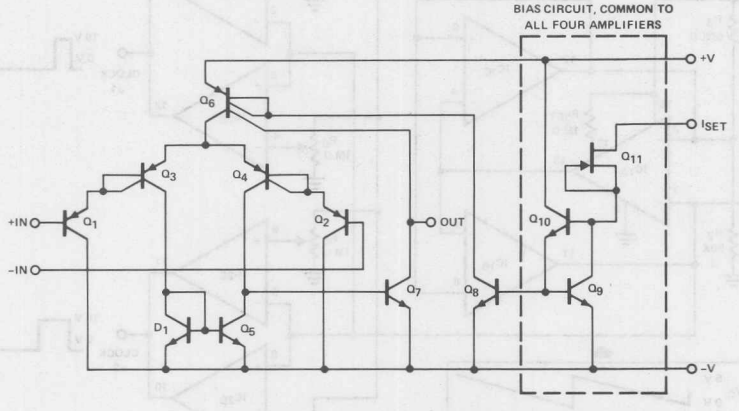
The L161 is a monolithic quad micropower comparator with an external control for varying its AC and DC characteristics. The variation of a single programming resistor will simultaneously alter parameters such as supply current, input bias current, slew rate, output drive capability, and gain. By making this resistor large, operation at very small supply current levels and power dissipations – typically in the low microwatt region – is possible. The L161 is therefore ideal for systems requiring minimum power drain, such as battery-powered instrumentation, aerospace systems, CMOS designs, and remote security systems.

Description

The L161 is fabricated on a 48 x 54 mil chip using standard bipolar processing. The circuit (Figure 1) is composed of five major blocks – four comparators and a common bias network. Q_1-Q_6 and D_1 form a darlington differential amplifier with double-to-single ended conversion. Q_6 is a dual current source whose outputs are exactly twice the current flowing through Q_8. The collector current of Q_8 is a function of the current supplied externally to Q_9-Q_{10}, which in turn is known as the set current or I_{SET}. This set current is established by a resistor connected between the I_{SET} terminal and a voltage source, most commonly the positive supply. Q_{11} prevents excessive current from flowing through Q_9 and Q_{10} in the event the I_{SET} terminal is shorted to the positive supply; it has no effect on circuit operation under normal conditions.

The set current can be expressed as:

$$I_{SET} = \frac{[(+V) - (2V_{BE}) - (-V)]}{R_{SET}} \quad (1)$$



Schematic of One Channel of the L161 Plus the Common Bias Network
Figure 1

where +V is the voltage to which the control resistor is connected, −V is the negative supply voltage, V_{BE} is the base emitter drop of Q_9 or Q_{10} (about 0.7 V), and R_{SET} is the value of the external control resistor or set resistor. Equation 1 is simply a derivative of ohms law. There is also an analytical relationship between I_{SET} and the total supply current:

$$
\begin{aligned}
I_{SUPPLY} = & \left[I_{SET} \text{ (current sourced by } Q_6 \text{ to } Q_8)\right. \\
& + 2\, I_{SET} \text{ (current sourced to the differential amplifier by } Q_6) \\
& \left. + 2\, I_{SET} \text{ (current sourced to the comparator output by } Q_6\right] \\
& \times 4 \text{ (the total numbers of comparators)} \\
& + I_{SET} \text{ (current sourced through } Q_{11}, Q_{10}, \text{ and } Q_9 \text{ to } -V) \\
= & \left[I_{SET} + 2\, I_{SET} + 2\, I_{SET}\right] \times 4 + I_{SET} \\
= & \ 21\, I_{SET}
\end{aligned}
$$

The output current pulldown capability (I_{OL}) of the L161 is about 2 orders of magnitude greater than the high output drive current, (I_{OH}), which allows wire-ORing the outputs. I_{OH} is simply the current sourced by Q_6:

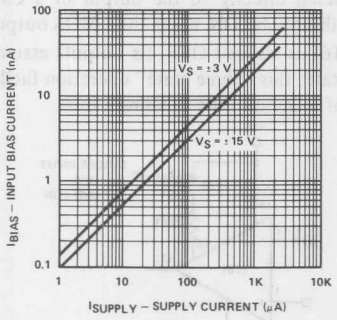
$$I_{OH} = 2 \times I_{SET} \qquad (3)$$

I_{OL} is found by multiplying the current sourced by the collector of Q_6 by the gain of Q_7:

$$I_{OL} = \beta(Q7) \times 2\, I_{SET} \qquad (4)$$

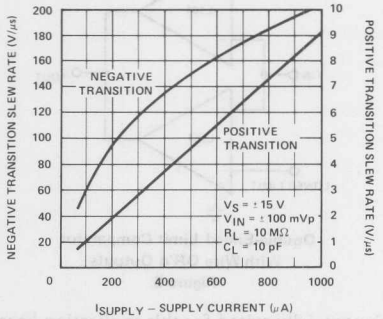
The beta of Q_7 is about 75-150.

Input bias current is a function of the betas of input devices Q_1-Q_2 and I_{SET}. This is difficult to express analytically because β varies greatly with both processing and collector current; however it is roughly proportional to the set current and can easily be determined experimentally (see Figure 2).

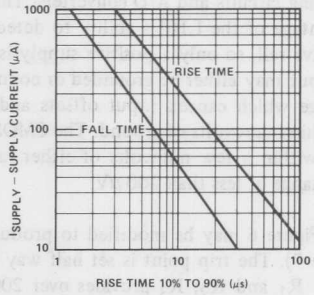


Input Bias Current vs Supply Current
Figure 2

Gain varies logarithmically with changes in supply voltage and linearly with changes in set current. Primary causes are the decrease in output impedance of Q_7 with decreasing supply voltage and an increase in transistor betas with increasing set current. Other AC parameters such as slew rate and transition time are also effected by set current; however current dependent parameters such as beta and chip capacitances make mathematical expressions imprecise. These relationships have been determined emperically and are presented in Figures 3 and 4.



Slew Rate vs Supply Current
Figure 3

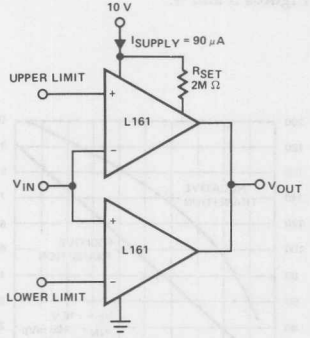


Rise and Fall Times vs Supply Current
With One CMOS Load
Figure 4

The designer's ability to program the key parameters of the L161 enables him to program just enough supply current to meet his design objectives. This coupled with the L161's performance using only microwatts of power makes it ideal for any micropower or battery-powered system, as well as a replacement for existing higher power comparators. The following applications illustrate the flexibility and unique capabilities of the L161.

Micropower Applications

limit may be as low as –0.4 V with the V– terminal at ground. A comparison about ground is therefore possible with only one supply.

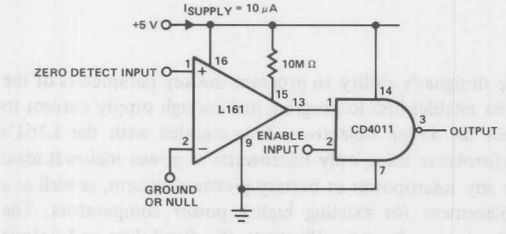


Double-Ended Limit Comparator With Wire OR'd Outputs
Figure 5

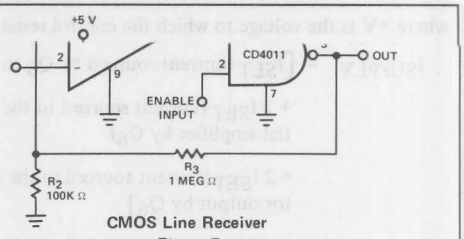
The L161 is especially suited for this application because of its wire OR capability; low output on either comparator will pull both outputs to ground. For this example a supply current of 90 μA was chosen to provide a slew rate of about 5 V/μs. If greater output drive current or decreased transition times are needed, lower R_{SET}.

The zero crossing detector shown in Figure 6 is useful in sine wave squaring circuits and A/D converters. This circuit also takes advantage of the L161's ability to detect signals below its negative rail, so only a positive supply is needed. The positive input may either be grounded or connected to a nulling voltage which cancels input offsets and enables accuracy to within microvolts of ground. The CMOS output will switch to within a few millivolts of either rail for an input voltage change of less than 200 μV.

The circuit in Figure 6 may be modified to produce a line receiver (Figure 7). The trip point is set half way between the supplies by R_1 and R_2; R_3 provides over 200 mV of hysteresis to increase noise immunity. With 800 μA of quiescent supply current the maximum frequency of operation is about 300 kHz. If response to TTL levels is desired, change R_2 to 39K. The trip point is now centered at 1.4 V.

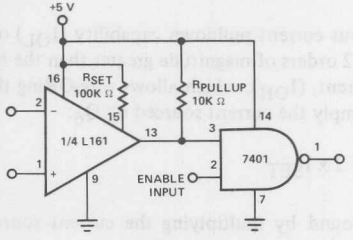


Zero Crossing Detector
Figure 6



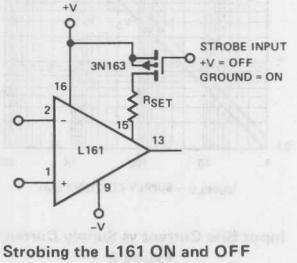
CMOS Line Receiver
Figure 7

Mating the L161 with CMOS logic is natural since the L161 draws microamps from a single 5 V supply. However, the L161 will also drive TTL when a suitable pull-up resistor is provided. Figure 8 shows this combination. Total power drain of the circuit is much heavier due to the presence of the 7402. Propagation delays through the circuit are about 1 μsec.



Driving TTL
Figure 8

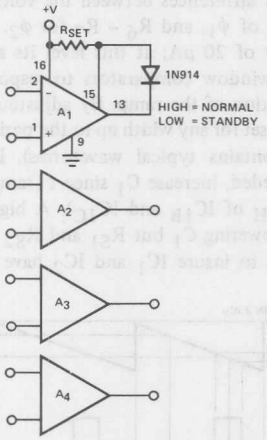
In many situations further power savings can be achieved by reducing or eliminating I_{SET} during part of the operating time. This is desirable. for example, when a system is multiplexed at a low duty cycle. The L161 may be strobed off completely by reducing I_{SET} to zero as shown in Figure 9. The 3N163 P-channel MOSFET is OFF when the strobe input is high so no set current flows into the L161. For a low strobe input, the 3N163 turns ON, pulling R_{SET} to the positive supply and turning on the comparator. The drain-source resistance of the 3N163 (3000 Ω) is negligible compared to R_{SET}. If the negative supply terminal of the L161 is returned to ground, the 3N163 may be eliminated and R_{SET} connected directly to the output of a CMOS gate. The L161 will now be ON when the CMOS output is high. When the L161 is strobed OFF, its outputs assume a high-impedance state; this "three state" operation facilitates the connection of many outputs to a single bus.



Strobing the L161 ON and OFF
Figure 9

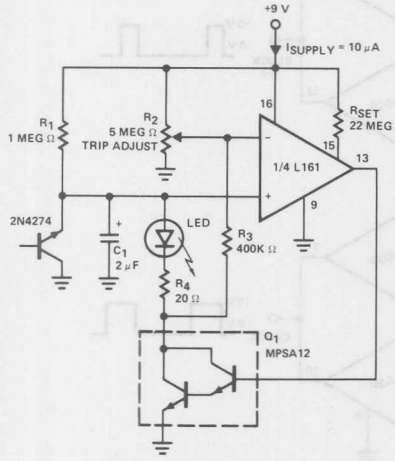
The L161 will switch itself into a standby mode if one of its outputs is connected to the I_{SET} terminal as illustrated in Figure 10. The diode blocks current when the output of A_1 is HIGH, and operation of the other three comparators is normal. When the output goes low, however, the 1N914 conducts most of I_{SET} to the negative supply. I_{OL} is therefore nearly equal to I_{RSET}, and (from Equations 2 and 4),

$$I_{SUPPLY} = 21\, I_{SET(actual)} = \frac{21\, I_{OL}}{2B} = \frac{I_{RSET}}{10} \qquad (5)$$



Switching the L161 to a Low Current "Standby" Mode
Figure 10

if a β of 105 is assumed. Equation 5 states that the supply current of the L161 is reduced from 21 x I_{R1} (normal operation) to $I_{R1}/10$, a factor of 210 (or twice whatever β of Q_7 is). Total supply drain is simply the current through R_{SET}. This circuit has an important advantage over the previous strobe circuit – even though the L161 is operating at a greatly reduced supply current, it is still ON and continues to function. If a lesser reduction in supply current is desired, connect a resistor in series with the diode.

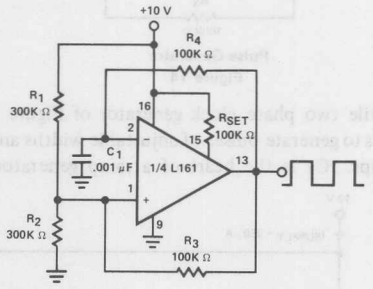


A Low Battery Indicator
Figure 11

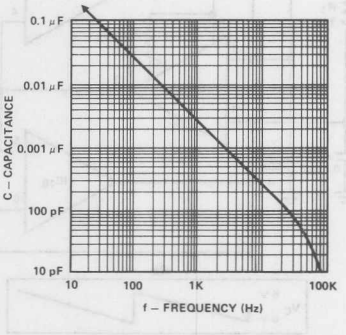
Figure 11 shows an L161 low battery indicator which flashes an LED when the battery voltage drops below a certain threshold. The 2N4274 emitter-base junction serves as a zener which establishes about 6 V on the L161's positive input. As the battery dies, the voltage at the negative input drops more quickly; when the low battery threshold (typically 7.5 V) is reached, the L161 output goes HIGH. This turns on the Darlington, which discharges C_1 through the LED. The interval between flashes is roughly equal to R_1C_1, which in this case is 2 seconds. By flashing the LED at a very low duty cycle, this circuit gives a low battery warning with only 10 μA average power drain.

Waveform Generators

Figure 12 is a square wave generator which is operable to over 100 kHz while Figure 13 depicts the typical frequency vs capacitance performance of the circuit. The low frequency limit is determined only by the size of C_1. Frequency is constant for supply voltages down to +5 V; below that the charging rate of C_1 in the positive direction is determined by I_{OH} and not R_4. For lower voltage operation, increase R_4 (and lower C accordingly) or decrease R_{SET}.



Squarewave Oscillator
Figure 12

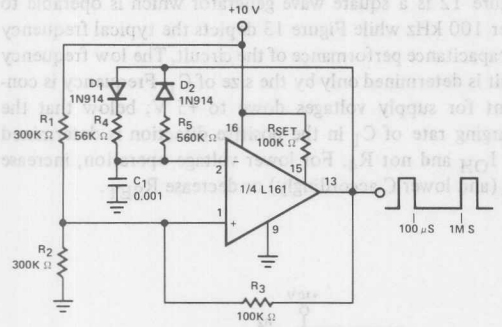


Frequency vs the Value of C_1 for the Squarewave Oscillator
Figure 13

To generate pulses the positive and negative charging rates of the capacitor must be unequal. Figure 14 illustrates a method using diodes and unequal resistors. The duty cycle of the output pulse is equal to $R_4/(R_4 + R_5)$ x 100%. For duty cycles of less than 50%, D_1 can be eliminated and R_2 raised according to the formula,

$$R_{4(actual)} = \frac{R_5 \times R_{4(eff)}}{R_5 - R_{4(eff)}} \quad (6)$$

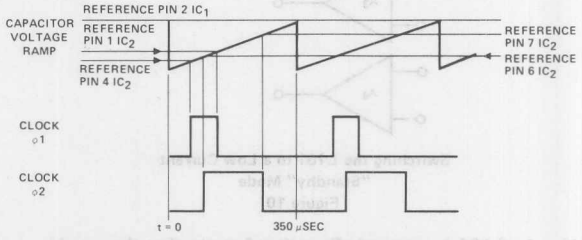
where $R_{4(eff)}$ is the effective value of R_2 in the circuit and $R_{4(actual)}$ is the actual value used; $R_{4(actual)}$ will always be larger than $R_{4(eff)}$. A similar analysis could be made for eliminating D_2 when t > 50%. Figure 13 may be used to determine frequency (= 1/period) if $1/2\,(R_4 + R_5) = 100K$.



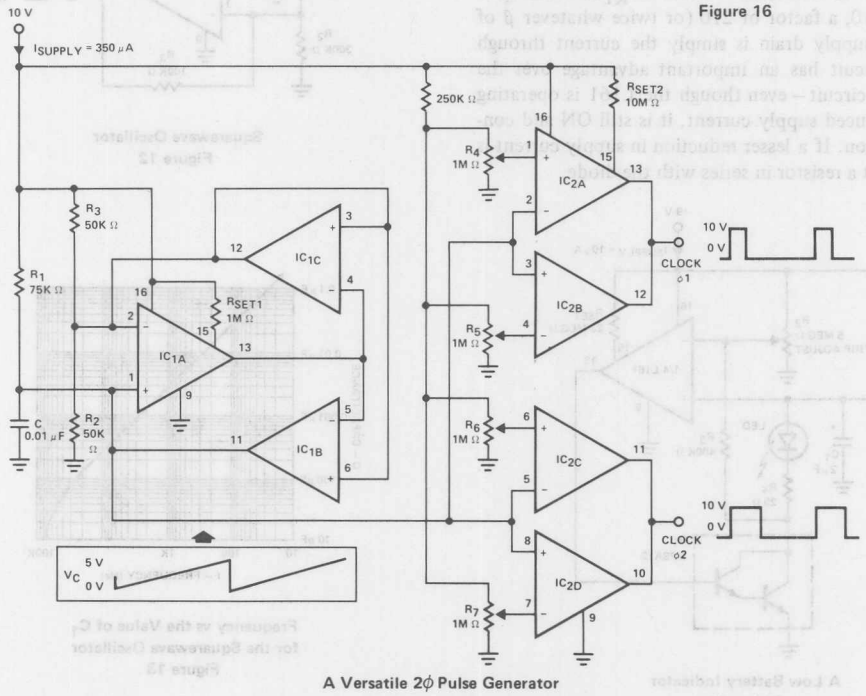
Pulse Generator
Figure 14

The versatile two phase clock generator of Figure 15 uses two L161's to generate pulses of adjustable widths and phase relationships. IC_1 is the heart of a ramp generator which feeds two variable window comparators formed by $IC_{2A} - IC_{2B}$ and $IC_{2C} - IC_{2D}$ respectively. The voltage on pin 1 of IC_{1A} ramps up as C_1 charges through R_1. When this voltage exceeds approximately 5 V (the potential on pin 2 of IC_{1A}), the output of IC_{1A} goes HIGH, forcing IC_{1B} and IC_{1C} LOW. C_1 is quickly discharged by I_{OL} of IC_{1B}, and the comparators reset to their normal state (IC_{1A} LOW, IC_{1B} and IC_{1C} HIGH).

As the ramp rises, its value passes through the two windows defined by the differences between the voltages on R_4 and R_5 in the case of ϕ_1, and $R_6 - R_7$ for ϕ_2. IC_2 is set for a supply current of 20 μA; at this level its slew rate is too slow for the window comparators to respond to the fast negative transition of the ramp. By adjusting $R_4 - R_6$, ϕ_1, and ϕ_2 may be set for any width up to the period of the ramp (Figure 16 contains typical waveforms). If longer pulse lengths are needed, increase C_1 since t (ramp) = 0.7 R_1C_1 (neglecting I_{OH} of IC_{1B} and IC_{1C}). A higher rep rate is obtained by lowering C_1 but R_{S1} and R_{S2} may also need to be lowered to insure IC_1 and IC_2 have adequate slew rates.

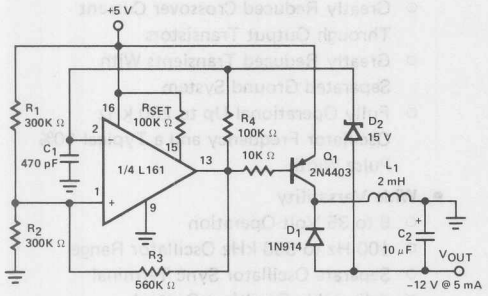


Typical Waveforms of the Two Phase Pulse Generator
Figure 16



A Versatile 2ϕ Pulse Generator
Figure 15

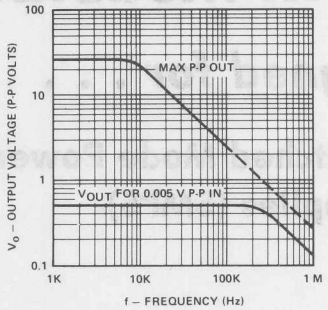
Figure 17 is a low power D.C. to D.C. converter obtained by adding a flyback circuit to the square wave oscillator. Operating frequency is 20 kHz to minimize the size of L_1 and C_2. Regulation is achieved by zener diode D_2; when the output is less than −12 V, the zener breaks down and discharges C_1 slightly which reduces the duty cycle of the oscillator below 50%. Maximum current available before the converter drops out of regulation is 5.5 mA at an overall efficiency of 71%. With no load the converter draws 590 μA.



A Regulated DC to DC Converter
Figure 17

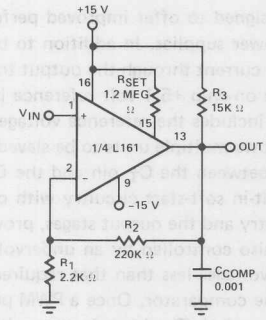
Operational Amplifiers

While designed primarily as a comparator, the L161 will perform as an op amp if proper compensation is applied. Figure 18 is a simple gain of 100 amplifier with a gain-bandwidth product of 20 MHz! The primary limitation in the performance is the low slew rate (0.3 V/μsec) imposed by I_{OH} charging C_{comp}. The effects of slew rate and compensation are shown in Figure 19. A lower gain amplifier

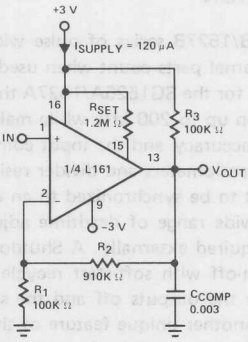


Frequency Response and Maximum Output for the X100 Op Amp
Figure 19

requires a larger C_{comp}, which in turn further reduces slew rate. For this reason it may actually be advantageous in certain cases to lower the gain by placing a resistive divider at the input rather than raising R_1. Figure 20 shows a 700 μwatt X10 op amp whose slew rate is 0.02 V/μsec and is 3 dB down at 100 kHz.



The L161 as a X100 Operational Amplifier
Figure 18



A Micropower X10 Op Amp
Figure 20

designed for . . .

■ Switched Mode Power Supplies (SMPS)

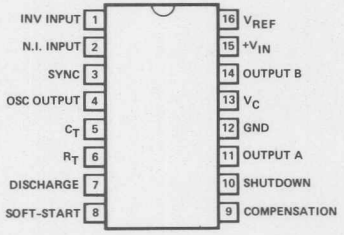
- **Direct Pin for Pin Replacement for SG1525A/1527A**
- **Improved Performance Over SG1525A/1527A**
 - Greatly Reduced Crossover Current Through Output Transistors
 - Greatly Reduced Transients With Separated Ground System
 - Fully Operational Up to 200 kHz Oscillator Frequency and a Typical 10% Pulse Width
- **Wide Versatility**
 - 8 to 35 Volt Operation
 - 100 Hz to 500 kHz Oscillator Range
 - Separate Oscillator Sync Terminal
 - Adjustable Deadtime Control
 - Internal Soft-Start
 - Input Undervoltage Lockout
 - Latching PWM to Prevent Multiple Pulses
- **Lower Overall Parts Count**
 - 5.1 Volt Onboard Reference Trimmed to ±1%
 - Dual 100 mA Source/Sink Output Drivers

DESCRIPTION

The Si1525B/1527B series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used to implement all types of switching power supplies. In addition to being a direct replacement for the SG1525A/1527A the Si1525B/1527B features low crossover current through the output transistors and full operation up to 200 kHz while maintaining a typical 10% pulse width. The on-chip +5.1 volt reference is trimmed to ±1% initial accuracy and the input common-mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and divider resistors. A Sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external system clock. A single resistor between the C_T pin and the Discharge pin provides a wide range of deadtime adjustment. These devices also feature built-in soft-start circuitry with only a timing capacitor required externally. A Shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn-off with soft-start recycle for slow turn-on. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for input voltages less than that required for normal operation. Another unique feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking 100 mA. The Si1525B output stage features NOR logic, giving a LOW output for an OFF state. The Si1527B utilizes OR logic which results in a HIGH output level when OFF.

PIN CONFIGURATION

Dual-In-Line Package



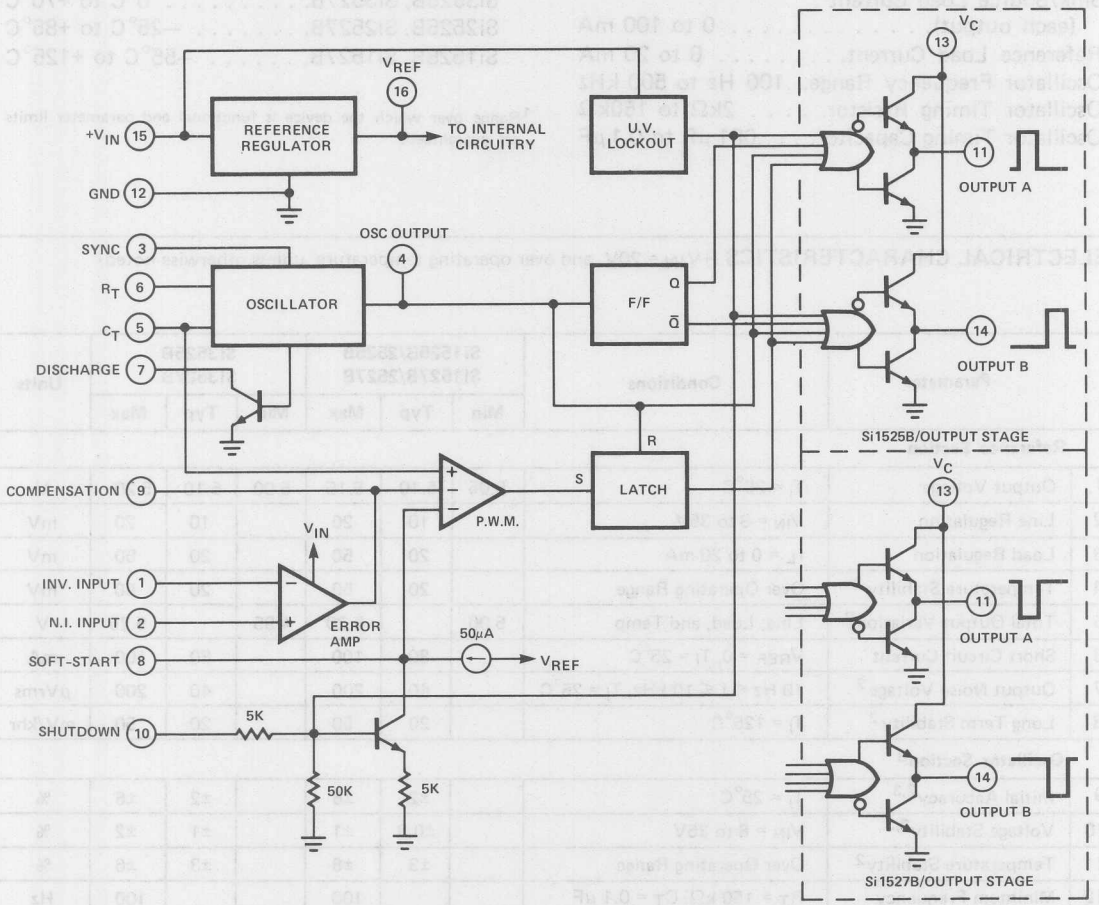
Top View

ORDER NUMBERS:

Si1525BK	Si1527BK
Si2525BK	Si2527BK
Si3525BK	Si3527BK

See Package 10

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS* (T_A = 25°C unless noted otherwise)

Supply Voltage ($+V_{IN}$) +40V
Collector Supply Voltage (V_C) +40V
Logic Inputs -0.3V to +5.5V
Analog Inputs -0.3V to $+V_{IN}$
Output Current, Source or Sink 200 mA
Reference Output Current 50 mA
Oscillator Charging Current 5 mA
Power Dissipation at T_A = +25°C** 1000 mW
Thermal Resistance: junction to ambient 100°C/W

Power Dissipation at T_C = +25°C*** 2000 mW
Thermal Resistance: junction to case 60°C/W
Operating Junction Temperature +150°C
Storage Temperature Range -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) +300°C

*Values beyond which damage may occur.
**Derate at 10 mW/°C for ambient temperatures above +50°C.
***Derate at 16 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS [1]

Input Voltage ($+V_{IN}$). +8V to +35V
Collector Supply Voltage (V_C). . . +4.5V to +35V
Sink/Source Load Current
(each output). 0 to 100 mA
Reference Load Current. 0 to 20 mA
Oscillator Frequency Range. .100 Hz to 500 kHz
Oscillator Timing Resistor. 2kΩ to 150kΩ
Oscillator Timing Capacitor. . . .001 μF to 0.1 μF
Deadtime Resistor Range. 0 to 500Ω
Operating Ambient Temperature Range
Si3525B, Si3527B. 0°C to +70°C
Si2525B, Si2527B. −25°C to +85°C
Si1525B, Si1527B. −55°C to +125°C

[1] Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL CHARACTERISTICS ($+V_{IN}$ = 20V, and over operating temperature, unless otherwise noted)

	Parameter	Conditions	SI1525B/2525B SI1527B/2527B			SI3525B SI3527B			Units
			Min	Typ	Max	Min	Typ	Max	
	Reference Section								
1	Output Voltage	T_j = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	V
2	Line Regulation	V_{IN} = 8 to 35V		10	20		10	20	mV
3	Load Regulation	I_L = 0 to 20 mA		20	50		20	50	mV
4	Temperature Stability [2]	Over Operating Range		20	50		20	50	mV
5	Total Output Variation [2]	Line, Load, and Temp	5.00		5.20	4.95		5.25	V
6	Short Circuit Current	V_{REF} = 0, T_j = 25°C		80	100		80	100	mA
7	Output Noise Voltage [2]	10 Hz ≤ f ≤ 10 kHz, T_j = 25°C		40	200		40	200	μVrms
8	Long Term Stability [2]	T_j = 125°C		20	50		20	50	mV/khr
	Oscillator Section [3]								
9	Initial Accuracy [2,3]	T_j = 25°C		±2	±6		±2	±6	%
10	Voltage Stability [2,3]	V_{IN} = 8 to 35V		±0.3	±1		±1	±2	%
11	Temperature Stability [2]	Over Operating Range		±3	±6		±3	±6	%
12	Minimum Frequency	R_T = 150 kΩ, C_T = 0.1 μF			100			100	Hz
13	Maximum Frequency	R_T = 2 kΩ, C_T = 1 nF	400			400			kHz
14	Current Mirror	I_{RT} = 2 mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
15	Clock Amplitude [2,3]		3.0	3.5		3.0	3.5		V
16	Clock Width [2,3]	T_j = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	μsec
17	Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
18	Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA

[2] These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
[3] Tested at f_{OSC} = 40 kHz (R_T = 3.6 kΩ, C_T = .01 μF, R_D = 0Ω).

CMCD

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ELECTRICAL CHARACTERISTICS (CONT)

	Parameter	Conditions	Si1525B/2525B Si1527B/2527B			Si3525B Si3527B			Units
			Min	Typ	Max	Min	Typ	Max	
	Error Amplifier Section (V_{CM} = 5.1 Volts)								
19	Input Offset Voltage			0.5	5		2	10	mV
20	Input Bias Current			1	10		1	10	µA
21	Input Offset Current				1			1	µA
22	DC Open Loop Gain	RL ⩾ 10 MegΩ	60	75		60	75		dB
23	Gain-Bandwidth Product[4]	A_V = 0 dB, T_j = 25°C	1	2		1	2		MHz
24	Output Low Level			0.2	0.5		0.2	0.5	V
25	Output High Level		3.8	5.6		3.8	5.6		V
26	Common Mode Rejection	V_{CM} = 1.5 to 5.2V	60	75		60	75		dB
27	Supply Voltage Rejection	V_{IN} = 8 to 35V	50	60		50	60		dB
	P.W.M. Comparator								
28	Minimum Duty Cycle				0			0	%
29	Maximum Duty Cycle		45	49		45	49		%
30	Input Threshold[5]	Zero Duty Cycle	0.6	0.9		0.6	0.9		V
31	Input Threshold[5]	Max Duty Cycle		3.3	3.6		3.3	3.6	V
32	Input Bias Current[4]			.05	1.0		.05	1.0	µA
	Soft–Start Section								
33	Soft Start Current	$V_{SHUTDOWN}$ = 0V	25	50	80	25	50	80	µA
34	Soft Start Voltage	$V_{SHUTDOWN}$ = 2V		0.4	0.6		0.4	0.6	V
35	Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V		0.4	1.0		0.4	1.0	mA
	Output Drivers (Each Output) (V_C = 20 Volts)								
36	Output Low Level	I_{SINK} = 20 mA		0.2	0.4		0.2	0.4	V
37		I_{SINK} = 100 mA		1.0	2.0		1.0	2.0	V
38	Output High Level	I_{SOURCE} = 20 mA	18	19		18	19		V
39		I_{SOURCE} = 100 mA	17	18		17	18		V
40	Undervoltage Lockout	V_{Comp} and V_{SS} = high	6	7	8	6	7	8	V
41	Collector Leakage[6]	V_C = 35V			200			200	µA
42	Rise Time[4]	C_L = 1 nF, T_j = 25°C		100	600		100	600	nsec
43	Fall Time[4]	C_L = 1 nF, T_j = 25°C		50	300		50	300	nsec
44	Shutdown Delay[4]	V_{SH} = 3V, C_S = 0, T_j = 25°C		0.2	0.5		0.2	0.5	µsec
	Total Standby Current								
45	Supply Current	V_{IN} = 35V		14	20		14	20	mA

CMCD

4 These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
5 Tested at f_{OSC} = 40 kHz (R_T = 3.6 kΩ, C_T = .01 µF, R_D = 0Ω).
6 Applies to Si1525B/2525B/3525B only, due to polarity of output pulses.

TENTATIVE DATA SHEET. *This page provides tentative information on a new product. Siliconix reserves the right to change specifications for this product in any manner without notice.*

	Parameter	Conditions	Si1282B/2828B Si1282/2827B Min	Typ	Max	Si1282B/2828B Si1282/2827B Min	Typ	Max	Unit
	Error Amplifier Section (VCM = 5.1 Volts)								
18	Input Offset Voltage			0.6	5		2	10	mV
20	Input Bias Current			1	10		1	10	pA
21	Input Offset Current				1			1	pA
22	DC Open Loop Gain	RL ≥ 10 MegΩ	60	75		80	75		dB
23	Gain Bandwidth Product[4]	AV = 0 dB, TJ = 25°C	1	2		1	2		MHz
24	Output Low Level			0.2	0.5		0.2	0.5	V
25	Output High Level		3.8	5.5		3.8	5.8		V
26	Common Mode Rejection	VCM = 1.5 to 5.2V	60	75		60	75		dB
27	Supply Voltage Rejection	VIN = 8 to 35V	60	80		60	80		dB
	PWM Comparator								
28	Minimum Duty Cycle				0			0	%
29	Maximum Duty Cycle		45	49		45	49		%
30	Input Threshold[5]	Zero Duty Cycle	0.8	0.8		0.8	0.8		V
31	Input Threshold[5]	Max Duty Cycle	3.2	3.5		3.2	3.5	3.8	V
32	Input Bias Current[4]			.05	1.0		.05	1.0	µA
	Soft–Start Section								
33	Soft Start Current	VSHUTDOWN = 0V	75	80	90	75	80	90	µA
34	Soft Start Voltage	VSHUTDOWN = 2V		0.4	0.6		0.4	0.6	V
35	Shutdown Input Current	VSHUTDOWN = 2.5V		0.4	1.0		0.4	1.0	mA
	Output Drives (Both Output) (VIN = 20 Volts)								
36	Output Low Level	ISINK = 20 mA		0.2	0.4		0.2	0.4	V
37		ISINK = 100 mA		1.6	2.0		1.6	2.0	V
38	Output High Level	ISOURCE = 20 mA	18	19		18	19		V
39		ISOURCE = 100mA	17	18		17	18		V
40	Undervoltage Lockout	VComp and VEa = high	6	7	8	6	7	8	V
41	Collector Leakage[6]	VC = 35V			200			200	µA
42	Rise Time[4]	CL = 1 nF, TJ = 25°C		100	200		100	200	nsec
43	Fall Time[4]	CL = 1 nF, TJ = 25°C		50	200		50	200	nsec
44	Shutdown Delay[4]	VSH = 3V, CS = 0, TJ = 25°C		0.2	0.5		0.2	0.5	µsec
	Total Standby Current								
45	Supply Current	VIN = 35V		14	20		14	20	mA

[4] These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
[5] Tested at fOSC = 40 kHz (RT = 2.8 kΩ, CT = .01 µF, RD = 0Ω).
[6] Applies to Si1282/2828/2827/2828 only; due to polarity of output pulse.

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A/D CONVERTERS

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Siliconix

Introduction to Quantized Feedback

INTRODUCTION

Siliconix' "Quantized Feedback" (or charge balancing as it is sometimes called) approach towards A/D conversion is an integrating technique, implemented through the use of an analog processor and digital controller. Intrinsic features of this approach are Auto-Polarity, Auto-Zero and ratiometric operation. As we shall see, this technique offers superior linearity, normal mode rejection and stability over that of other integrating techniques while at the same time requiring no critical components except a stable voltage reference.

Let's begin our discussion by considering the following op-amp adder:

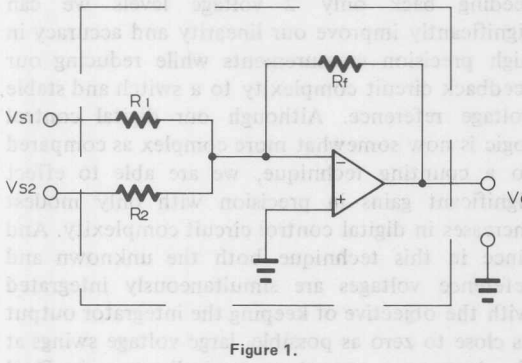


Figure 1.

$$\text{where } V_0 = -\left(\frac{R_f V_{S1}}{R_1} + \frac{R_f V_{S2}}{R_2}\right)$$

Recalling basic op-amp operation, it is easy to see that the output voltage V_0 is equal to the algebraic sum of V_{S1} and V_{S2} appropriately scaled. By taking this simple adder circuit and a few additional components it is possible to construct a rudimentary A/D converter as shown in Figure 2.

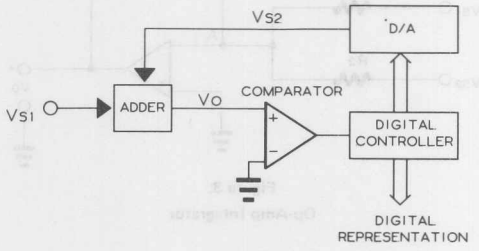


Figure 2.
Rudimentary A/D Converter

$$\frac{V_{S1}}{R_1} \approx -\frac{V_{S2}}{R_2} \therefore V_0 \approx 0$$

V_{S1} must be stable during conversion ∴ requires S/H in front end.

If V_{S1} is the unknown voltage that we would like to measure and V_{S2} an input voltage that we control, then by examining the state of V_0 and feeding back a V_{S2} sufficient to cancel out V_{S1}, (i.e. keep V_0 as close to zero as possible) we can digitally keep track of V_{S1} as diagrammed in Figure 2.

This is the technique used by successive approxi- D/A (greater than 8 bits input) which would be necessary to construct a high-precision A/D could prove prohibitive both in cost and circuit complexity. A more accurate and less complex approach as we shall see, would be to feed back just 2 voltage levels (say + V_{ref1}, $-V_{ref2}$) instead of the multitude of voltages possible with a D/A. However in using this approach we become interested in the time average of the feedback voltage as compared to the voltage under measurement, since we are now restricted to 2 voltage levels which should bracket the input voltage to be measured.

This being the case we now want to change our simple op-amp adder (of Fig. 1) into an integrator (Fig. 3) to perform the necessary averaging function.

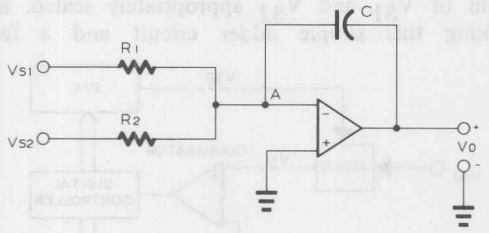


Figure 3.
Op-Amp Integrator

where $V_0 = -1/C \int \left(\frac{V_{S1}}{R_1} + \frac{V_{S2}}{R_2} \right) dt$

Once again V_{S1} is the unknown voltage we would like to measure and V_{S2} one of two voltage levels returning from our feedback network. We examine V_0 and feed back a voltage (V_{S2}) such that the time average of V_{S2} is sufficient to cancel out the analog unknown, V_{S1}. However since the input node (point A in Figure 3) to our analog adder is really a virtual ground, what we are really trying to balance out are the 2 currents flowing into the node (i.e. $\frac{V_{S1}}{R_1}$ and $\frac{V_{S2}}{R_2}$). This is easily seen in the integrator circuit (Fig. 3) where the quantity that V_{S1} V_{S2} zero as possible is the charge on the capacitor C as supplied by V_{S1} and V_{S2}. But since in our averaging process the feedback V_{S2} can only assume one of 2 voltage levels for an integer number of *time units,* we can only add or take away capacitor charge in quantum lumps ($-1/C \frac{V_{ref1}\ dt}{R_2}$ or $+ 1/C \frac{V_{ref2}\ dt}{R_2}$), thus giving us our technique name *quantized feedback.* A block diagram of such an A/D converter is shown in Figure 4.

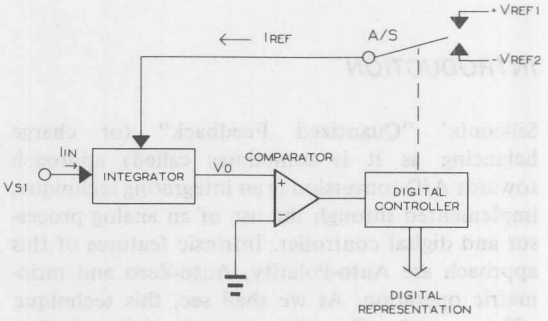


Figure 4.
Quantized Feedback A/D Converter

Figure 4 is the quantized feedback technique in its most basic form. As previously mentioned, by feeding back only 2 voltage levels we can significantly improve our linearity and accuracy in high precision measurements while reducing our feedback circuit complexity to a switch and stable voltage reference. Although our digital control logic is now somewhat more complex as compared to a counting technique, we are able to effect significant gains in precision with only modest increases in digital control circuit complexity. And since in this technique both the unknown and reference voltages are simultaneously integrated with the objective of keeping the integrator output as close to zero as possible, large voltage swings at the integrator output as typically seen in Dual Slope converters are avoided, thus easing integrator requirements. This dynamic feedback measurement process also ensures equally spaced count transition windows under varying conversion rates; even

around zero. Although timing is now critical to proper high resolution operation, our task is easily met through dedicated digital-control logic. Another feature inherent in this technique is that since we are trying to balance charges which are proportional to the input voltages, scale changes are easily accomplished through simple ratiometric resistor (R_1 and R_2) changes (i.e. Fullscale α R_1/R_2).

The basic principles underlying the quantized feedback technique should now be apparent, as well as the fundamental relationship between the voltage-under-measurement (V_{IN}, formerly V_{SI}) and our 2 feedback voltage levels V_{ref1} and V_{ref2}. That is, the current supplied by V_{IN} must be of opposite polarity and lie within the range bounded by the reference currents, $I_{ref2} \leq I_{in} \leq I_{ref1}$, (see Fig. 4) in order for V_{IN} to be measured. So in order to measure a $\pm V_{IN}$ using our simple system, we would have to supply both a $\pm$ reference voltage. We are also limited in our simple system to measuring single ended inputs (i.e. no common mode voltage). Siliconix however, has overcome these problems through an enhancement of the basic technique in which only 1 polarity V_{ref} is necessary for auto-polarity operation and where a zeroing measurement is automatically performed. Briefly, the way it is done is through the use of negative feedback to impress a system offset voltage when zeroing.

Let's now look at Figure 5 which is a diagram of the analog processor architecture as found in the Siliconix LD111A, LD120 and LD122 (the input buffer is user-supplied). Note that outside of a few additions, this circuit closely resembles our basic Quantized Feedback Converter (Figure 4). We still have the integrator summing node, pin 9 fed by a voltage reference source, unknown input voltage source, and (new here) an Auto-Zero (whose use will soon be explained) voltage source. The control logic near the Auto-Zero buffer is used by the digital controller to implement the

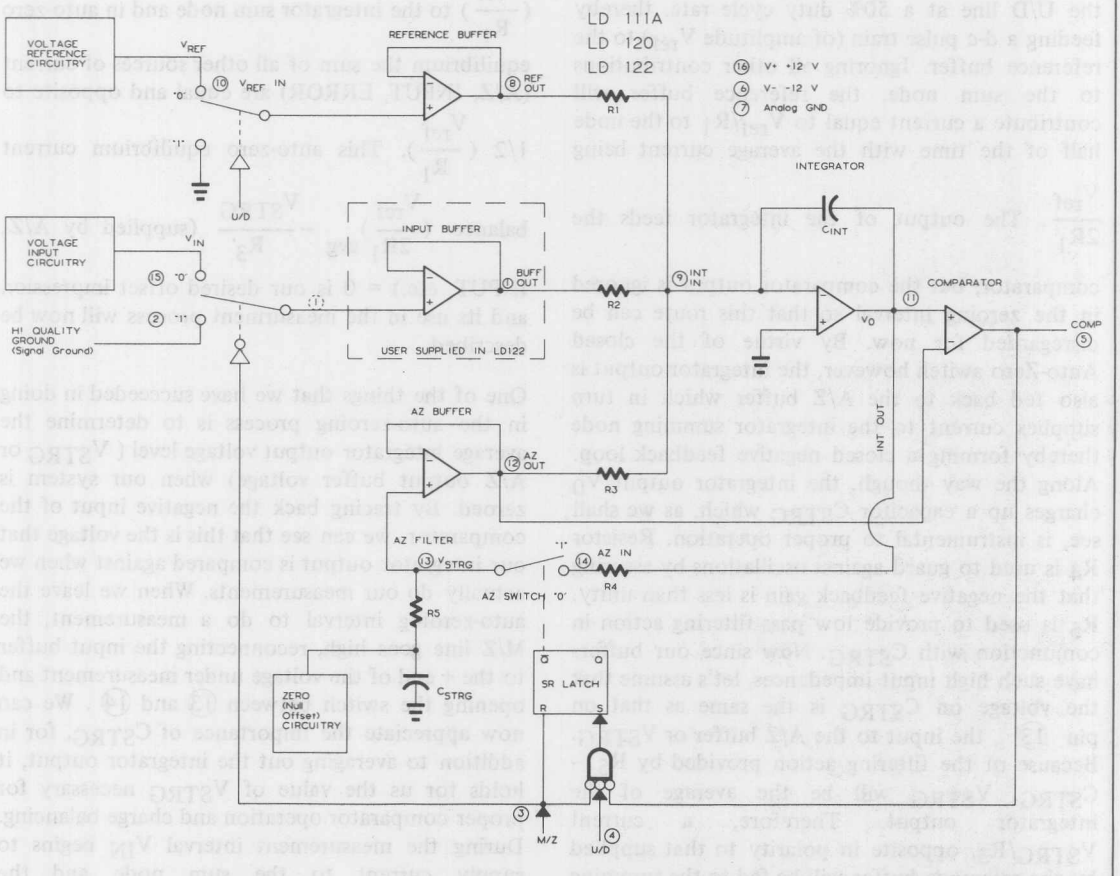


Figure 5. Siliconix Analog Processor

measurement algorithm. All of the inputs are now unity buffered so that loading effects on inputs are effectively eliminated. As before the output of the integrator is fed to a comparator whose output COMP 5 is monitored by the digital control logic. A feedback control signal UP/DOWN, U/D 4, from the digital controller determines which of 2 reference voltage levels (V_{ref} or GND) are to be fed back. The addition of the Measure/Zero M/Z 3 control line permits the division of our sampling process into 2 parts, a zeroing and a measuring interval.

The aforementioned system offset impression is accomplished in an auto-zeroing interval which is of sufficient duration to ensure equilibrium conditions. In the auto-zeroing interval the M/Z line is set low, connecting the input buffer to the input signal ground (or negative input if doing differential measurements). With the combination of the other 2 control lines U/D and COMP, the SR latch is set, forcing the switch between pins ⑬ and ⑭ closed. The digital control logic toggles the U/D line at a 50% duty cycle rate, thereby feeding a d-c pulse train (of amplitude V_{ref}) to the reference buffer. Ignoring all other contributions to the sum node, the reference buffer will contribute a current equal to V_{ref}/R_1 to the node half of the time with the average current being $\frac{V_{ref}}{2R_1}$. The output of the integrator feeds the comparator, but the comparator output is ignored in the zeroing interval so that this route can be disregarded for now. By virtue of the closed Auto-Zero switch however, the integrator output is also fed back to the A/Z buffer which in turn supplies current to the integrator summing node thereby forming a closed negative feedback loop. Along the way though, the integrator output V_0 charges up a capacitor C_{STRG} which, as we shall see, is instrumental to proper operation. Resistor R_4 is used to guard against oscillations by assuring that the negative feedback gain is less than unity. R_5 is used to provide low pass filtering action in conjunction with C_{STRG}. Now since our buffers have such high input impedances, let's assume that the voltage on C_{STRG} is the same as that on pin ⑬, the input to the A/Z buffer or V_{STRG}. Because of the filtering action provided by $R_5 - C_{STRG}$, V_{STRG} will be the average of the integrator output. Therefore, a current V_{STRG}/R_3, opposite in polarity to that supplied by the reference buffer will be fed to the summing node. With a little imagination we can envision that the DC or time average of all the currents flowing into the integrator sum node will eventually cancel each other out and in equilibrium the net current will equal zero. There will however, be an integrator output voltage V_0 the average of which will be V_{STRG} and both will be opposite in polarity to the V_{ref} voltage. Thus far all mention of the input buffer and error/offset currents have been avoided, but it can easily be seen that any current supplied through the input buffer from the negative differential input (Hi-Quality Ground ②) as well as any error currents will simply either aid or oppose the A/Z buffer in its attempts to balance out current from the reference source. Consequently in equilibrium, the V_{STRG} will be shifted slightly from what it would have been had none of these other current sources been present. Of course we assume that these additional sources do not change appreciably with time when we later move into the measurement interval. The key point to remember here is that the reference buffer is constantly supplying an average current of 1/2 $(\frac{V_{ref}}{R_1})$ to the integrator sum node and in auto-zero equilibrium the sum of all other sources of current (A/Z, INPUT, ERROR) are equal and opposite to 1/2 $(\frac{V_{ref}}{R_1})$. This auto-zero equilibrium current balance $(\frac{V_{ref}}{2R_1})_{avg} - \frac{V_{STRG}}{R_3}$ (supplied by A/Z, INPUT, etc.) = 0 is our desired offset impression and its use in the measurment process will now be described.

One of the things that we have succeeded in doing in the auto-zeroing process is to determine the average integrator output voltage level (V_{STRG} or A/Z output buffer voltage) when our system is zeroed. By tracing back the negative input of the comparator, we can see that this is the voltage that our integrator output is compared against when we actually do our measurements. When we leave the auto-zeroing interval to do a measurement, the M/Z line goes high, reconnecting the input buffer to the + end of the voltage under measurement and opening the switch between ⑬ and ⑭. We can now appreciate the importance of C_{STRG}, for in addition to averaging out the integrator output, it holds for us the value of V_{STRG} necessary for proper comparator operation and charge balancing. During the measurement interval V_{IN} begins to supply current to the sum node and the comparator output is closely monitored by the

digital controller. In response to the state of COMP, the controller feeds back either V_{ref} or GND to the reference buffer by toggling the U/D line. Measurement now is exactly as described in our simple A/D converter circuit (Figs. 3 & 4). However since all of our equilibrium conditions in auto-zero were calculated with an average $\frac{V_{ref}}{2}$ being fed into the reference buffer, feeding back a constant V_{ref} will result in a net current over and above that in equilibrium of $+V_{ref}/2R_1$ being sent to the sum node. Likewise feeding back a constant GND will cause a net current of $-V_{ref}/2R_1$ (from A/Z, etc.) to flow into the sum node. So whatever polarity V_{IN} may be, we will be able to balance it out with appropriate resistor scaling. An interesting aside here is that in all of our discussions the absolute polarity of V_{ref} (i.e. + or – with respect to GND) was never specified and any polarity could have been used with equal, but differing polarity results. However due to the nature of the switch Siliconix uses with the V_{ref} buffer (PMOS) only positive references will work.

THE "QUANTIZED FEEDBACK" ALGORITHM

The measurement algorithm used by all of our digital processor chips (LD110, 114, 121A) is basically the same. There are some minor variations due to slightly different analog control structures and the different precision that each

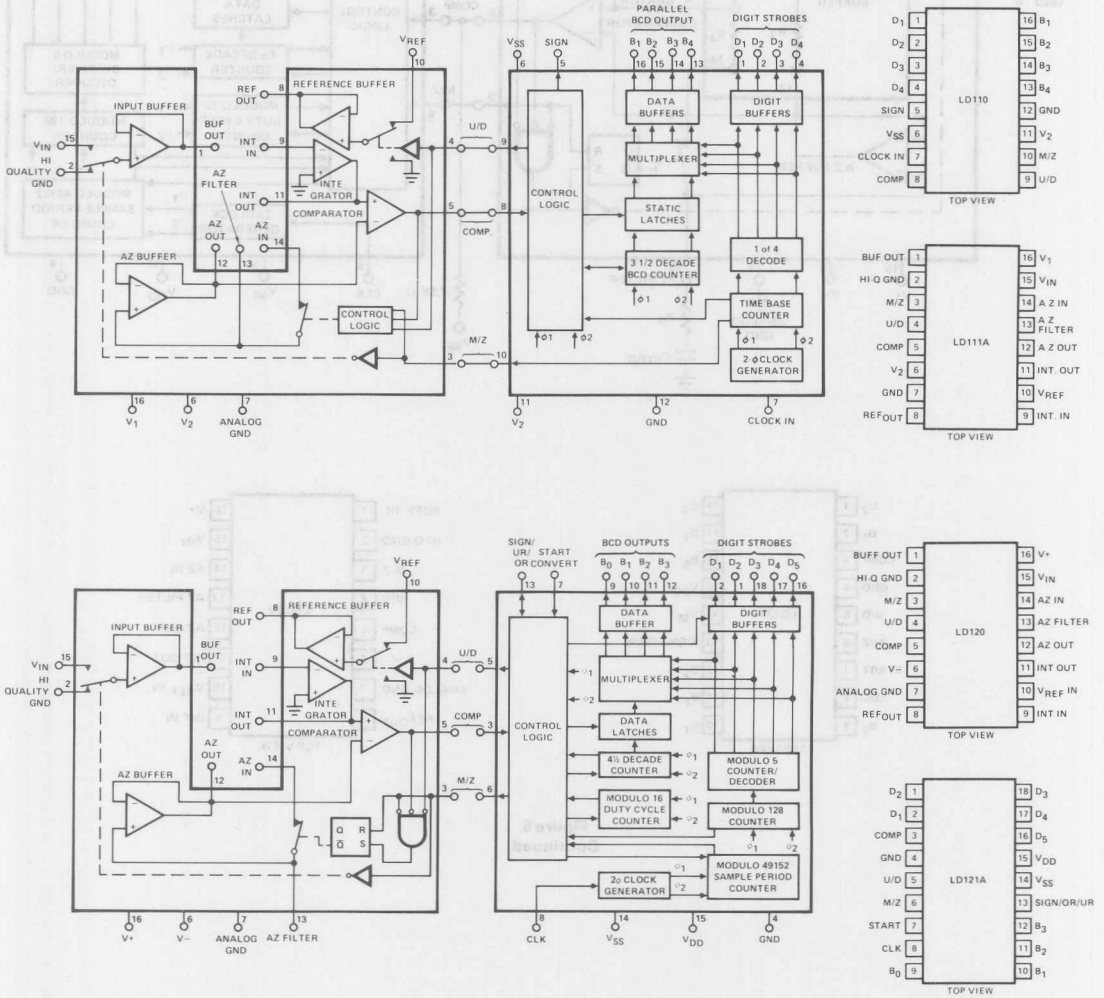
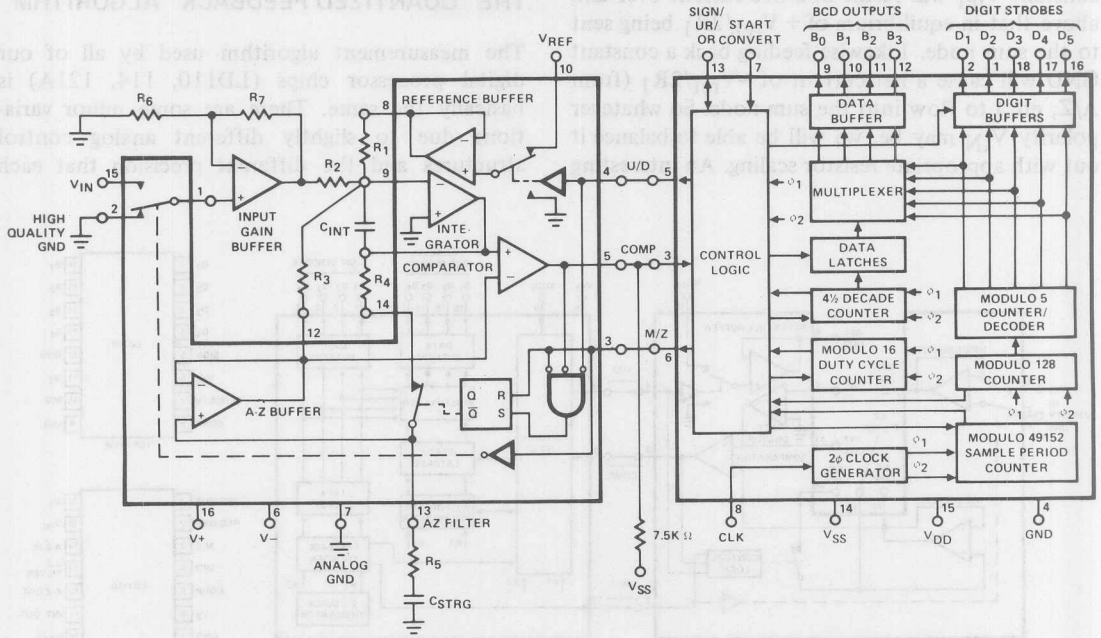
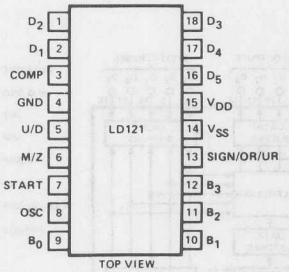


Figure 6

their timing from a stable clock signal generated either internally or externally. Inside the chip and typical analog processor interfacing for each of the digital controllers.





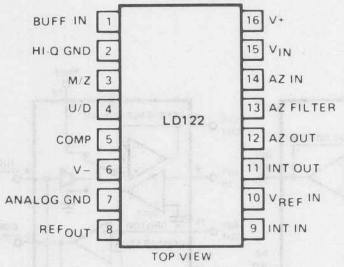


Figure 6 Continued

Every sampling interval is composed of an integral number of clock periods (LD110 = 6144, LD121A = 49,152). The sampling interval can be further subdivided into 2 operational periods, the Auto-Zero (A/Z) and Measure intervals. The A/Z interval, as we know, gives us a means of nulling offset voltages and establishing a second tracking reference voltage necessary for bipolar conversion. The interval is signified by the Measure-Zero control line (M/Z) going low and consists of the following number of clocks: LD110 = 2048, LD121A = 16,384. In the Measurement interval (when M/Z = 1), the actual charge balancing process is implemented and consists of the following number of clocks: LD110 = 4096, LD121A = 32,768. As you may have noticed, A/Z makes up 1/3 and Measure Interval 2/3's of the sampling interval. The reason why such a significant fraction of time is devoted to A/D to insure that equilibrium zero conditions are attained. The M/Z line is the principal signal to the analog circuitry to tell it which interval it is in so that the appropriate switches can be closed. The Up-Down (U/D) line, on the other hand, is responsible for controlling the reference voltage fed back in the A/Z and Measure Intervals. As we may recall, during the A/Z interval a 50% duty cycle pulse train of V_{REF} amplitude is fed back in the analog system. This is accomplished by toggling the U/D line once every 4 clocks in the LD110 and once every 8 clocks in the LD121A.

Figure 7 shows typical waveforms in the auto-zero interval for the LD110. The LD121A has essentially the same timing except that twice as many clocks are required for U/D toggling.

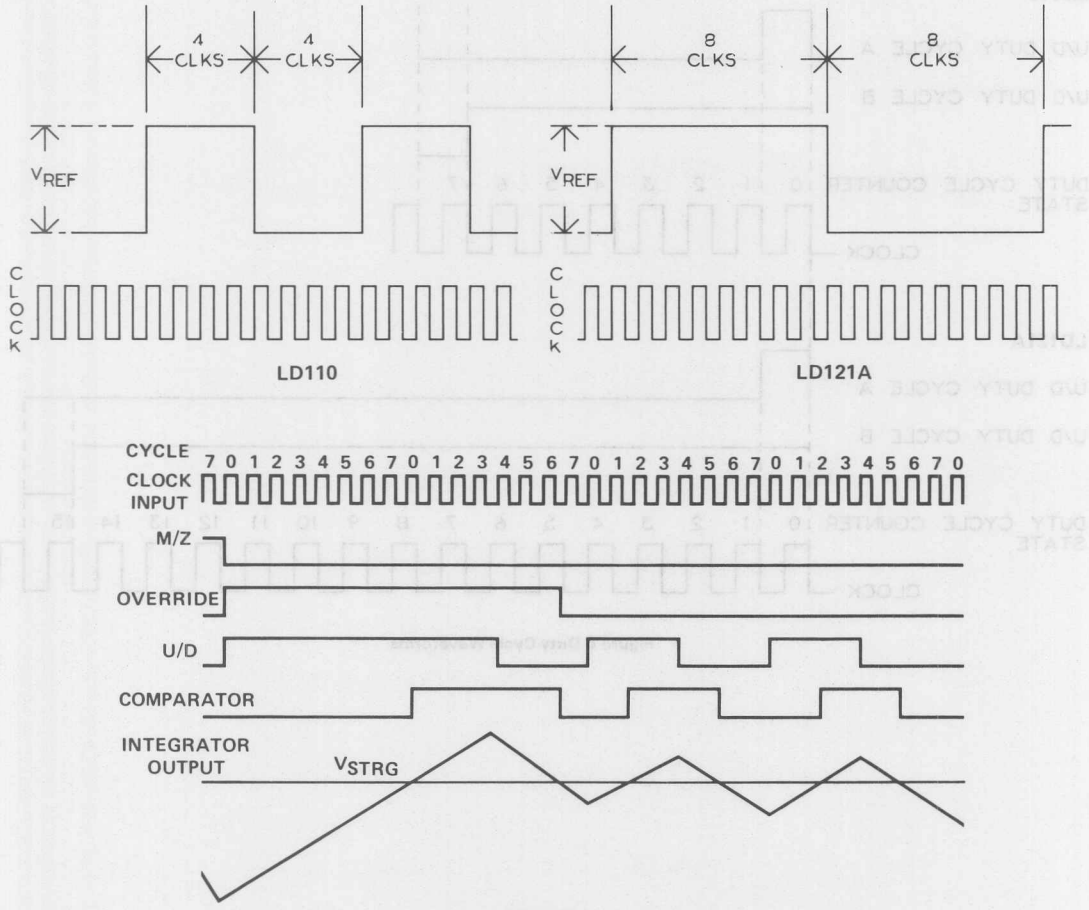


Figure 7
Auto-Zero Timing

In the measure interval, where we attempt to balance integrator charge, U/D is set in response to the state of the COMP input, so that the appropriate reference voltage will be fed back in the analog system. A counter automatically increments or decrements once every clock cycle, depending on the state of the U/D line, so that an accurate record can be kept of the net number of charge packets fed back. Ordinarily one would think that once every clock cycle the U/D would be set accordingly. However, since this technique is as dependent on timing as it is on feedback voltage level, we really have to be mindful of U/D transitions since they bring with them error in the form of rise and fall time. One way around this problem is to insure that in every measure interval there is always the same number of U/D transitions, irrespective of the unknown, V_{IN}. This can be done by dividing the measure interval into an integral number of duty cycle periods in which the U/D line can assume 1 of 2 duty cycle waveforms. In the LD121A the duty cycle period consists of 16 clocks while it's 8 in the LD110. The 2 duty cycle waveforms possible in each 16 or 8 clock period is:

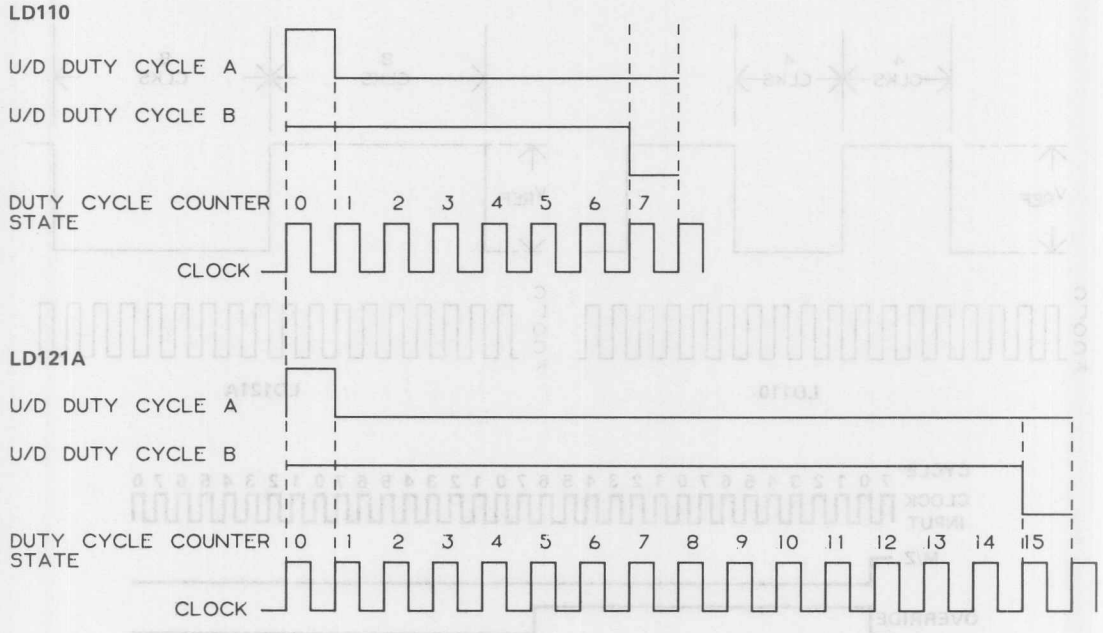


Figure 8 Duty Cycle Waveforms

So instead of depositing a maximum possible (±16 or ±8) charge packets every duty cycle period, we have to be content with a net maximum of ±14 or ±6. Consequently the maximum counts possible are: LD110 = 3072, LD121A = 28,672. However, since these maximum counts are larger than the advertised precision of the A/D's, overrange capability is possible and built into some of the converters.

Since we can only feedback rather large lumps of charge (±14, ±6 counts), when the measure interval comes to an end, there will, undoubtedly, be some residual charge left over to be resolved to the nearest count. This is done in a brief override period at the start of the A/Z interval where normal A/Z operation is temporarily inhibited while we fine tune (i.e. abandon duty cycles and feedback charge packets one at a time). The override period starts at the end of the measure interval when M/Z → low and the input buffer is switched to input 'gnd' so that no more charge is accumulated. The U/D line is set high and held until the comparator goes high and the next *state 8* of the duty cycle counter comes around at which time U/D is set low. When the comparator next goes low again, the override period is ended (M/Z = 0, COMP = 0, U/D = 0, Auto-Zero switch closes initiating normal Auto-Zero action). The counter which until now has been faithfully keeping track of the charge packets fed back, is inhibited and its count used to update the data outputting latches on the next clock pulse. Figure 9 shows typical Measure, Override, and Auto-Zero waveforms in an LD120/LD121A system.

Now that the measurement algorithm has been described, a few words about the relationship between the count and unknown input voltage are in order. What the count represents is the net number of reference charge units ($\pm \frac{V_{REF}}{2R_1} \frac{1}{f_{CLK}}$) which were needed to cancel out the charge as supplied by the unknown input

$$(\frac{V_{IN}}{R_2} \cdot \frac{\#\text{ clocks in measure interval}}{f_{CLK}}).$$

Neglecting signs, this equality is:

$$\text{COUNT} \cdot \frac{V_{REF}}{2R_1} \cdot \frac{1}{f_{CLK}} =$$

$$\frac{V_{IN}}{R_2} \cdot \frac{\#\text{ clocks in measure interval}}{f_{CLK}}$$

rearranging, this becomes:

$$\text{COUNT} = \frac{V_{IN}}{V_{REF}} \cdot \frac{R_1}{R_2} \cdot 2$$

(# clocks in measure interval).

For an LD121A with 32,768 clocks in the measure interval, this equality becomes:

$$\text{COUNT} = \frac{V_{IN}}{V_{REF}} \cdot \frac{R_1}{R_2} \cdot 65{,}536$$

By manipulating the resistor ratios and V_{REF} we could theoretically scale the A/D to any input voltage range desired. Practical circuit limitations, though, prevent us from getting carried away.

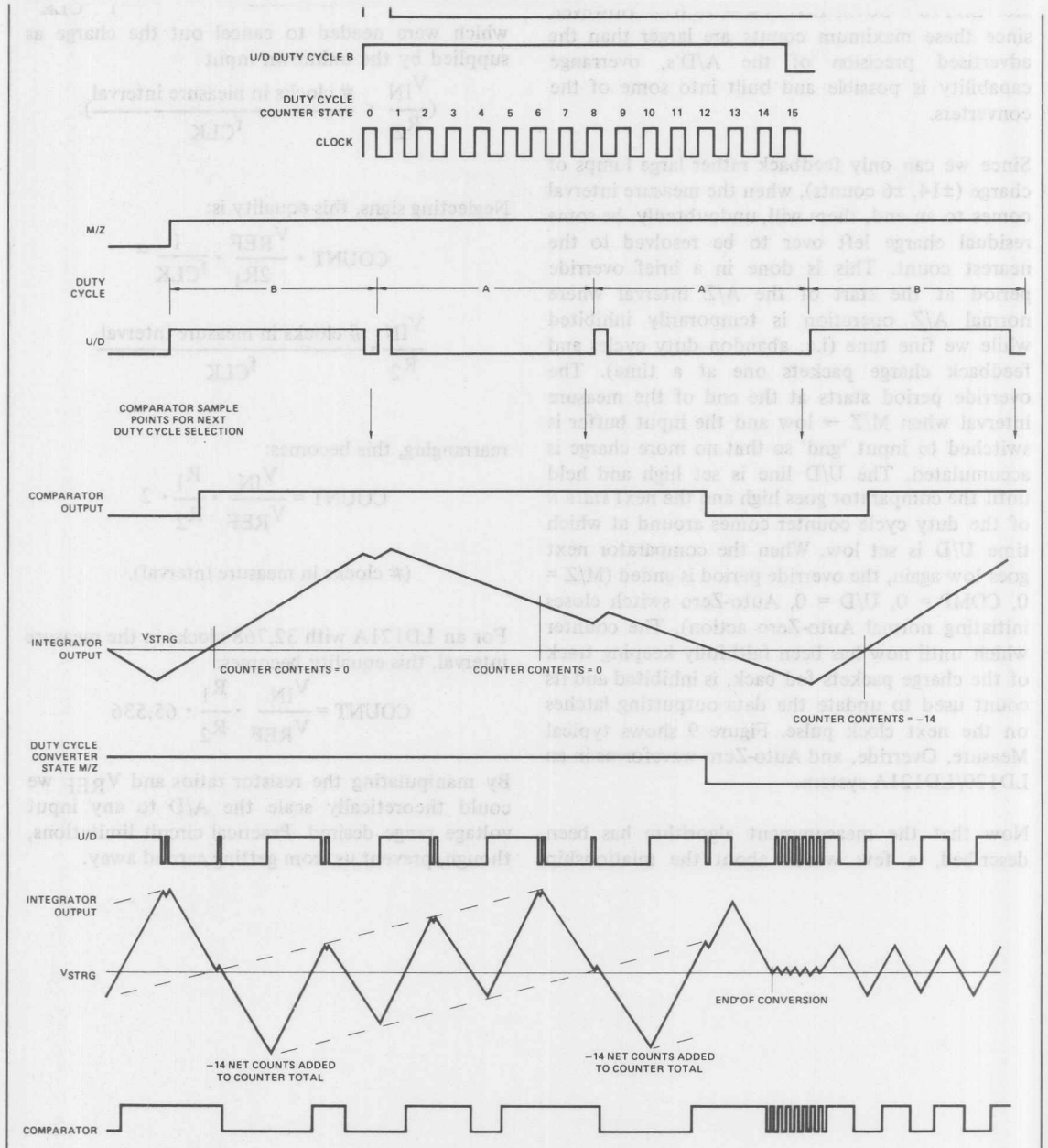


Figure 9. Up/Down and Integrator Waveforms

Siliconix

Microprocessor Interface Techniques As Applied to the Siliconix A/D Converter Family

INTRODUCTION

When attempting to interface a microprocessor system with a peripheral device (in this case an A/D) that operates at a substantially slower speed, the communications process between the system and peripheral can be thought of as lying between two extremes, synchronous and asynchronous operation. Either mode of operation will offer trade-offs between speed or throughput, and hardware complexity. For instance, in a synchronous communications approach, overall system speed is effectively reduced to that of the slow peripheral as the system must wait for a response or handshake from it. In an asynchronous approach however, both the system and the peripheral are able to operate at their own respective clock rates, with the speed differential problem being solved through the use of an interface buffer between the two. Hardware complexity is considerably higher here though than in a handshaking synchronous interface because such an asynchronous buffer is usually implemented through the use of latches to retain all of the data.

More often than not in A/D application notes or data sheets where an interface to a microprocessor is shown, the approach taken is the use of a peripheral interface chip such as an 8255 PPI or a 6820 PIA. While this approach will ultimately get the job done, it's extremely costly in terms of all of the negative features of both asynchronous and synchronous approaches (high hardware cost - peripheral interface chips aren't cheap; slowness - we are essentially operating synchronously with the A/D). As an added drawback, there's the software overhead necessary to initialize the chip and implement the synchronizing software routines. It's possible however, as we'll soon see, to construct totally synchronous and asynchronous interfaces out of common TTL parts costing only 1/3 to 1/2 the price of a peripheral interface chip and requiring none of the software overhead.

The circuits to be presented were built with the LD121A, but are of a sufficiently general nature that they can easily be modified to accommodate the other A/D's in the Siliconix product line.

LD121A DATA FORMAT

Just to review, Figure 1 shows the output data format of the LD121A digital controller and as you can see, data is BCD and sent out digital serial - bit parallel, perfect for multiplexed displays for which it was designed. The sequence in which the BCD digits are sent out is D5, D4, D3, D2, D1, repeating continously as indicated. Note that the BCD data for a particular digit is available (16 LD121A clock cycles) both before and after the digit strobe comes on, a feature of which we shall make good use. Sign data appears 250 ns after the D5 strobe and is valid for the duration of D5. Although not shown here, a means of determining that the A/D has completed a measurement and has new data available is the positive edge of a signal called M/Z which occurs once every measurement interval. Complete LD120/LD121A operational information may be obtained by consulting the data sheet. All of the LD121A digital output signals can drive 1 standard TTL load and the M/Z line – 1/2 a load, a factor which contributed to the use of 74LS parts as much as possible in my circuits.

Since the synchronous interface is the simpler of the two, let's start with it first.

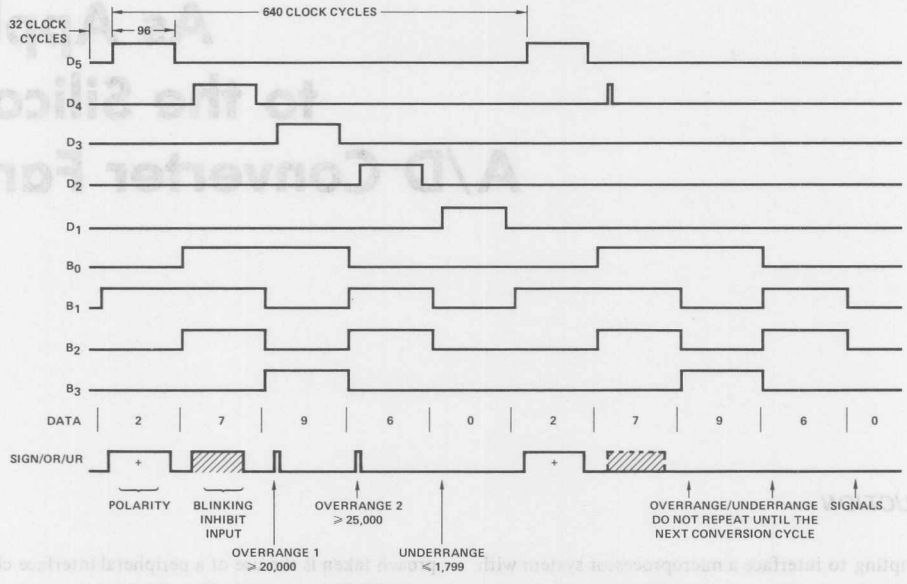


Figure 1. LD121 Digital Output Timing Diagram

SYNCHRONOUS A/D INTERFACE

In Figure 2 we have the schematic of an LD121A synchronous interface which was built and operated in an Intel SDK-85 system. Key to the operation of this circuit is the READY line which can be found on Intel, MOS Technology and other microprocessors. For those not familiar with it, the READY line is an input to the processor through which slow memories and in this case, slow peripherals can make the processor wait while data to be read in is being placed on the data bus. In this way the processor can be SYNCHRONIZED to the rate at which the slow peripheral is giving data, while running at full speed when other, faster, memories and peripherals are being accessed. The operation of the circuit is as follows. Normally the output to the READY input, A5 pin 5 is high, permitting full-speed processor operation. To accomplish this, all of the inputs to A5 must be low which is possible if none of the first 5 outputs of the 4 to 10 line decoder are active (low). Although the A, B, C inputs of A2 may change continously, by using the D input as a chip enable, the outputs in question will remain high. However when a valid chip select (read peripheral operation) comes along, the tristate bus buffer A1 will be enabled as well as the 4 - 10 line decoder. Now depending on the valid address on ADR 0, 1, 2 one of the decoder outputs, corresponding to a particular LD121A digit, will go low. Assuming that all of the digit strobes are low (inactive), the READY line goes low causing the processor to wait up. As soon as the digit strobe in question goes high, indicating valid data is available, the READY line rises again allowing the processor to continue its read operation. Note that the digits may be read in any order as the synchronization is accomplished automatically. However the processor does have to wait for the right digit strobe to come along. The 74LS74 D type F.F. in the circuit is used as an interrupt indicator latch, generating a latched high level interrupt

signal when the positive M/Z edge comes along (new data ready) and resetting when a data read occurs. Depending on how the chip select is generated, the circuit may be set up as regular or memory mapped I/O, the choice is up to the user. As set up, the BCD data is located in the low data nibble and the sign is the high order data bit. However considerable lattitude is possible both in data word configuration and parts selection, particularly in choosing the tristate bus buffer and decoder chips.

Lastly, after receipt of a valid chip select there's only a 3 gate delay in generation of a correct READY signal, permitting the circuit to be used with even the fastest of processors providing that they have a READY input.

ASYNCHRONOUS A/D INTERFACE

In Figure 3 we have the schematic of an asynchronous LD121A interface, also built and operated with an SDK-85. Although it's somewhat more complex than the previous circuit, relatively common parts are used and hardware costs are still well below that of a peripheral interface chip. Briefly, this circuit uses a 2101A memory as a 5 word X 4 bit latch to store the BCD data for immediate access later on by the microprocessor (i.e. no wait states). The 2101A was chosen because of its separate data inputs and outputs and is relatively cheap as far as memories go. Ordinarily LD121A BCD data is being written into the 2101A memory at addresses determined by encoding the LD121A digit strobes into 3 bit binary. The encoding is done by the A4 OR gates and the address is gated to the memory by the A2, A3 AND–NOR gates.

Note that 1/2 of the A3 AND–NOR chip is used to permit the storage of sign information as data bit DI_4 during digit strobe 5. The memory write pulse is generated by A7 and A8 and is a low level pulse of minimum duration so as not to interfere during microprocessor reads (i.e. lock up the A5 read-write arbitrator logic unnecessarily). Note the 0.01 μF capacitor on the trigger input to the A8 monostable. It's used to delay the generation of the write enable pulse so that the sign information which is slightly delayed from D5 (by 250 ns) will be valid. A5 is arbitration logic which determines whether a microprocessor read or LD121A data write is to be performed on the 2101A memory. The A5 outputs, pins 3, 6 control the A2, A3 AND–NOR gates and determine whether the 2101A memory address is to be supplied by the system address bus (read) or encoded digit strobes (write). A5 is also set up so that if a data write pulse is present from the monostable, its output pins 3, 6 will not change state (i.e. lock up). However when the write pulse ends, A5 will change state if necessary to reflect whether or not we have a valid chip select present (microprocessor read). If so, it will enable the memory data bus drivers, lock out monostable write pulses and gate the system address bus to the 2101A memory so that the read can be performed. When the chip select is in control of the A5 logic, further updating of the memory by the LD121A is inhibited until the chip select is removed.

Although I was using a 2101A-2N with a 250 ns access time, measurements showed that data could be obtained within 250 ns after application of a valid chip select, providing that there was no monostable write pulse to lock up the A5 logic at the time. In which case it would have taken 250 ns plus the width of the monostable write pulse. However I found it very difficult to coincidence the chip select and write pulse since the write pulse is so short and so infrequent. So except on very rare occasions, my read access time from application of a valid chip select was at most 250 ns. By being careful about how and when the processor determines that there is new data to be read in (i.e. further qualify the interrupt signal) any possible coincidence of chip select and write pulse can be totally avoided.

As in the previous circuit, the A9–74LS74 is used as an interrupt latch. The entire circuit is of sufficiently general purpose design that the only real limitation to using it with any processor is its 250 ns access time. Again, depending on how the chip select is generated the circuit may be set up as either regular or memory mapped I/O.

Through careful examination of both the asynchronous and synchronous schematics it can be seen that in each, the correspondence between a system address supplied and the BCD digit read is:

ADR 2	ADR 1	ADR 0	Digit
0	0	0	D1
0	0	0	D2
0	1	0	D3
0	1	1	D4
1	0	0	D5

A rough estimate of the savings in time possible using an asynchronous rather than an synchronous interface approach in this application would be something on the order of 1 complete LD121A data output cycle each time we read in all 5 digits. For a LD121A running at maximum clock frequency (250 KHz, 5 conversions/second) this is a savings of about 2.5 milliseconds each and every time. Since the asychronous circuit acts as though it were memory as far as the processor is concerned, the amount of time necessary to read in new data from it is essentially how quickly the processor can execute memory or I/O read commands, as the case may be, providing of course that read access times are met.

REFERENCES

1. Intel MCS-85 Users Manual, September 1980 Intel Corporation.

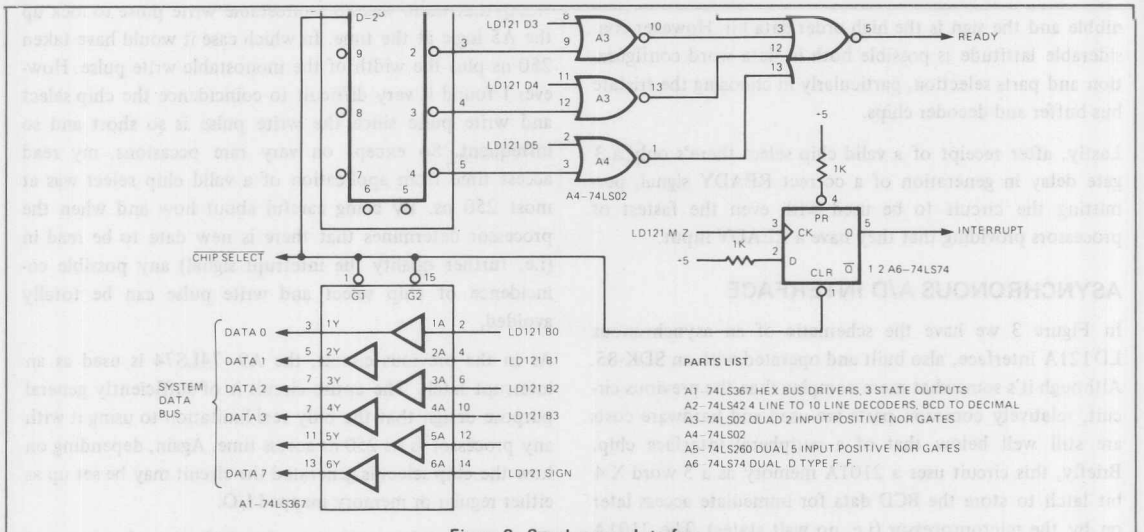


Figure 2. Synchronous Interface

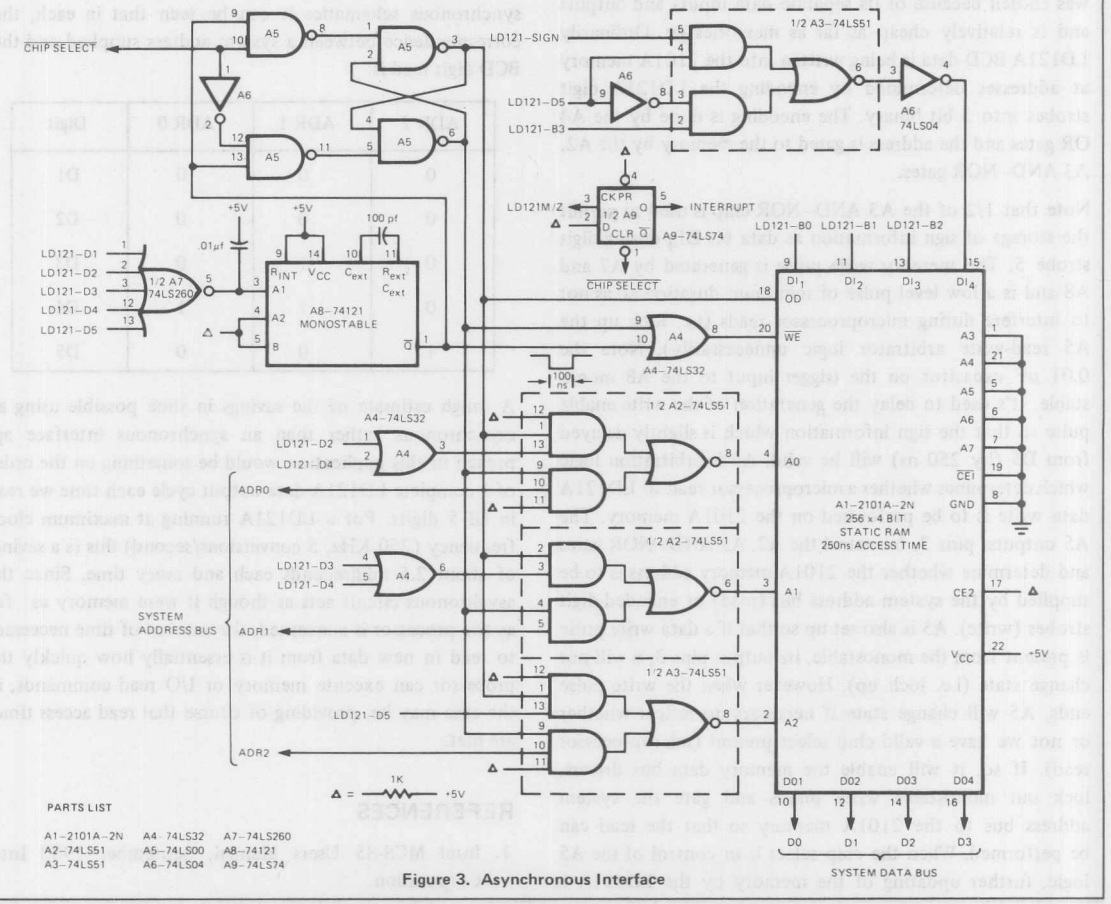


Figure 3. Asynchronous Interface

3½ Digit A/D Converter Set

Siliconix

designed for . . .

- **High Performance Digital Voltmeters**
- **Digital Panel Meters**
- **Digital Instrumentation Readouts**
- **Microprocessor A/D Interface Subsystem**
- **Auto-Zeroed Microvolt or Strain-Gauge Systems**

BENEFITS

- Three Usable Ranges with a Single Resistor Change. 1.999 V, 199.9 mV, 19.99 mV
- Excellent System Performance From Basic 0.02% ±1 Count Accuracy
- Wide Sampling Rate: 1/3 to 40/Second
- High Gain Stability (5 ppm/°C) with Buffered Reference Input
- Reduced Signal Loading with MOSFET Input ($Z_{IN} > 10^9\ \Omega$)
- Auto-Zero System Minimizes Internal and External Offset and Drift Over Temperature
- Auto-Polarity with a Single Reference
- Easy Interface to Displays with Strobed BCD Output Format
- Overrange and Underrange Signals Available

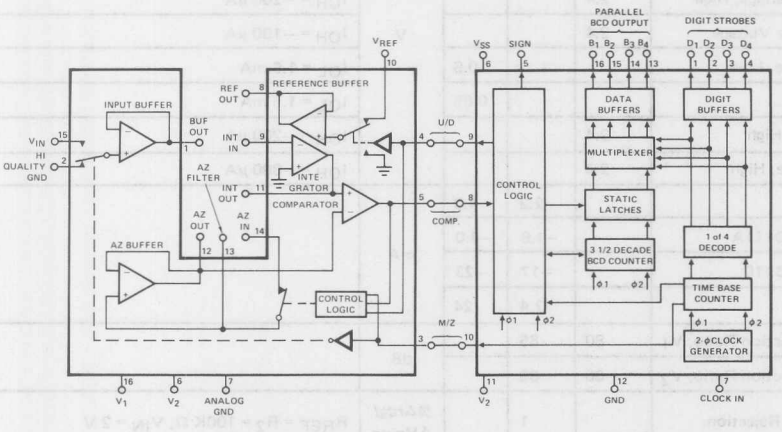
DESCRIPTION

The "Quantized Feedback" conversion scheme used in the LD110/LD111A set provides an Auto-Zeroing, Auto-Polarity A/D system requiring only a single reference voltage.

The monolithic LD111A high performance analog processor contains a bipolar comparator, a bipolar integrating amplifier, a bipolar reference amplifier, two MOSFET input unity gain amplifiers, several P-channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. The high impedance input and reference buffer amplifiers eliminate source loading errors and provide the outstanding temperature coefficient inherent in this system. Break-before-make switch action insures that neither the analog input nor the reference voltage will be shorted to ground at any time.

The PMOS LD110 synchronous digital processor combines the counting, storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing function of the analog processor. Seventeen static latches store the 3 1/2 digits of BCD data as well as overrange, underrange and polarity information. Nine push-pull output buffers (capable of driving one standard TTL load each) provide the sign, digit strobe and multiplexed BCD data outputs, all of which are active high. The digit scan is an interlaced format of digits 1, 3, 2 and 4.

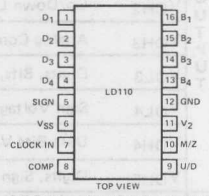
FUNCTIONAL DIAGRAM



SWITCH STATES ARE FOR A LOGIC "0" AT U/D AND M/Z INPUTS.

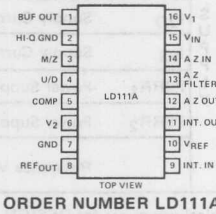
PIN CONFIGURATIONS

Dual-In-Line Package



ORDER NUMBER LD110CJ
SEE PACKAGE 8

Dual-In-Line Package



ORDER NUMBER LD111ACJ
SEE PACKAGE 8

ABSOLUTE MAXIMUM RATINGS

I_{IN} (Pin 15, 2) ±1 mA
$V_1 - V_2$ (LD111A) 30 V
V_{SS} 6 V
$V_{SS} - V_2$ (LD110) 20 V
V On Any Pin Relative to V_{SS} (LD110) . 0.3 V to −20 V
V_{REF} V_1

Operating Temperature 0 to 70°C
Storage Temperature −65 to +125°C
Power Dissipation (Package)* 750 mW

*Device mounted with all leads welded or soldered to PC board. Derate 6.3 mW/°C above 25°C.

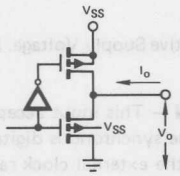
ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters to assure conformance with specifications.

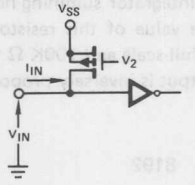
			Characteristics	Min	Typ	Max	Unit	Test Conditions, Unless Noted: V_1 = +12 V, V_2 = −12 V, V_{SS} = 5 V, V_{REF} = 8.2 V, T_A = 25°C, R_1 = 100K Ω
1	GENERAL		Linearity		0.02		% rdg	
2			Noise		0.1		LSB	Peak-to-Peak Noise Apparent When Going From One Steady Reading to Another
3			Gain T.C.		5		ppm/°C	
4		NMR	Normal Mode Rejection		40		dB	f_{noise} = 60 Hz
5		f_{IN}	Clock Frequency	2	30.7	250	kHz	50% Duty Cycle
6		$r_{DS(on)}$	ON Resistance, Auto Zero Switch		6	20	K Ω	$V_{AZ(in)}$ = −4.0 V, I_S = −30 μA
7	INPUT	I_{CL}	Clock Input Current, Low			−500	μA	$V_{CLOCK\ in}$ = 0.4 V
8		I_{IN}	Input Bias Current		4		pA	T_A = 25°C
9					40			T_A = 70°C
10		I_{INL}	Comp. LD110	−1500	−700	−50	μA	V_{IN} = −12 V
11	AMP	I_{source}	Reference Buffer	−400	−800		μA	V_{INL} (U/D) = 0.8 V, V_{OUT} = 0
12		I_{sink}	AZ Buffer		800			V_{AZ} = −4 V, V_{OUT} = 0 V
13		I_{sink}	Input Buffer	400	800			V_{IN} = −2 V, V_{OUT} = 0 V
14		I_{source}	Input Buffer	−50	−100			V_{IN} = 2 V, V_{OUT} = 0 V
15		V_{offset}	AZ Buffer	−100		100	mV	V_{OUT} = 0 V
16	OUTPUT	V_{OL1}	Measure/Zero Voltage, Low			0.6	V	I_{OL} = 150 μA
17		V_{OH1}	Measure/Zero Voltage, High	2.4				I_{OH} = −200 μA
18		V_{OL2}	Up/Down Logic Voltage, Low			0.6		I_{OL} = 250 μA
19		V_{OH2}	Up/Down Logic Voltage, High	2.4				I_{OH} = −200 μA
20		V_{OH3}	Analog Comparator Voltage	2.4				I_{OH} = −100 μA
21		V_{OL3}	Digits, Bits, Voltage, Low			0.6		I_{OL} = 1.6 mA
22		V_{OL4}	Sign Voltage, Low			0.65		I_{OL} = 1.6 mA
23		V_{OH4}	Data Bits Voltage, High	2.4				I_{OH} = −200 μA
24		V_{OH5}	Digits, Sign Voltage, High	2.4				I_{OH} = −800 μA
25	SUPPLY	I_1	Supply Current		2.2	4.0	mA	
26		I_{2A}	Supply Current, LD111A		−1.8	−4.0		
27		I_{2D}	Supply Current, LD110		−17	−23		
28		I_{SS}	Supply Current		17.4	24		
29		$PSRR_1$	Power Supply Rejection Ratio, V_1	80	85		dB	
30		$PSRR_2$	Power Supply Rejection Ratio, V_2	60	65			
31			Reference Voltage Rejection		1		%Δrdg/ ΔV_{REF}	R_{REF} = R_2 = 100K Ω, V_{IN} = 2 V

Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing **LD110 IPANII LD11A CMAMI-A**

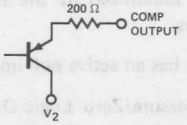
INPUT/OUTPUT SCHEMATICS



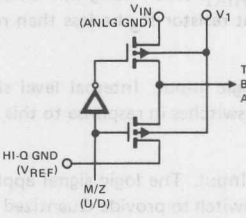
LD110 OUTPUT BUFFERS
(Digits, Bits, Sign, M/Z, U/D)



LD110 COMPARATOR, CLOCK INPUTS



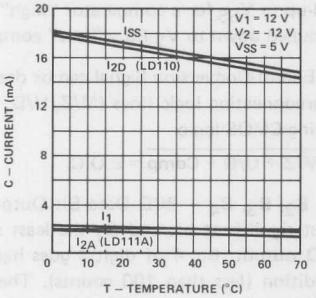
LD111A Comparator Output



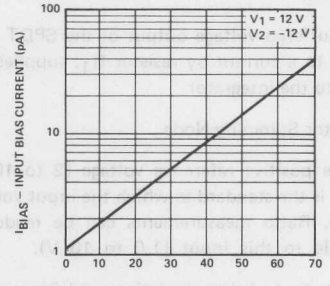
LD111A Inputs (V_{IN}, V_{REF})

TYPICAL CHARACTERISTICS

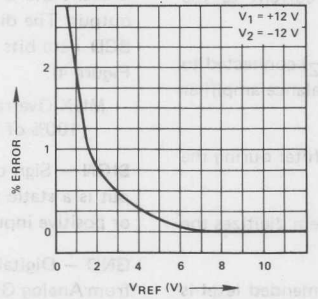
Supply Currents vs Temperature



Input Bias Current vs Temperature



Ratio Operation
(V_{IN}/V_{REF} = Constant)



10K Ω for a 200.0 mV full scale and 100K Ω for a 2.000 V full scale. The digital output is inversely proportional to the value of this resistor.

$$\text{Count} = \frac{V_{IN}}{V_{REF}} \frac{R_1}{R_2} 8192$$

HI-QUALITY GND – This pin, typically connected to a High Quality Ground point for single ended inputs *can be used as the inverting input for differential signals.* The digital output will be $V_{IN} - V_{HI\text{-}Q}$. When using this differential mode, it is important that resistor R_3 be less than resistor R_2 for proper operation.

M/Z – Measure/Zero Logic Input. Internal level shifting drivers operate the PMOS switches in response to this digital signal.

U/D – Up/Down Logic Input. The logic signal applied to this pin operates a SPDT switch to provide Quantized pulses of charge to the integrator.

COMP – This analog comparator output is an open collector configuration which goes to V_2 when "low."

V_2 – Negative Supply Voltage. Recommended level is –12 V ±10%.

GND – Analog Processor Ground. Should be kept separate from Digital Grounds.

REF_{out} – This buffered voltage output of the SPDT U/D switch, converted to a current by resistor R_1, supplies the reference current to the integrator.

INT. IN – Integrator Summing Node.

V_{REF} – A stable positive reference voltage (2 to 10 V) applied to this pin is the standard to which the input voltage V_{IN} is measured. Ratio measurements can be made by applying a variable to this input (1.0 to 10 V).

INT. OUT – The output of the integrating amplifier is made available for application to the Auto-Zero amplifier by means of resistor R_4.

AZ OUT – The output of the unity gain Auto-Zero amplifier provides a second negative reference current to the integrator through resistor R_3.

AZ FILTER – The Auto-Zero Capacitor (C_{AZ}) connected to this pin stores D.C. voltage components to balance amplifier offset and drift components.

AZ IN – This input is switched into the AZ filter during the zeroing interval.

V_{IN} – Analog Voltage Input. The A/D System digitizes the voltage appearing at this input.

V_1 – Positive Supply Voltage. The recommended level is +12 volts ±10%.

CLOCK IN – This input accepts a TTL or MOS level clock to drive the synchronous digital circuitry. Acceptable duty cycles on the external clock range from 30% high, 70% low to 70% high, 30% low for clock frequencies from 2 kHz to 250 kHz. Although any clock frequency between 2 kHz and 250 kHz may be used, clock frequencies that are integer divisions of $2048F_L$ ($F_{IN} = 2048F_L/n$, n = 1, 2, 3, . . . , 51), (F_L = Line Frequency) provide measure and zero periods that are integer multiples of the line frequency period ($T_{zero} = n/F_L$, $T_{measure} = 2n/F_L$). Line frequency interference is minimized by the selection of one of these 51 frequencies.

This input has an active pull-up to V_{SS}.

M/Z – Measure/Zero Logic Output. This 0 to 5 volt logic output successively provides Autozero and Measurement intervals of 2048 and 4096 clock periods respectively. This output is compatible with CMOS logic and directly interfaces with the LD111A analog processor.

U/D – Up/Down Logic Output. This output has logic levels of 0 and +5 volts to provide pulse-width modulation of the reference current when used with the LD111A analog processor. This output is CMOS compatible.

COMP – Analog Comparator Input. This input has an active pull-up to V_{SS} for a comparator "high" state. This pin must be pulled down to V_2 for a "low" comparator state.

An End-of-Conversion Signal can be decoded from the three interconnecting logic lines (M/Z, U/D, Comp) using the following CMOS logic.

$$\overline{M/Z + U/D + Comp} = E.O.C.$$

B_1, B_2, B_3, B_4 – BCD Data Bit Output. B_4 represents the most significant bit and B_1 the least significant bit of the BCD output. Bit 4 of digit 4 goes high for an underrange condition (less than 100 counts). These outputs are compatible with 1 standard TTL load.

MUX Underrange = $B_4 \times D_4$ (5% of full scale)

D_1, D_2, D_3, D_4 – Digit Strobe Outputs. D_4 is the most significant and D_1 the least significant digit of the 3 1/2 digit output. The digit strobes are each selected in turn when the BCD data bits for that digit appear at the bit outputs (see Figure 4).

MUX Overrange = $\overline{D_1 + D_2 + D_3 + D_4}$
(100% of full scale, count ⩾ 2000)

SIGN – Sign of Analog Input Polarity. This TTL level output is a static signal which is either 0 or V_{SS} for a negative or positive input polarity respectively.

GND – Digital Processor Ground. Should be kept separate from Analog Grounds. Common connection should be made at the power supply.

FUNCTIONAL OPERATION

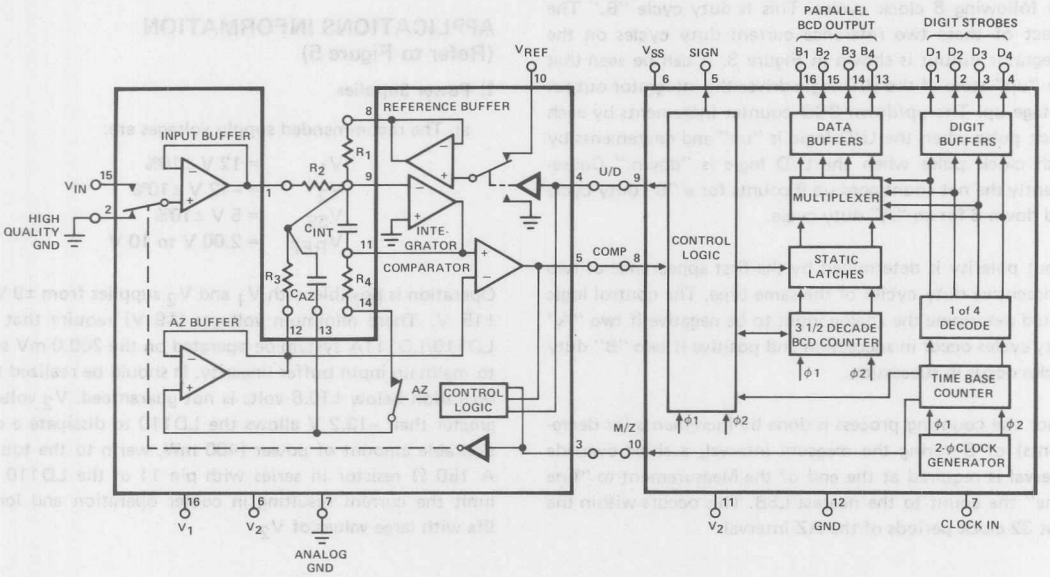
The Connection Diagram of Figure 1 should be referred to along with the timing diagrams of Figures 2, 3, and 4 in this discussion of functional operation.

Time Base Counter: An external clock signal using either TTL or MOS logic levels drives a 2-ϕ clock generator on the synchronous digital chip. The clock frequency is divided by the time base counter into sampling intervals of 6144 pulses of which 4096 constitute the measurement interval/and 2048 the auto-zero interval. Intermediate frequency divisions are utilized by both the control logic and the 1 of 4 decoder for the digit enables and bit scan.

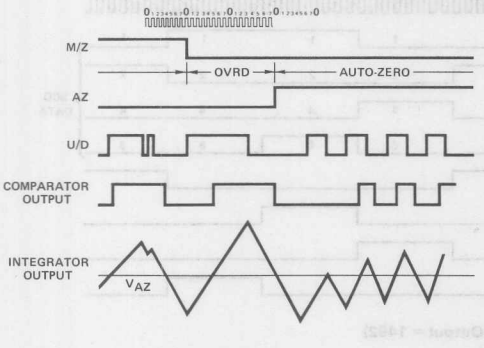
AUTO-ZERO INTERVAL

The Auto-Zero interval provides a means to null out the offset voltages of the amplifiers used in the LD110/LD111A system. In addition, it automatically establishes a second tracking reference voltage necessary for bipolar A/D conversion.

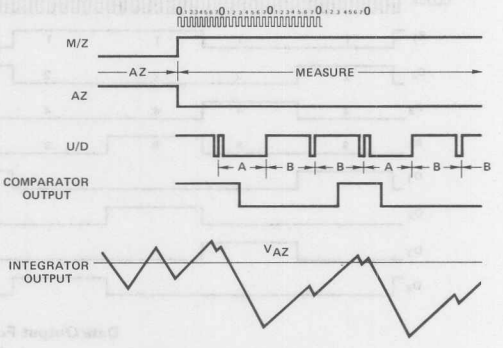
The Auto-Zero sequence is initiated when the M/Z (Measure/Zero) signal switches the input buffer amp to analog ground. After a brief count-correcting override period, the AZ switch is closed connecting the AZ amplifier and Integrator together in a closed-loop second-order system. During this time the control logic ignores the comparator output and pulses the U/D switch at a 50% duty cycle of 4 clock periods "Up" and 4 "Down" (see Figure 2). Equilibrium of this closed-loop system is attained when the average currents through R_1 and R_3 are equal and opposite. This is achieved when V_{AZ}, the Auto-Zero voltage, is equal to $-\frac{1}{2} V_{REF}$ ($R_1 = R_3$). Establishing V_{AZ} and storing it on C_{AZ} gives the U/D logic the capability of switching either a + or – reference current to the integrator during conversion. Thus when U/D is "Up," $I_1 + I_3 = -V_{REF}/2R_1$ and when U/D is "Down," $I_1 + I_3 = V_{REF}/2R_1$. The Auto-Zero interval is of sufficient duration to insure that V_{AZ} will be well established.



Connection Diagram
Figure 1



Auto-Zero Timing
Figure 2



Measure Interval Timing
Figure 3

FUNCTIONAL OPERATION (Cont'd)

MEASUREMENT INTERVAL

The "Quantized Feedback" conversion system is characterized by a single phase Digitization interval in which a digital control system feeds back quantized units of charge in response to the sampled state of an analog comparator. These quanta of charge balance the charge being supplied to the integrator by the analog voltage. The magnitude ($V_{REF}/2R_1 \times 6/f_{clock}$) of the Quantized charge being fed back and its sign (+ or –) arise from the fact that the control logic has two U/D duty cycles available during the Measure interval as shown in Figure 3.

The U/D logic is "up" one clock cycle and "down" 7 cycles for a high comparator output in the clock cycle preceding a set of 8 cycles. This will be designated duty cycle "A." With a low comparator output in clock cycle number 7 the U/D logic will be "up" for 7 cycles and "down" for 1 cycle in the following 8 clock cycles. This is duty cycle "B." The effect of these two reference current duty cycles on the integrator output is shown in Figure 3. It can be seen that the "up" state of the U/D logic drives the integrator output voltage up. The up/down BCD counter increments by each clock pulse when the U/D logic is "up" and decrements by each clock pulse when the U/D logic is "down." Consequently the net count goes up 6 counts for a "B" duty cycle and down 6 for an "A" duty cycle.

Input polarity is determined by the first appearance of two consecutive duty cycles of the same type. The control logic would determine the analog input to be negative if two "A" duty cycles occur in succession and positive if two "B" duty cycles occur in succession.

Since the counting process is done by increments (or decrements) of 6 during the measure interval, a short override interval is required at the end of the Measurement to "fine tune" the count to the nearest LSB. This occurs within the first 32 clock periods of the AZ interval.

DATA FLOW

Following the count correcting override sequence; the contents of the BCD counters and sign flip-flop are loaded into the internal latches. Counter states of less than 100 or greater than 1999 are decoded as underrange or overrange conditions respectively. The underrange signal is forced on Bit 4 during D_4 time. The overrange signal will be used to blank the display during the zero interval giving a visual overrange cue by means of a blinking display.

The BCD data stored in the latches is continuously scanned every 32 clock periods (8 clock times per digit). This data format is shown in Figure 4. Sign information is available as a static signal on a separate pin (high for +, low for –).

The BCD data output is an interlaced scan of digits 1, 3, 2, and 4 where digit 4 is the most significant digit. All outputs are active high and TTL compatible.

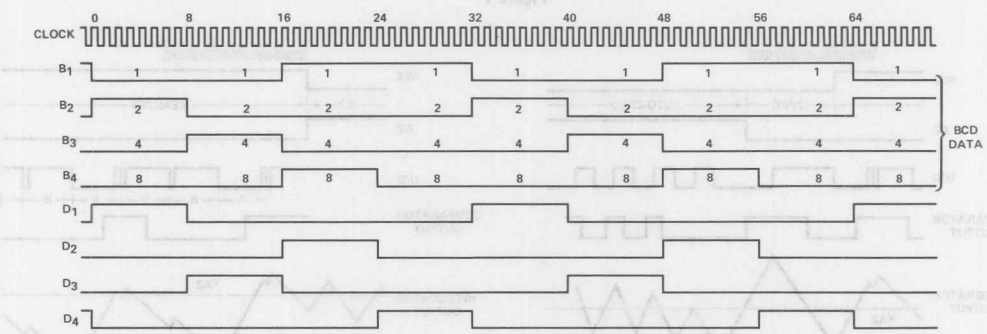
APPLICATIONS INFORMATION (Refer to Figure 5)

1. Power Supplies

a) The recommended supply voltages are:

V_1	= 12 V ±10%
V_2	= –12 V ±10%
V_{SS}	= 5 V ±10%
V_{REF}	= 2.00 V to 10 V

Operation is possible with V_1 and V_2 supplies from ±9 V to ±15 V. These minimum voltages (±9 V) require that the LD110/LD111A system be operated on the 200.0 mV scale to maintain input buffer linearity. It should be realized that operation below ±10.8 volts is not guaranteed. V_2 voltages greater than –13.2 V allows the LD110 to dissipate a considerable amount of power (400 mW, warm to the touch). A 150 Ω resistor in series with pin 11 of the LD110 will limit the current resulting in cooler operation and longer life with large values of V_2.



Data Output Format (Output = 1492)
Figure 4

APPLICATIONS INFORMATION (Cont'd)

2. Input Protection. Under normal operating conditions the inputs of the LD111A should not be exposed to a voltage exceeding either V_1 or V_2 (see absolute maximum ratings). In many applications however, such as a DMM/DVM, the V_{IN} or V_{REF} input may have a high voltage source connected which is capable of supplying destructive currents into the LD111A. To prevent such an occurrence, a current limiting resistor should be placed in series with the appropriate input pin. The 1 mA maximum current rating should be observed. A 1M Ω resistor in series with pin 15 of the LD111A would offer input protection up to a 1000 V overvoltage.

3. Operation Over the Full Sampling Range. Any sampling rate from 1/3 to 40 samples/second can be accommodated by simply changing the values for C_{INT} and C_{AZ} (R_3 and R_4 will remain as shown in Figure 5).

To find the proper value for C_{INT} and C_{AZ}, (shown as C_1 and C_2 respectively on Figure 5) find the needed clock frequency for a specific sampling rate from the following relationship.

$$f_{clock} = \text{Sampling Rate} \times 6144$$

Once the clock frequency has been determined, the values for C_{INT} and C_{AZ} can be found.

$$C_{INT} \cong \frac{200\ \mu F/sec}{f_{clock}}$$

$$C_{AZ} \cong 10\ C_{INT}$$

4. Resistor Selection. Resistor R_2 is the scaling resistor and is selected to provide 10 nA per LSB into the integrator summing junction. Thus,

$$R_2 = \frac{V_{IN(Full\ Scale)}}{(2000\ Counts)\ (10\ nA/Count)}$$

$$= 100K\ \Omega\ (2.000\ V\ Scale)$$

$$= 10K\ \Omega\ (200.0\ mV\ Scale)$$

$$= 1K\ \Omega\ (20.00\ mV\ Scale)$$

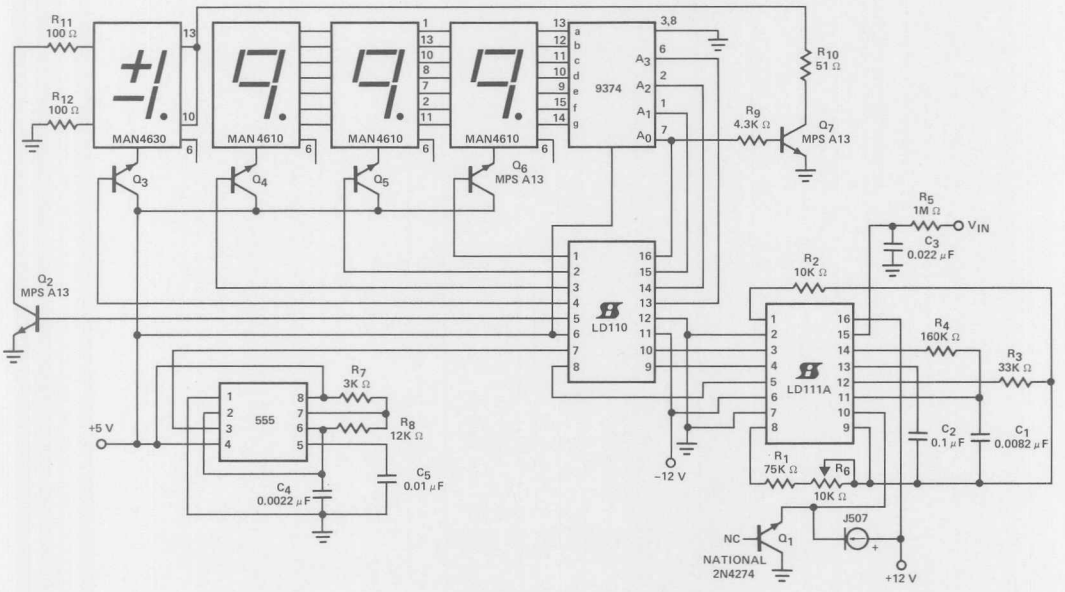
The reference resistor R_1 is chosen to satisfy the relationship

$$R_1\ (\text{Trimmed}) = \frac{V_{REF}}{81.92\ V}\ M\Omega$$

5. 20.00 mV Scale (10 μV Resolution). The improved noise performance of the LD111A allows it to be used in a 20.00 mV DPM when R_2 is selected to be 1K Ω. This high resolution range, while useful, does not have the same degree of zero and LSD stability as the 200.0 mV and 2.000 V ranges. Extreme care in layout is required to minimize noise and offsets at V_{IN} and Hi-Q GND.

6. Ratio Operation. The LD110/LD111A is a ratio measuring system — the output being

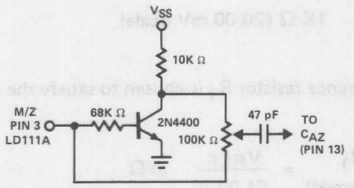
$$\text{Count} = \frac{V_{IN}}{V_{REF}}\ \frac{R_1}{R_2}\ 8192$$



3½ Digit DVM (±200.0 mV) Common Anode Display
Figure 5

loading. The ratio curve shown with the typical characteristics illustrates the ratio performance.

7. Zero Adjustment. The LD110/LD111A converter set is an Auto-zeroing system. Many applications exist, however, in which a means of nulling out external offsets is needed. The circuit of Figure 6 provides this offset nulling feature.

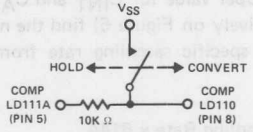


Offset Nulling Circuit
Figure 6

8. Replacing the LD111 with the LD111A. The LD111A offers a significant improvement in linearity, noise and temperature stability over the LD111. It also eliminates the need for the integrator clamp zener required on the LD111. The LD111A is a plug-in replacement for the LD111.

the override interval. The 3½ digits of data are then repeatedly multiplexed out during the rest of the zero and for the full Measure Interval. Since the data cannot change during the Measure Interval and since the Measure Interval occurs once each sampling interval, this high state of the M/Z line can be used as a Data Valid or End-of-Conversion signal.

10. "Hold". The last conversion of the LD110/LD111A may be held indefinitely by means of the added circuitry shown in Figure 7. Forcing the comparator input of the LD110 to the high state eliminates any future data transfers. The resistor protects the LD111A comparator output. Opening the connection to V_{SS} allows normal comparator action and data transfer. The first conversion after a "hold" will always be in error since the AZ voltage has not been maintained during "hold".



"Hold" Circuit
Figure 7

Siliconix

Function/Application of the LD110/LD111 3½ Digit A/D Converter Set

Replace LD111 with LD111A for New Designs

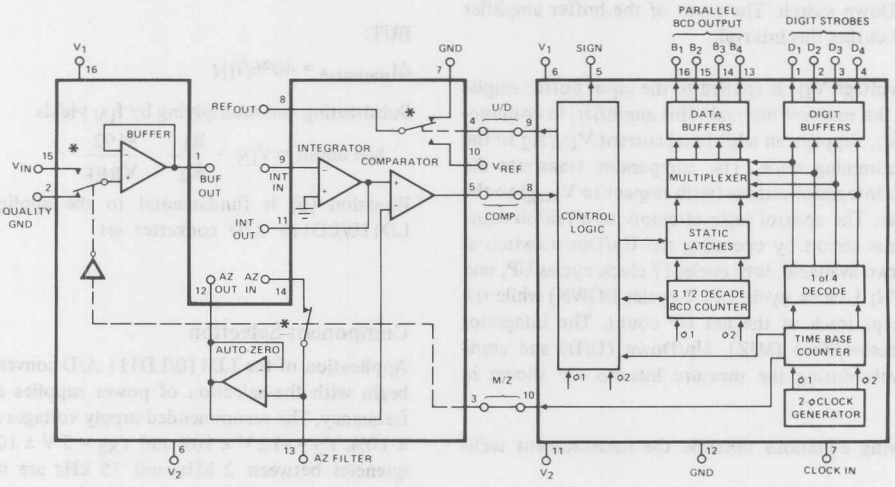
INTRODUCTION

The Siliconix LD110/LD111 3½-digit A/D converter integrated circuit set offers high performance and versatility with a minimum of required external circuitry. The set consists of a monolithic PMOS synchronous digital processor (LD110) and a monolithic bipolar-PMOS analog processor (LD111). The salient features of the A/D converter set include an accuracy of 0.05% (of reading) ±1 count; a 4 pA typical input bias current; an input impedance of greater than 1,000 MΩ; autozeroing; and a single reference voltage requirement. External user-selected components will allow for two different voltage ranges (2.000 V and 200.0 mV) and a wide range of sampling rates (1/3 to 12 samples per second) to accomodate a variety of applications.

This Application Note describes the functional operation of the LD110/LD111 A/D converter chip set, provides a basis for criteria in external component selection, and offers some practical circuit applications.

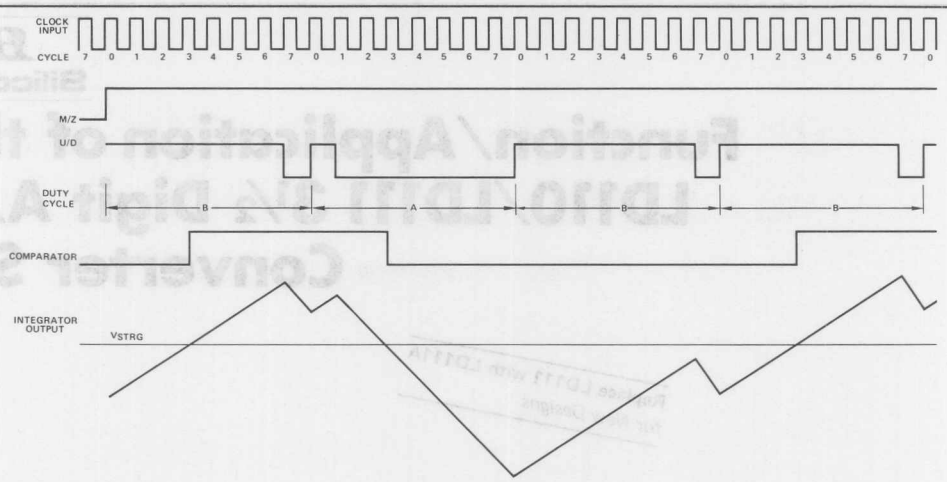
Functional Operation

The conversion technique balances the charge supplied by a current proportional to the input voltage, over a measure interval, with an accumulation of quantized charges equal to a BCD count. The units of quantized charge are provided through pulsewidth modulation of a reference current. In Figure 1, the A/D converter set is shown with the external RC components required to analyze the functional operation.



* P-channel Enhancement Mode MOS-FET Switches
U/D Shown in Down State (logic "0") M/Z in Zero State (logic "0")

Functional Diagram
Figure 1



Measure Interval Timing
Figure 2

The clock frequency is divided by the time-base counter of the LD110 digital processor into sampling intervals of 6144 cycles; 4096 cycles constitute the measurement interval and 2048 cycles make up the auto-zero interval.

The auto-zero interval allows the effects of offset, temperatures and drift to be impressed on the auto-zero storage voltage, V_{strg}, which is maintained as a reference by C_{strg}. Therefore, during the succeeding measure interval these effects will be balanced out. In addition, V_{strg} acquires a voltage component available at the AZ amplifier output, which provides a current equal to $-\frac{1}{2} V_{REF}/R_1$ through resistor R_3. The net current provided to the integrator summing node by the sum of V_{strg}/R_3 and the current through R_1 is either + or –. $V_{REF}/2R_1$, depending on the position of the Up/Down switch. The input of the buffer amplifier is grounded during this interval.

The input voltage V_{IN} is applied to the input buffer amplifier during the measure interval. This amplifier, in conjunction with R_2, supplies an additional current V_{IN}/R_2 to the integrator summing node. The comparator transmits the state of the integrator output (with respect to V_{strg}) to the control logic. The control logic attempts to establish equilibrium in the circuit by operating the Up/Down switch at one of the two available duty cycles (7 clock cycles UP, one cycle DOWN; 1 clock cycle UP, 7 cycles DOWN) while the counter keeps track of the net UP count. The integrator output, Measure/Zero (M/Z), Up/Down (U/D) and comparator levels during the measure interval are shown in Figure 2.

The following equations describe the measurement technique:

$$\Delta Q = 0$$

WHERE:

$$\Delta Q = \frac{V_{IN}}{R_2}\,\Delta t_{measure} - \frac{V_{REF}}{2R_1 f_{IN}}\,(N_U) \quad \frac{+V_{REF}}{2R_1 f_{IN}}\,(N_D) \quad (1)$$

WHERE:

(N_U) = (# counts UP) and
(N_D) = (# counts DOWN)

BUT:

counts UP + # counts DOWN = 4096 (clock cycles in the measure interval) (2)

counts UP – # counts DOWN = net count (3)

THEN:

$$0 = \frac{V_{IN}}{R_2}\,\Delta t_{measure} - \frac{V_{REF}}{2R_1 f_{IN}}\ (\text{net count}) \quad (4)$$

BUT:

$$\Delta t_{measure} = 4096/f_{IN} \quad (5)$$

Substituting and multiplying by f_{IN} yields

$$\text{Net count} = V_{IN} \cdot \frac{R_1}{R_2} \cdot \frac{8192}{V_{REF}} \quad (6)$$

Equation (6) is fundamental to the application of the LD110/LD111 A/D converter set.

Component Selection

Application of the LD110/LD111 A/D converter set should begin with the selection of power supplies and the clock frequency. The recommended supply voltages are V_1 = 12 V ± 10%, V_2 = -12 V ± 10% and V_{SS} = 5 V ± 10%. Clock frequencies between 2 kHz and 75 kHz are recommended. The duty cycle of the clock is not of particular importance; the logic "0" time should however, be greater than 5 μsec. The sampling rate and clock frequency are related as follows:

$$\text{Sampling Rate} = f_{IN}/6144 \quad (7)$$

The clock frequency may be chosen to minimize line frequency interference. If the auto-zero and measurement periods are integral multiples of the line frequency (f_L) period, line frequency rejection will be maximized:

$$\Delta t_{ZERO} = 2048/f_{IN} \; (\Delta t_{measure} = 2\,\Delta t_{zero}) \qquad (8)$$

$$\frac{2048}{f_{IN}} = \frac{n}{f_L}, \text{ where } n = 1, 2, 3, \ldots 51 \qquad (9)$$

THEN:

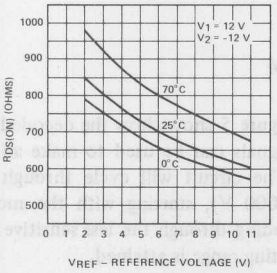
$$f_{IN} = \frac{2048\, f_L}{n} \qquad (10)$$

Once the clock frequency is chosen, the proper values for the external RC components may be determined.

Equation (6) defines the relationship between the ratio R_1/R_2 and the reference voltage V_{REF} when a full-scale voltage range V_{IN} (F.S.) is chosen. This relationship is:

$$\frac{R_2}{R_1} = \frac{V_{IN}\,(F.S.)}{2000} \quad \frac{8192}{V_{REF}} \qquad (11)$$

It is usually more convenient to select V_{REF} before assigning resistance values because of the implications of temperature coefficients, availability, or other considerations. V_{REF} should be greater than 5 V, but less than V_1. As V_{REF} is increased the U/D switch ON resistance decreases, as is shown in Figure 3. R_1 also increases with V_{REF}, thus decreasing the proportion of the total resistance provided by $r_{DS(ON)}$. Consequently, a large V_{REF} minimizes the effects of the U/D switch ON resistance. It is very important that V_{REF} have a low temperature coefficient to minimize drift and the resulting count error.



$R_{DS(ON)}$ (U/D Switch) vs. V_{REF} and Temperature
Figure 3

Equation (12) shows the change in count which will occur for a fractional change in V_{REF} (see Appendix A, Page 10)

$$\Delta count = -2000 \; \frac{V_{IN}}{V_{IN}\,(F.S.)} \; \frac{\Delta V_{REF}}{V_{REF}} \qquad (12)$$

Consequently, the count will decrease by 1 for each +0.05% change in V_{REF}, for $V_{IN} = V_{IN}$ (F.S.)

R_2 should be chosen to supply a full scale current of 20 μA into the integrator summing node (100 KΩ for 2.000 V and 10 KΩ for 200.0 mV). R_1 can then be determined by Equation (11). R_1, R_2 and V_{REF} and the basic temperature-sensitive components of the system. The auto-zero interval makes the system essentially independent of changes in C_{INT}, R_3, R_4, R_5, C_{strg} and the offset voltages of the amplifiers. In Figure 3, note that the U/D switch ON resistance has a temperature coefficient of about 0.2/°C. This temperature-dependent resistance must be considered as a part of R_1, the reference resistor. The error in count resulting from a change in this total resistance R_1 is examined in Appendix B (Page 10) and found to be:

$$\Delta Count = 2000 \; \frac{V_{IN}}{V_{IN}\,(F.S.)} \; \frac{\Delta R_1}{R_1} \qquad (13)$$

Since the count is proportional to the ratio R_1/R_2, equal temperature coefficients for these resistors should allow this ratio (and the count) to be maintained even with a change in the ambient temperature. It is desireable, however, to use resistors with low temperature coeffients for R_1 and R_2 to reduce any errors resulting from the differences in these coefficients.

The net error that can be attributed to temperature effects is the sum of the errors due to the changes in V_{REF} and the $R_{DS(ON)}$ of the U/D switch. Temperature compensation for the A/D converter circuit, then, can be approached in two different ways. The first method would be to provide a large V_{REF} (less than V_1, however) with a very low temperature coefficient. This would require a large value of resistance for R_1, reduce $R_{DS(ON)}$ and make changes in $R_{DS(ON)}$ negligible. The alternative method is to note that a reference voltage with a positive temperature coefficient produces an error in the count which tends to oppose the error caused by the positive temperature coefficient of $R_{DS(ON)}$. Thus the two effects can be used to counteract one another (an example is provided in Appendices A and B).

The specified accuracy of the A/D converter will be maintained if the integrator capacitor C_{INT} is chosen so that the voltage swing of the integrator is held to within 0.75 volt of V_{strg}. An analysis of this constraint, shown in Appendix C, (Page 11) results in the following relationship for C_{INT}:

$$C_{INT} = \frac{28.5\; V_{IN}\,(F.S.)}{R_2 f_{IN}} \qquad (14)$$

This capacitor and the zener diode to be placed in parallel with it should have a combined leakage of less than 10 nA (see Appendix D, Page 11) to minimize this possible source of error.

The storage voltage, V_{strg}, should be maintained between -2 V and -5 V for normal operation. The ON resistance of

the auto-zero (AZ) switch is typically 11 KΩ at V_{strg} = tive than -9 V to maintain the functionality of the analog processor. This can be accomplished by placing back-to-back Zener diodes in parallel with C_{INT} (the second diode is to prevent the Zener from being forward biased). It then becomes important that the integrator output voltage not exceed the breakdown voltage of the Zener diodes, for the maximum input voltage for which an accurate readout is desired. The relevant equations are:

$$V_{o(min)} > -V_{zener} \quad (15)$$

WHERE:

$$V_{o(min)} = V_{strg} - \frac{7}{f_{IN}C_{INT}}\left[\frac{V_{REF}}{2R_1} + \frac{V_{IN(max)}}{R_2}\right] \quad (16)$$

(see Appendix C)

$$V_{strg} = \frac{-V_{REF}}{2}\frac{R_3}{R_1} - \frac{R_3}{R_2}V_{Hi\text{-}Q} \text{ (If Hi-Q Gnd} \quad (17)$$

is not at zero potential)

If $V_{o(min)}$ exceeds the breakdown voltage value of the selected Zener diodes, either V_{strg} or C_{INT} must be adjusted to maintain this inequality (see Equation (15)).

A number of engineering tradeoff considerations must be made in selecting RC components for the A/Z filter (R_4, R_5 and C_{strg}). Some of these are covered in Appendix E. Various component values for different clock frequency ranges are presented in Table I, along with the recommended values for the integrator capacitor, C_{INT}.

TABLE I

Auto/Zero Filter Values

f_{IN} (kHz)	C_{INT} (μF)	C_{strg} (μF)	R_4 (KΩ)	R_5 (KΩ)
2 to 10	0.1	1.0	68	15
10 to 20	0.039	0.056	240	47
20 to 40	0.022	0.056	120	33
40 tu 75	0.01	0.056	82	18

APPLICATIONS

Digital Voltmeters

The circuits shown in Figure 4 present the LD110/LD111 A/D converter set in typical ±2.000 V digital voltmeter applications. The clock frequency of 24.5 kHz provides a sampling rate of 5 samples per second. Trimmer resistor R_6 calibrates the DVM. R_1 and R_2 are metal film resistors. The illustrated connection of the analog circuit grounds

The use of a seven-segment LED for Digit 4 will allow the DVM to be employed up to the maximum count of 3100. The output of the BCD-to-seven-segment decoder will be erroneous during Digit 4 time, however, because underrange information is encoded on bit 4 during Digit 4 time. The bit 4 input of the decoder in Figure 4a (bit 4 is the most significant bit) should be clamped to ground during Digit 4 time to provide the correct Digit 4 readout, as in:

$$\text{Input D of decoder} = B_4 \cdot \overline{D_4} \quad (18)$$

where B_n is the nth BCD data bit and D_n is the nth digit.

The display will blink at a rate equal to the sampling rate when the count exceeds 1999. If the grounding system is poor, erroneous readings will result for counts of 2000 and above.

The data output format is an interlaced scan of Digits, 1, 3, 2 and 4 with Digit 4 as the most significant digit. This permits the use of Sperry displays with clock frequencies of 25 kHz or less. All outputs are active high and TTL-compatible.

The overrange and underrange signals may be obtained by external logic, i.e.,

$$\text{MUX Underrange} = B_4 \cdot D_4 \text{ (5\% of full scale)} \quad (19)$$

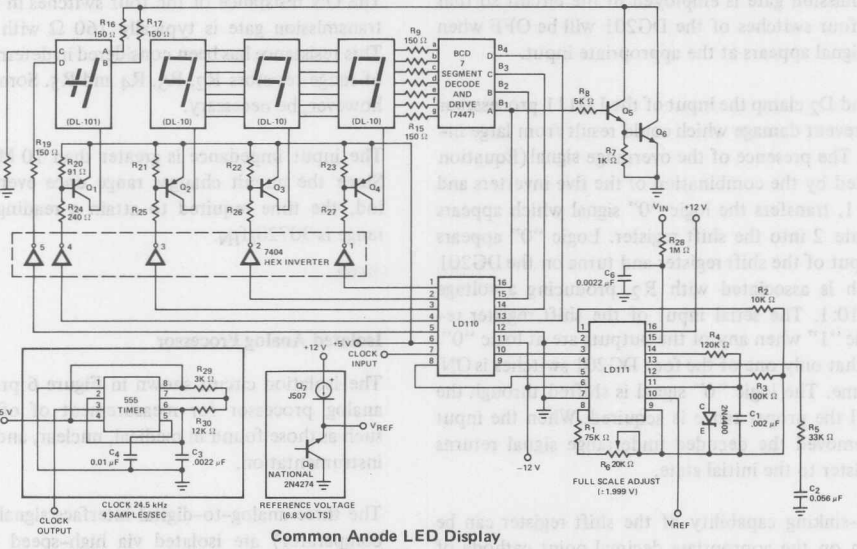
$$\text{MUX Overrange} = \overline{D_1 + D_2 + D_3 + D_4} \text{ (100\% of full scale)} \quad (20)$$

Autoranging DVM

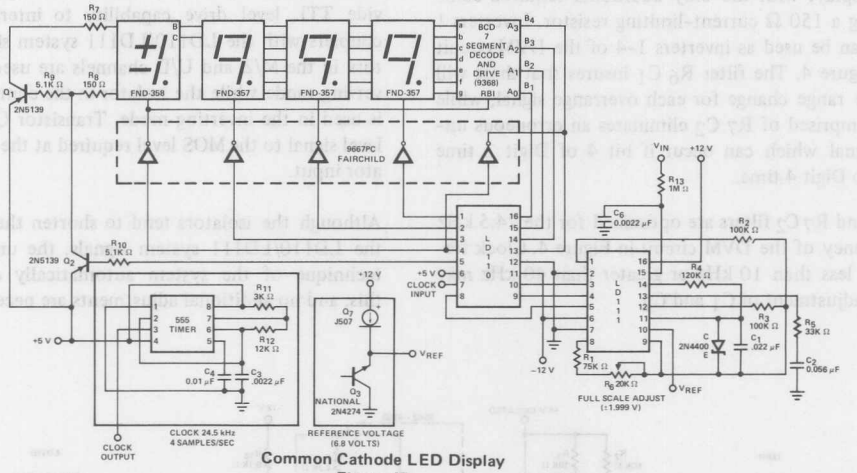
The circuit in Figure 5 shows how the decoded underrange and overrange signals can be used to make an automatic-ranging DVM. The circuit will cycle through five ranges (200 mV to 2,000 V), starting with the most sensitive range and proceeding through the less sensitive ranges until the proper operating range is attained.

When the cycle proceeds from the most sensitive to the least sensitive range, the proper range will be achieved for voltages which will provide a count between 1000 and 2000. If the cycle began at the least sensitive range, a voltage such as 15.0 V would be read on the 200 V range, since the count of 150 would not initiate an underrange signal to advance the circuit to a more sensitive range.

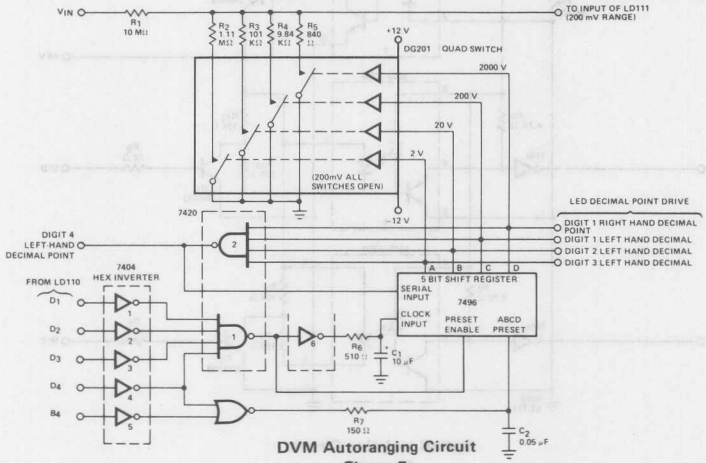
The two-input NOR gate decodes the underrange signal to preset the shift register with a "1" logic at each of the parallel bit outputs. A Siliconix DG201 quad SPST CMOS



Common Anode LED Display
Figure 4A



Common Cathode LED Display
Figure 4B



DVM Autoranging Circuit
Figure 5

analog transmission gate is employed in the circuit so that each of the four switches of the DG201 will be OFF when a logic "1" signal appears at the appropriate input.

Diodes D_1 and D_2 clamp the input of the LD111 processesor at ±5 V to prevent damage which could result from large input voltages. The presence of the overrange signal (Equation (20)), decoded by the combination of the five inverters and NAND gate 1, transfers the logic "0" signal which appears at NAND gate 2 into the shift register. Logic "0" appears at the A output of the shift register and turns on the DG201 switch which is associated with R_2, producing a voltage division of 10:1. The serial input of the shift register remains at logic "1" when any of the outputs are at logic "0", this insures that only one of the four DG201 switches is ON at a given time. The logic "0" signal is shifted through the register until the proper range is acquired. When the input voltage is removed the decoded underrange signal returns the shift register to the initial state.

The current-sinking capability of the shift register can be used to turn on the appropriate decimal point cathode of the LED display, with the only additional required component being a 150 Ω current-limiting resistor. Inverters 1 through 4 can be used as inverters 1-4 of the DVM circuit shown in Figure 4. The filter R_6 C_1 insures that there will be only one range change for each overrange signal, while the filter comprised of R_7 C_2 eliminates an erroneous underrange signal which can occur if bit 4 of Digit 2 time overlaps into Digit 4 time.

The R_6C_1 and R_7C_2 filters are optimized for the 24.5 kHz clock frequency of the DVM circuit in Figure 4. Clock frequencies of less than 10 kHz or greater than 40 kHz may require the adjustment of C_1 and C_2.

The ON resistance of the four switches in the DG201 quad transmission gate is typically 160 Ω with ±12 V supplies. This resistance has been considered in determining the values of range resistors R_2, R_3, R_4 and R_5. Some trimming may, however, be necessary.

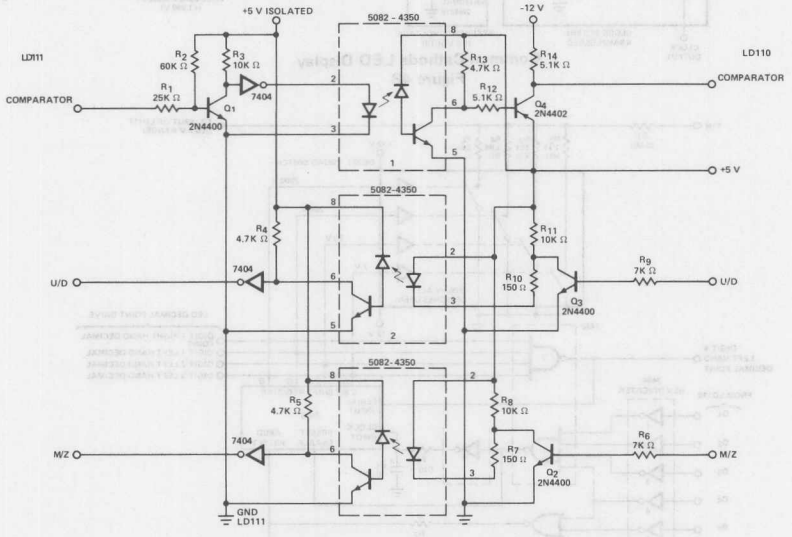
The input impedance is greater than 10 MΩ on all ranges. Since the circuit changes range once every sampling period, the time required to attain a reading on the highest range is $30720/f_{IN}$.

Isolated Analog Processor

The isolation circuit shown in Figure 6 provides a floating analog processor for measurement of off-ground signals such as those found in medical, nuclear, and process control instrumentation.

The three analog-to-digital interface signals (M/Z, U/D and comparator) are isolated via high-speed optical couplers with a 2,500 V insulation. Transistors Q_1, Q_2 and Q_3 provide TTL level drive capability to interface the optical couplers with the LD110/LD111 system signals. The isolators in the M/Z and U/D channels are used in the non-inverting mode while the isolator in the comparator interface is used in the inverting mode. Transistor Q_4 shift the TTL level signal to the MOS level required at the LD110 comparator input.

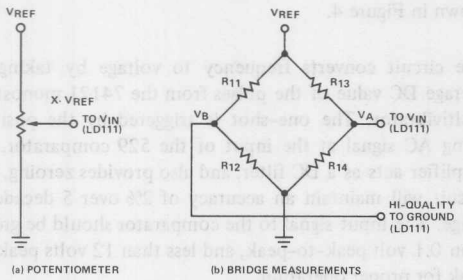
Although the isolators tend to shorten the pulse length of the LD110/LD111 system signals, the unique conversion technique of the system automatically compensates for this, and no additional adjustments are necessary.



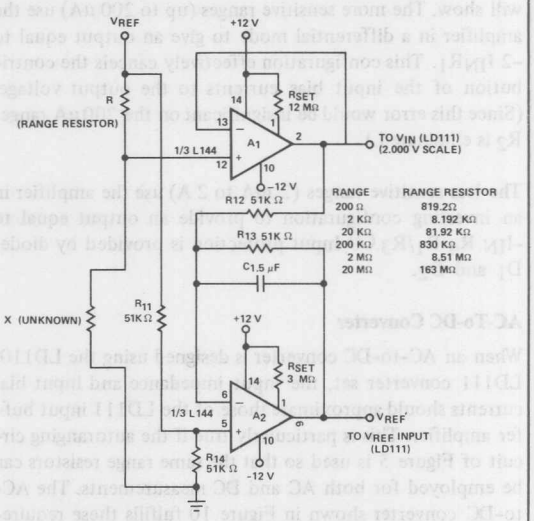
Optical Isolation Circuit
Figure 6

Ratio Measurements

Equation (6) shows that the LD110/LD111 A/D converter measures input voltage as a ratio: the count is proportional to the ratio of the input voltage and the reference voltage. This system conversion technique is ideally suited to the measurement of ratio. Ratio measurements using a reference voltage which is also the excitation voltage of the ratio device allows measurements to be independent of variations in the excitation voltage. Typical ratio-measuring circuits are shown.



Ratio Measurements
Figure 7



Resistance To Voltage Converter
Figure 8

The output of the potentiometer in Figure 7A (which can represent position, level, etc.) can be substituted in Equation (6) to demonstrate this capability:

$$\text{Count} = XV_{REF} \cdot \frac{R_1}{R_2} \cdot \frac{8192}{V_{REF}} = \frac{R_1}{R_2} \cdot 8192X \qquad (21)$$

Bridge transducer measurements, as shown in Figure 7B, can also be normalized to an external reference. The Hi-Q ground input of the LD111 functions as the inverting input of a difference amplifier to provide a count proportional to the difference of the two input voltages V_A and V_B.

$$\text{Count} = \frac{R_1}{R_2} \frac{8192}{V_{REF}} (V_A - V_B)$$

$$= \frac{R_1}{R_2} 8192 \left(\frac{R_{14}}{R_{13} + R_{14}} - \frac{R_{12}}{R_{11} + R_{12}} \right) \qquad (22)$$

Ratio measurement techniques can also be extended to resistance measurement. The resistance-measuring circuit shown in Figure 8 will measure accurately to 20 MΩ when associated with a buffer amplifier (A_1) having a low input bias current ($I_{IN} < 30$ nA). The circuit illustrated uses two of the three amplifiers contained in the Siliconix L144 micropower triple op amp.

This circuit exhibits a very high reference voltage rejection ratio, as shown by the following pertinent equations. (1)

$$V_{IN} = V_{REF} \left(\frac{X}{R + X} \right) \qquad (23)$$

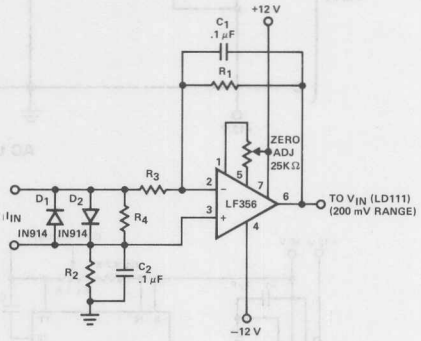
$$V_{REF}' = V_{REF} \left[1 - \frac{X}{R + X} \right] \frac{R_{14}}{R_{11}} \qquad (24)$$

Substituting into Equation (6) yields

$$\text{Count} = 8192 \frac{X}{R} \cdot \frac{R_{11}}{R_{14}} \cdot \frac{R_1}{R_2} \qquad (25)$$

Current-To-Voltage Converter

A current-to-voltage converter featuring eight decades of current range is shown in Figure 9. The circuit is intended to be used with the 200.0 mV range of the DVM.



CURRENT RANGE	R1	R2	R3	R4
200 nA	500 KΩ	500 KΩ	0	∞
2 μA	50 KΩ	50 KΩ	0	∞
20 μA	5 KΩ	5 KΩ	0	∞
200 μA	1 KΩ	0	0	∞
2 mA	50 KΩ	0	5.0 K	10.0 Ω
20 mA	50 KΩ	0	5.0 K	1.0 Ω
200 mA	50 KΩ	0	5.0 K	.1 Ω
2 A	50 KΩ	0	5.0 K	.01Ω

Current To Voltage Converter
Figure 9

The arrangement actually comprises two different circuits, as examination of the table of resistance values in Figure 9 will show. The more sensitive ranges (up to 200 μA) use the amplifier in a differential mode to give an output equal to $-2\ I_{IN}R_1$. This configuration effectively cancels the contribution of the input bias currents to the output voltage. (Since this error would be insignificant on the 200μA range. R_2 is eliminated.)

The less sensitive ranges (2 mA to 2 A) use the amplifier in an inverting configuration to provide an output equal to $-I_{IN}\ R_4\ R_1/R_3$.(2) Input protection is provided by diodes D_1 and D_2.

AC-To-DC Converter

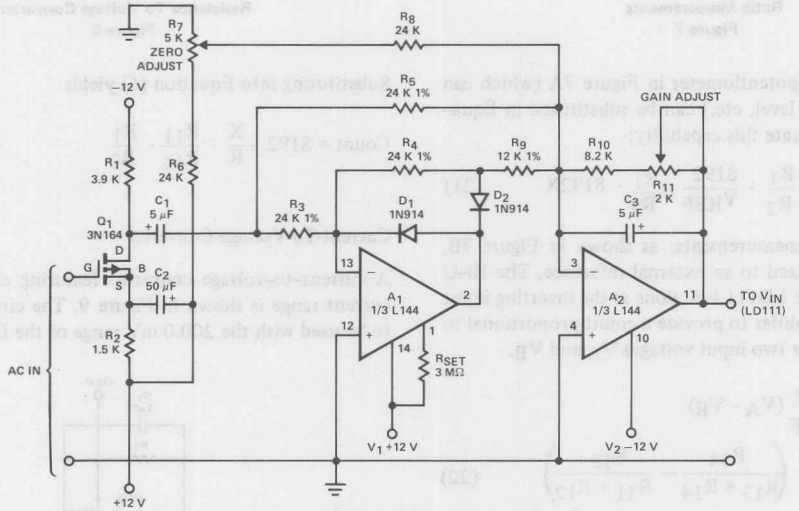
When an AC-to-DC converter is designed using the LD110/LD111 converter set, the input impedance and input bias currents should approximate those of the LD111 input buffer amplifier. This is particularly true if the autoranging circuit of Figure 5 is used so that the same range resistors can be employed for both AC and DC measurements. The AC-to-DC converter shown in Figure 10 fulfills these requirements. The circuit includes a PMOS enhancement-mode FET input buffer amplifier, coupled to a classical absolute value circuit which essentially eliminates the effect of the forward voltage drop across diodes D_1 and D_2.

A filter removes the DC component of the rectified AC, which is then scaled to RMS. The output is linear from 40 Hz to 10 kHz or higher.

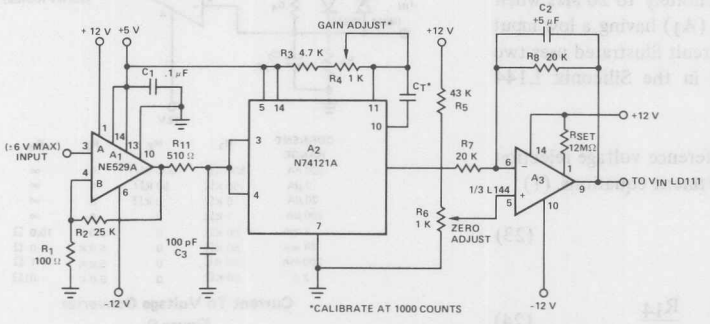
Digital Frequency Meter

A digital frequency meter can be fashioned by using the circuit shown in Figure 11 with the basic 2-volt DVM circuit shown in Figure 4.

The circuit converts frequency to voltage by taking the average DC value of the pulses from the 74121 monostable multivibrator. The one-shot is triggered by the positive-going AC signal at the input of the 529 comparator. The amplifier acts as a DC filter, and also provides zeroing. This circuit will maintain an accuracy of 2% over 5 decades of range. The input signal to the comparator should be greater than 0.1 volt peak-to-peak, and less than 12 volts peak-to-peak for proper operation.



AC to DC Converter
Figure 10

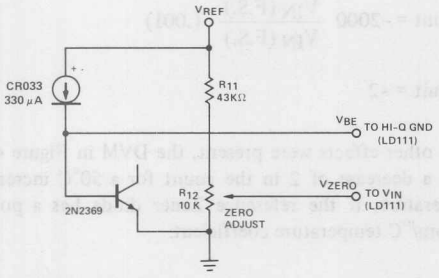


RANGE	C_T
2 kHz	.082 µF
20 kHz	.0082 µF
200 kHz	820 pF
2 MHz	82 pF
20 MHz	8.2 pF

Frequency To Voltage Converter
Figure 11

Digital Thermometer

A digital thermometer can be constructed by using the change in forward voltage drop across a PN junction as the temperature-sensitive element in the circuit. This change is typically -2.3 mV/°C. The circuit shown in Figure 12 has the base-emitter junction of a bipolar transistor biased with a 470 μA current source.



TEMPERATURE SENSOR

NOTE:
THE DVM SHOWN IN FIGURE 4 MUST BE CHANGED IN THE FOLLOWING WAYS FOR THIS APPLICATION

1. R_3 = 51 KΩ
2. R_2 = 23 KΩ (CENTIGRADE SCALE)
 11 KΩ (FARENHEIT SCALE)
3. HI-QUALITY GND NO LONGER CONNECTED TO GROUND

Temperature To Voltage Converter
Figure 12

The junction voltage V_{BE} is applied to the input buffer amplifier of the analog processor which functions as a differential amplifier. The buffer resistor R_2 is scaled to give a count proportional to temperature as shown by the following equations:

$$\text{Count} = \frac{R_1}{R_2}\,\frac{8192}{V_{REF}}\left[V_{ZERO} - V_{BE}(T)\right] \qquad (26)$$

AND SO:

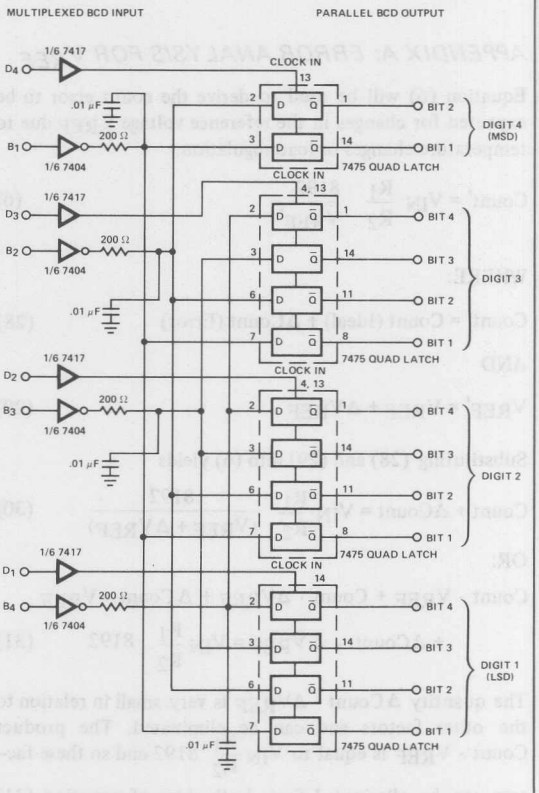
$$\text{Count} = 1000\,A\left[V_{ZERO} - V_{BE}(T)\right] \qquad (27)$$

Gain A must be approximately 5 for the Centigrade scale and 9 for the Farenheit scale.

Multiplexed BCD To Parallel BCD Converter

Although the multiplexed BCD output of the LD110/LD111 A/D converter set is useful for digital displays, there are applications (such as printer inputs) in which the BCD data for all four digits should be available in a parallel format. The multiplexed BCD-to-parallel-BCD converter shown in Figure 13 will provide the proper interface for such applications.

The converter consists of 4 quad bistable latches activated in the proper sequence by the digit strobe output of the LD110. The complemented outputs ($\overline{Q}$) of the quad latch set will reflect the state of the bit outputs when the digit strobe goes high, and will maintain this state when the digit strobe goes low. The latches will be updated with the next digit strobe. This parallel BCD output will not then be affected by the blinking-off of the digit strobes when the count exceeds 1999 (overrange), and can be used to drive a non-blinking display up to a full scale ot 3000 counts. The parallel BCD output can be put in a "hold" state by lamping all digit strobes to ground to prevent the uplating of the latches.



Multiplexed BCD To Parallel BCD Converter
Figure 13

CONCLUSIONS

The LD110/LD111 A/D converter integrated circuit set lends itself to a wide range of applications in which analog information is desired in digital format. High accuracy and long term stability combined with a minimum of external circuitry and calibration requirements make this converter set a superior choice for any application. The circuit examples presented are intended to be of general interest, and do not touch upon the wide variety of more specialized applications.

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(1) R. Milner, *"Integrate with a DMM?"*, Electronic Design, October 25, 1973, pp. 93-96.

(2) M.K. Vander Kooi, *"Simple IC Meter Amplifier Circuit Measure 100 Nanoamps Full-Scale"*, ED/EEE, April 15, 1972, pp. 40-41.

(3) J. D'Azzo and C. Houpis, Feedback Control System Analysis and Synthesis, McGraw-Hill Co. New York, 1960, pp. 81-83.

APPENDIX A: ERROR ANALYSIS FOR V_{REF}

Equation (6) will be used to derive the count error to be expected for changes in the reference voltage V_{REF} due to temperature changes or load regulation.

$$\text{Count}' = V_{IN} \frac{R_1}{R_2} \frac{8192}{V_{REF}'} \quad (6)$$

WHERE:

$$\text{Count}' = \text{Count (Ideal)} + \Delta\text{Count (Error)} \quad (28)$$

AND

$$V_{REF}' = V_{REF} + \Delta V_{REF} \quad (29)$$

Substituting (28) and (29) into (6) yields

$$\text{Count} + \Delta\text{Count} = V_{IN} \frac{R_1}{R_2} \frac{8192}{(V_{REF} + \Delta V_{REF})} \quad (30)$$

OR:

$$\text{Count} \cdot V_{REF} + \text{Count} \cdot \Delta V_{REF} + \Delta\text{Count} \cdot V_{REF} + \Delta\text{Count} \cdot \Delta V_{REF} = V_{IN} \frac{R_1}{R_2} \; 8192 \quad (31)$$

The quantity $\Delta\text{Count} \cdot \Delta V_{REF}$ is very small in relation to the other factors and can be eliminated. The product $\text{Count} \cdot V_{REF}$ is equal to $V_{IN} \frac{R_1}{R_2} \; 8192$ and so these factors can be eliminated from both sides of equation (31) leaving

$$\text{Count} \cdot \Delta V_{REF} + \Delta\text{Count} \cdot V_{REF} = 0 \quad (32)$$

THEREFORE:

$$\Delta\text{Count} = -\text{Count} \frac{\Delta V_{REF}}{V_{REF}} \quad (33)$$

This can be related to V_{IN} by noting that the full-scale count is 2000, thus:

$$\Delta\text{Count} = -2000 \frac{V_{IN}}{V_{IN}\,(F.S.)} \frac{\Delta V_{REF}}{V_{REF}} \quad (34)$$

The reference supply shown in Figure 4 has a typical temperature coefficient of ±20 ppm/°C. Therefore the reference voltage would change by 0.1% for an increase in temperature of 50°C (20°C to 70°C). The maximum error will occur when V_{IN} equals the full scale voltage V_{IN} (F.S.) as shown below.

$$\Delta\text{Count} = -2000 \frac{V_{IN}\,(F.S.)}{V_{IN}\,(F.S.)} \; (.001) \quad (35)$$

$$\Delta\text{Count} = -2 \quad (36)$$

If no other effects were present, the DVM in Figure 4 will show a decrease of 2 in the count for a 50°C increase in temperature, if the reference Zener diode has a positive 20 ppm/°C temperature coefficient.

APPENDIX B: TEMPERATURE EFFECT OF $R_{DS(on)}$ (U/D SWITCH)

The analysis of the readout error caused by a change in the $R_{DS(on)}$ of the U/D switch will proceed along similar logic as that of Appendix A. Again we look at Equation (6).

$$\text{Count}' = V_{IN} \frac{R_1'}{R_2} \frac{8192}{V_{REF}} \quad (6)$$

WHERE

$$\text{Count}' = \text{Count (Ideal)} + \Delta\text{Count (Error)} \quad (28)$$

AND

$$R_1' = R_1\,(\text{Ideal}) + \Delta R_1 \quad (37)$$

Substituting (28) and (37) into (6) yields,

$$\text{Count} + \Delta\text{Count} = = V_{IN} \frac{R_1}{R_2} \frac{8192}{V_{REF}} + V_{IN} \frac{\Delta R_1}{R_2} \frac{8192}{V_{REF}} \quad (38)$$

Eliminating Equation (6) from (38) gives the change in count (Δ Count).

$$\Delta\text{Count} = V_{IN} \frac{\Delta R_1}{R_2} \frac{8192}{V_{REF}} \quad (39)$$

BUT:

$$V_{REF} = V_{IN} \frac{R_1}{R_2} \frac{8192}{Count} \quad (40)$$

so that by substituting (40) into (39) yields

$$\Delta Count = \frac{\Delta R_1}{R_1} \quad Count \quad (41)$$

or by relating the count to the input voltage V_{IN} we see that:

$$\Delta Count = 2000 \frac{V_{IN}}{V_{IN}(F.S.)} \frac{\Delta R_1}{R_1} \quad (42)$$

We can now examine how the temperature dependency of $R_{DS(on)}$ (U/D Switch) will affect the accuracy of the DVM application circuit of Figure 4. Using Figure 3, it can be seen that $R_{DS(on)}$ will increase by 100 Ω when the ambient temperature changes by about 50°C (V_{REF} = 6.8 volts). The maximum error ($V_{IN} = V_{IN}$ (F.S.)) will be:

$$\Delta Count = \frac{100\ \Omega}{83\ K\Omega} \quad 2000 = 2.41 \quad (43)$$

The net count error will then be due to the sum of the error associated with V_{REF} and the error due to the change is $R_{DS(ON)}$ which is:

$$Net\ Count\ Error = \Delta Count\ (V_{REF}) + \Delta Count\ (R_1) \quad (44)$$

$$Net\ Count\ Error = -2 + 2.41 = .41\ counts \quad (45)$$

If the reference resistor R_1 and the input resistor R_2 have the same temperature coefficients, the temperature effects of these resistors will be balanced out.

APPENDIX C: PROPER SELECTION OF THE INTEGRATOR CAPACITOR C_{INT}

In order to maintain good accuracy, the integrator output V_o should not be allowed to deviate from V_{strg} by more than 0.75 volts. The maximum deviation from V_{strg} will occur when the maximum input current $\frac{V_{IN}(F.S.)}{R_2}$ is of the same sense as the reference current. These considerations are shown in the following mathematical expressions:

$$|\Delta V_o| = \frac{1}{C_{INT}} \int_0^{7/f_{IN}} \left(\frac{V_{IN}(F.S.)}{R_2} + \frac{V_{REF}}{2R_1} \right) dt \quad (46)$$

SO

$$|\Delta V_o| = \frac{7}{C_{INT}\, f_{IN}} \left[\frac{V_{REF}}{2R_1} + \frac{V_{IN}(F.S.)}{R_2} \right] \quad (47)$$

BUT:

$$R_1 = \frac{2000\, V_{REF}\, R_2}{8192\, V_{IN}(F.S.)} \quad \text{See Eq. (6)} \quad (48)$$

Substituting (48) into (47) yields

$$|\Delta V_o| = \frac{7}{C_{INT}\, f_{IN}} \left[\frac{2.048\, V_{IN}(F.S.)}{R_2} + \frac{V_{IN}(F.S.)}{R_2} \right] \quad (49)$$

AND

$$|\Delta V_o| = \frac{21.336\, V_{IN}(F.S.)}{R_2\, C_{INT}\, f_{IN}} \quad (50)$$

Setting this absolute deviation equal to 0.75 volts gives

$$C_{INT} = \frac{28.45\, V_{IN}(F.S.)}{R_2\, f_{IN}} \quad (51)$$

For the application circuit of Figure 4:

$R_2 = 100\ K\Omega$

$f_{IN} = 24.5\ kHz$

$V_{IN}(F.S.) = 2.000$ volts

From equation (51) then:

$$C_{INT} = 0.0232\ \mu F \quad (52)$$

and we choose the closest standard value which is 0.022 μF.

APPENDIX D: ERROR DUE TO C_{INT} LEAKAGE

In order to determine how much leakage from integrator capacitor C_{INT} is tolerable we must first find the relationship between read-out error and leakage current I_L. From Equation (1) it can be seen that the charge Q proportional to 1 count is:

$$Q\ per\ count = \frac{-V_{REF}}{2\, R_1\, f_{IN}} \quad (53)$$

Therefore, to maintain an error of less than 1 count, the net charge leaked from C_{INT} during the measure interval must be less than the charge associated with 1 count.

$$I_L\, \Delta t_{measure} < \frac{V_{REF}}{2\, R_1\, f_{IN}} \quad (54)$$

OR

$$\frac{4096\, I_L}{f_{IN}} < \frac{V_{REF}}{2\, R_1\, f_{IN}} \quad (55)$$

THUS

$$I_L < \frac{V_{REF}}{8192\, R_1} \quad (56)$$

Given the values for the application circuit of Figure 4,

R_1 = 83 K (after trimming)

V_{REF} = 6.8 volts

THEN:

$I_L < 10$ nA to have less than 1 count error

tion of the following transfer functions:

1. The low pass filter composed of R_4, R_5 C_{strg} and the AZ amplifier has a transfer function $G_1(S)$

$$G_1(S) = \frac{V_{AZ}}{V_O} = \frac{R_5}{R_4 + R_5} \quad \frac{S + 1/R_5C_{strg}}{S + 1/C_{strg}(R_4 + R_5)} \qquad (57)$$

which is of the form

$$G_1(S) = \alpha \quad \frac{S + 2\pi f_2}{S + 2\pi f_1} \qquad (58)$$

where α is the high frequency gain of this filter and f_1 and f_2 are the pole and zero frequencies respectively.

2. The closed-loop system composed of the integrator and AZ amplifier has the transfer function $G_2(S)$ shown below:

$$G_2(S) = \frac{V_O}{V_{IN}} = \qquad (59)$$

$$\frac{S\,C_{STRG}(R_4 + R_5) + 1}{S^2 R_3 C_{INT} C_{strg}(R_4 + R_5) + S(R_3C_{INT} + R_5 C_{strg}) + 1}$$

which is of the form

$$G_2(S) = \frac{S\,T_1 + 1}{\frac{1}{\omega_n^2} S^2 + \frac{2\zeta}{\omega_n} S + 1} \qquad (60)$$

SO THAT

$$\omega_n^2 = \frac{1}{R_3 C_{INT} C_{strg}(R_4 + R_5)} \qquad (61)$$

where ω_n is 2π times the natural frequency and ζ is the system damping factor.

With these equations, R_4 and R_5 can be determined. C_{INT} should already be chosen (see Appendix C) and C_{strg} can be somewhat arbitrarily chosen (.1 μF is a good choice to keep R_4 and R_5 at useful resistance values). The following procedure evolved from a desire to decrease the high frequency gain α of the low pass filter while maintaining a well damped Auto-Zero system. The procedure is as follows:

a) From Equations (57) and (58) it can be found that:

$$f_1 = \frac{1}{2\pi C_{strg}(R_4 + R_5)} \qquad (63)$$

The total resistance $(R_4 + R_5)$ can be solved for by setting f_1 equal to 2 times the sampling rate.

b) Since the sum $R_4 + R_5$ is known, R_5 can be found by setting the damping factor equal to 0.4 and solving for R_5 using Equation (62).

c) R_4 can then be found now that R_5 is known.

These AZ filter component values will be valid if:[3]

$$\frac{2048}{f_{IN}} \zeta\, \omega_n \geq 5 \qquad (64)$$

This assures that V_{strg} settles properly during the auto-zero period. If the values determined for R_4 and R_5 do not meet this criteria, a higher value of damping factor should be chosen and the determination of R_5, as delineated in step b, should be repeated.

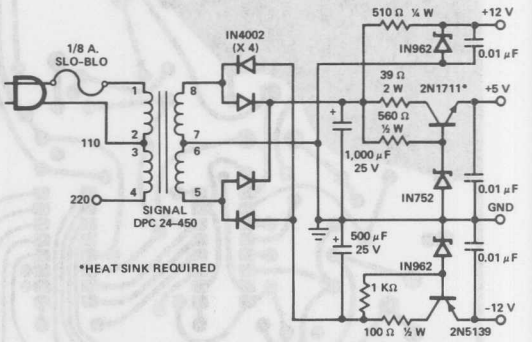
3½ Digit DVM Demonstrator Board

Replace LD111 with LD111A for New Designs

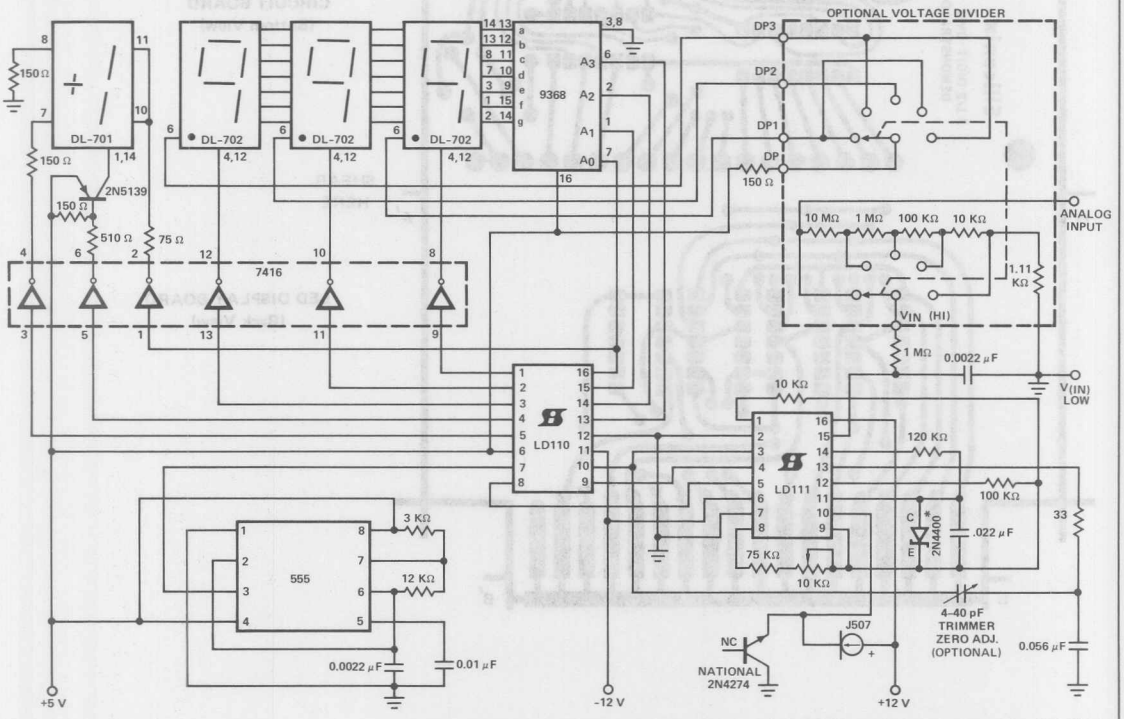
INTRODUCTION

The schematics, parts-list and art-work for a DVM demonstrator board are presented on the following pages. Inexpensive reflective-bar LEDs are used in the basic DVM circuit which features 100 μV resolution and an accuracy of ±0.05% of reading ±1 count. A five range voltage divider shown on the schematic can further extend the usefulness of this instrument. An optional power supply circuit is incorporated into the P.C. board to give line operation if desired.

The metal pattern diagram and component placement diagram are both to 1:1 scale. The component placement art is intended to be silk-screened on the top side of the board to provide easy component installation. It can, however, be used simply as a loading diagram.



OPTIONAL POWER SUPPLY



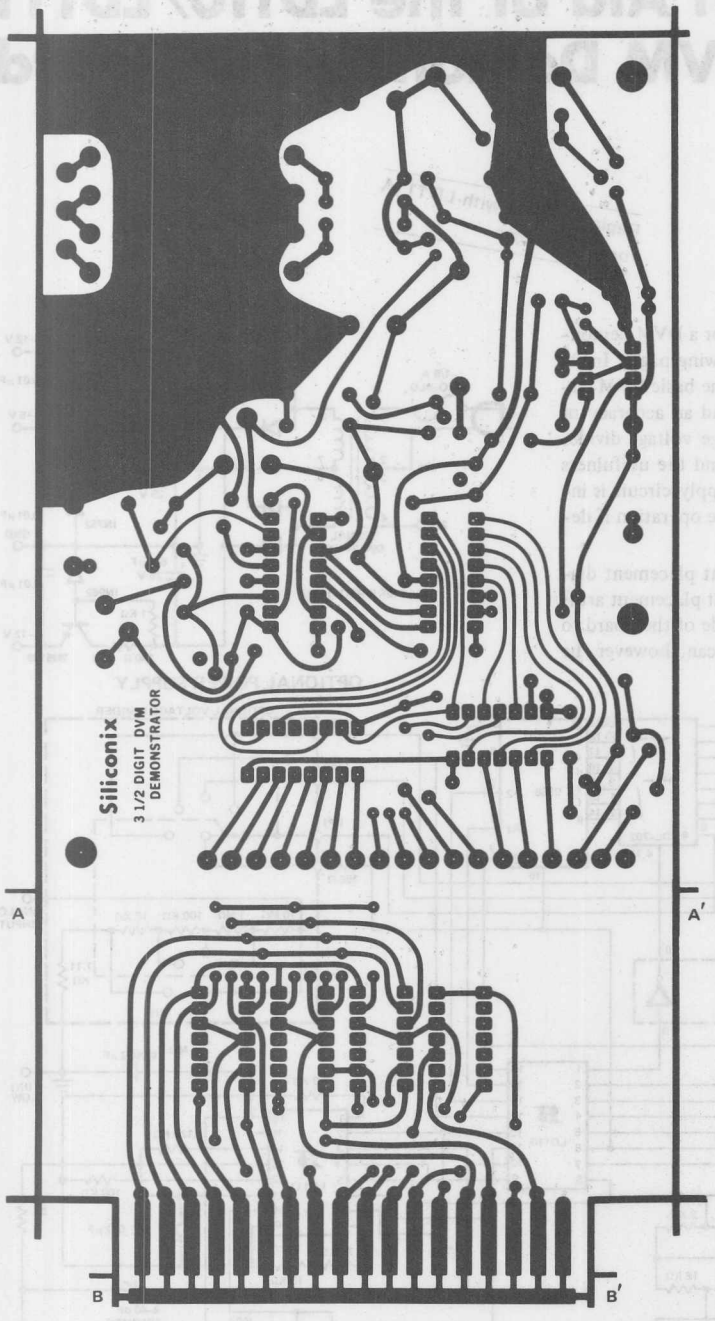
SILICONIX DVM DEMONSTRATOR

*2N4400 not required when using LD111A.

METAL PATTERN FOR DVM BOARD

(refer to last page of design aid for 1:1 P.C. pattern)

Replace LD111 with LD111A for New Designs



SHEAR HERE

CIRCUIT BOARD
(Bottom View)

LED DISPLAY BOARD
(Back View)

FABRICATION HINTS

1. All holes require a #60 drill except for the following holes which require a #54 drill.
 a) Transformer
 b) AC input
 c) Power Supply filter capacitors
 d) 39 Ω Resistor in Power Supply
 e) Trimmer Resistor (10K)
 f) Trimmer Capacitor
 g) Edge Connector (labeled A thru Q)
 h) V_{IN} (Hi and Lo)

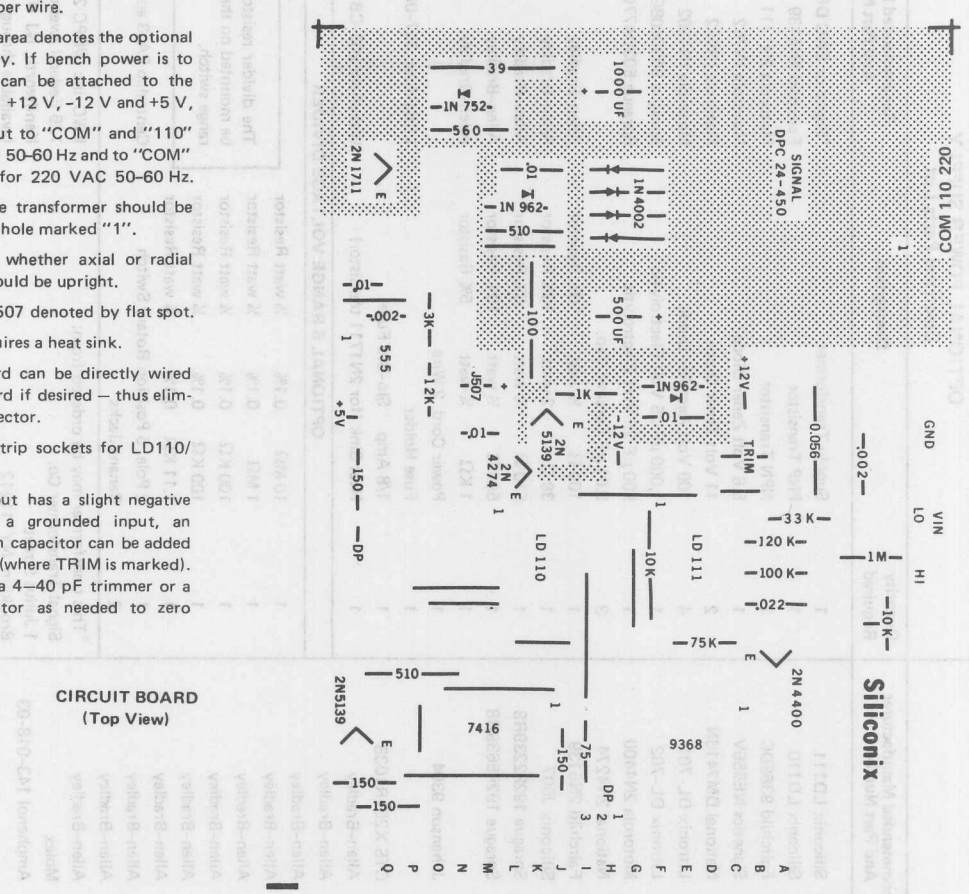
 The location of these holes may be determined from the component placement diagram and the adjacent metal pattern.
2. Shear board along lines A–A′ and B–B′.

COMPONENT PLACEMENT DIAGRAM

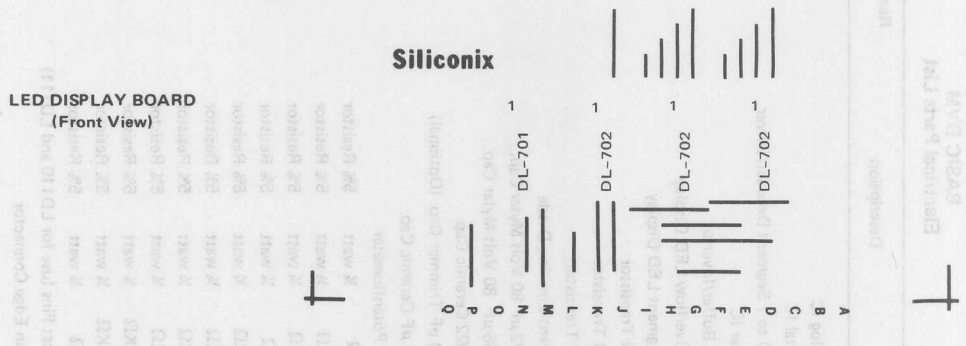
(refer to last page of design aid for 1:1 P.C. pattern)

INSTALLATION HINTS

1. A solid line between two holes requires a jumper wire.
2. The dotted area denotes the optional power supply. If bench power is to be used, it can be attached to the pads marked +12 V, -12 V and +5 V,
3. AC line input to "COM" and "110" for 110 VAC 50-60 Hz and to "COM" and "220" for 220 VAC 50-60 Hz.
4. Pin 1 of the transformer should be aligned with hole marked "1".
5. Filter Caps, whether axial or radial lead type should be upright.
6. Anode of E507 denoted by flat spot.
7. 2N1711 requires a heat sink.
8. Display board can be directly wired to main board if desired — thus eliminating connector.
9. Use Molex strip sockets for LD110/LD111.
10. If the readout has a slight negative offset with a grounded input, an optional trim capacitor can be added to the board (where TRIM is marked). This can be a 4—40 pF trimmer or a fixed capacitor as needed to zero the reading.



CIRCUIT BOARD
(Top View)



LED DISPLAY BOARD
(Front View)

CAUTION!

The AC line voltages associated with this board can be fatal to human life. Proper precautions for operating this instrument must be observed by the user. Siliconix assumes no liability for unsafe operation.

DA74-1 (LD110/LD111)

BASIC DVM
Electrical Parts List

Quantity Required	Description	Recommended Manufacturer And Part Number
1	Analog IC	Siliconix LD111
1	Digital IC	Siliconix LD110
1	BCD to 7 Segment Decoder/Driver	Fairchild 9368DC
1	Timer IC	Signetics NE555V
1	Hex Buffer/Inverter	National DM7416N
1	±1 Overflow LED Display	Litronix DL-701
3	7 Segment LED Display	Litronix DL-702
1	NPN Transistor	Motorola 2N4400
1	NPN Transistor	National 2N4274
1	PNP Transistor	Fairchild 2N5139
1	Current Limiting Diode	Siliconix J507
1	0.022 μF 80 Volt Mylar Cap.	Sprague 192P2239R8
1	0.056 μF 80 Volt Mylar Cap.	Sprague 192P5639R8
1	0.0022 Ceramic Cap.	
1	4-40 pF Trimmer Cap. (Optional)	Johanson 9304
1	0.01 μF Ceramic Cap.	
1	10K Potentiometer	CTS X201R103B
1	75 Ω ¼ watt 5% Resistor	Allen-Bradley
4	150 Ω ¼ watt 5% Resistor	Allen-Bradley
1	510 Ω ¼ watt 5% Resistor	Allen-Bradley
1	3 KΩ ¼ watt 5% Resistor	Allen-Bradley
1	10 KΩ ¼ watt 5% Resistor	Allen-Bradley
1	12 KΩ ¼ watt 5% Resistor	Allen-Bradley
1	33 KΩ ¼ watt 5% Resistor	Allen-Bradley
1	75 KΩ ¼ watt 5% Resistor	Allen-Bradley
1	100 KΩ ¼ watt 5% Resistor	Allen-Bradley
1	120 KΩ ¼ watt 5% Resistor	Allen-Bradley
1	1 MΩ ¼ watt 5% Resistor	Allen-Bradley
32	Socket Pins (use for LD110 and LD111)	Molex
1	18 pin Edge Connector	Amphenol 143-018-03

OPTIONAL POWER SUPPLY
Electrical Parts List

Quantity Required	Description	Recommended Manufacturer And Part Number
1	Supply Transformer	*Signal or EWC DPC24-450
1	PNP Transistor	Fairchild 2N5139
1	NPN Transistor	Motorola 2N1711
1	5.6 Volt Zener Diode	Motorola IN752
2	11 Volt Zener Diode	Motorola IN962
4	100 Volt Rectifier Diode	Motorola IN4002
1	1,000 μF 25 Volt Electrolytic	Sprague 503DI08G025EU
1	500 μF 25 Volt Electrolytic	Sprague 503D477G025EK
3	0.01 μF Ceramic Cap.	
1	100 Ω ½ watt 10% Resistor	Allen-Bradley
1	39 Ω 2 watt 10% Resistor	Allen-Bradley
1	510 Ω ¼ watt 5% Resistor	Allen-Bradley
1	560 Ω ½ watt 10% Resistor	Allen-Bradley
1	1 KΩ ¼ watt 5% Resistor	Allen-Bradley
1	Power Cord, 2 Wire	
1	Fuse Holder	Little-fuse 357-001
1	1/8 Amp Slo-Blo Fuse	
1	Heat Sink (for 2N1711 transistor)	Wakefield 205-CB

OPTIONAL 5 RANGE VOLTAGE DIVIDER

1	10 MΩ 0.1% ½ watt Resistor	
1	1 MΩ 0.1% ¼ watt Resistor	
1	100 KΩ 0.1% ¼ watt Resistor	
1	100 KΩ 0.1% ¼ watt Resistor	
1	1.11 KΩ 0.1% ¼ watt Resistor	
1	2 Pole 5 Position Rotary Switch	Centralab PA-3 and 30° Index
2	Banana Jacks	

The divider resistors should be mounted on the rotary range switch.

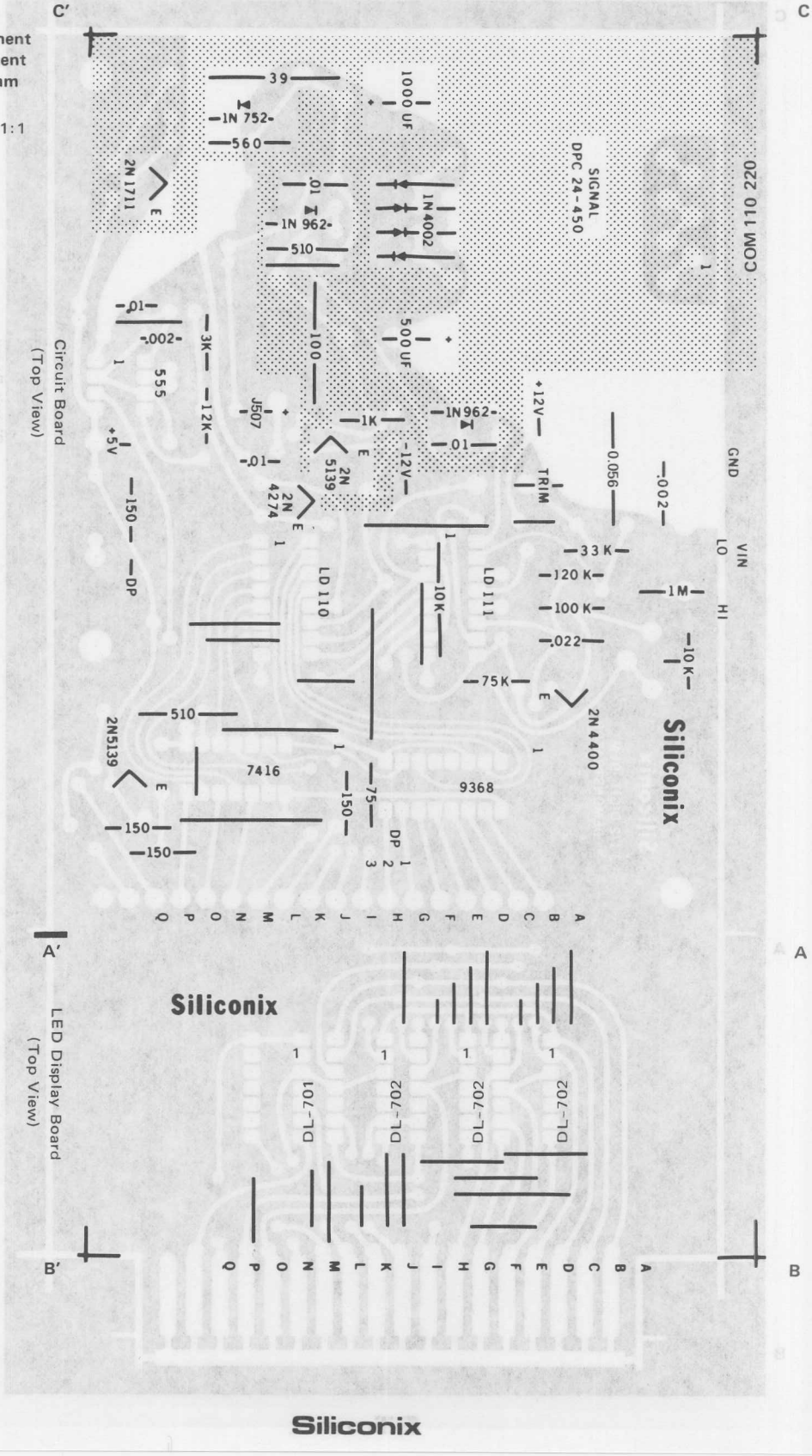
*This transformer may be ordered from:
Signal Transformer Co.
1 Julius Street
Brooklyn, NY 11212
(only direct from factory)

EWC, inc (#DPC-24-450B19)
725 Federal Avenue
Kenilworth, NJ 07033
(available through factory or West coast distributors)

LD110/111 3½ Digit DVM Demonstrator

Component Placement Diagram

Scale 1:1



4½ Digit A/D Converter Set

designed for . . .

- **High Accuracy Digital Voltmeters, Panel Meters**
- **Digital Scales, Thermometers**
- **Microprocessor Data Acquisition Systems**
- **Scientific Instrumentation**

Siliconix

BENEFITS

- 0.005% ±1 Count Accuracy Ensures High System Performance
- Two Ranges, ±2.0000 V or ±200.0 mV, With Single Resistor Change
- 28,672 Count Maximum For 42.5% Overrange
- Sample Rate From One to Five/Second
- Auto-Zero Cycle Nulls Out Internal and External Amplifier Offsets
- Auto-Polarity Operation with One Reference
- Multiplexed BCD Output For Easy Interface To Displays
- Two Overrange Outputs, Underrange Output, Blink Inhibit, and Convert-On-Command Capabilities Allow Easy Interface to External Circuitry and Microprocessors

Replace LD121 with LD121A for New Designs

DESCRIPTION

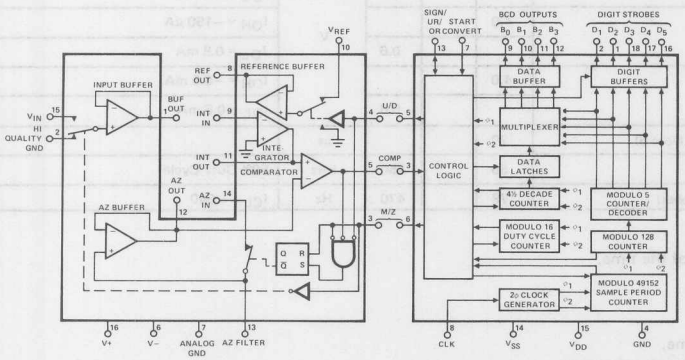
The LD122/LD121A 4½ digit A/D system uses Siliconix's "Quantized Feedback" conversion technique. Intrinsic features of this system are Auto-Polarity, Auto-Zero and ratiometric operation. No critical components are required except for a stable voltage reference and a low noise op amp. The technique offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts, thus critical, high resolution performance is not required of either the integrator or comparator.

The LD120 analog processor is fabricated with a unique combined PMOS/Bipolar process. It contains all the necessary amplifiers, MOSFET switches, and switch driver circuits for the system. The reference voltage input is fully buffered on the LD120 to eliminate the reference switch resistance as a source of error. All the amplifiers are internally compensated. The LD120 directly interfaces the LD121A digital processor with no additional active components required.

The LD121A synchronous processor contains all the digital circuitry for the quantized feedback system. Device outputs supply two overrange signals, underrange, sign and 4 1/2 digits of multiplexed BCD data. (All outputs are TTL compatible). Overrange is also indicated by blinking digit strobes above 20,000 counts. An input is provided to inhibit this feature at user option. Microprocessor controlled operation is simplified by a start conversion input that allows conversion-on-command.

Both devices are supplied in space saving 300 mil dual-in-line plastic packages. The LD120 has 16 pins and the LD121A has 18 pins.

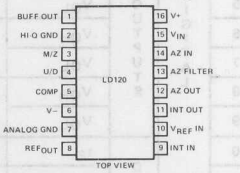
FUNCTIONAL BLOCK DIAGRAM



SWITCH STATES ARE FOR A LOGIC "0" AT U/D AND M/Z INPUTS.

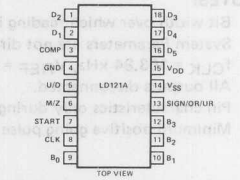
PIN CONFIGURATIONS

Dual-In-Line Package



ORDER NUMBER LD120CJ
SEE PACKAGE8

Dual-In-Line Package



ORDER NUMBER LD121ACJ
SEE PACKAGE 19

V+ – V– (LD120) 32 V
$V_{SS} - V_{DD}$ (LD121A) 20 V
Any Pin (LD121A) V_{DD} to V_{SS} ± 0.3
V_{REF} V+

Power Dissipation (Package)* 750 mW

*Device mounted with all leads welded or soldered to PC Board. Derated 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

			CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS UNLESS NOTED OTHERWISE $V+ = 12\ V; V- = V_{DD} = -12\ V, V_{SS} = 5\ V, T_A = 25°C$
1	SYSTEM (Notes 2 and 3)		Linearity		–1	±1/4	1	Count	2 V Scale
					–2	±1/2	2		200 mV Scale
2			Noise (Note 1)			1/3	1	Count	2 V Scale
						1/2	2		200 mV Scale
3		NMRR				40		dB	f_L = 50 or 60 Hz
		PSRR				80			
4			Gain T.C.			5	15	ppm/°C	
5			Zero Drift			1	5	Count	T_A = 25 to 75°C, C_{STRG} = 1 µF, $R_{IN} \leq$ 100K Ω
6	LD121ACJ DIGITAL	POWER	V_{SS}		4.5	5	5.5	V	Range Over Which Functionality is Guaranteed
7			V_{DD}		–10.8	–12	–13.2		
8			I_{SS}	(Note 4)		14	25	mA	
9			I_{DD}			–14	–25		
10		INPUTS	V_{INH}	Comparator Input, Sign/UR/OR/ Blink (Note 5), Start, CLK IN	4.0			V	Guaranteed Input Threshold Voltages
11			V_{INL}				0.5		
12			I_{INH}	Sign/OR/UR (Note 5)		170	300	µA	V_{IN} = 5 V
13			I_{INL}	Start Convert, Clock		–150	–400		V_{IN} = 0 V
14		OUTPUTS	V_{OH}	Bit Lines, Sign/OR/UR Digit Strobes	2.4			V	I_{OH} = –40 µA
15			V_{OL}				0.6		I_{OL} = 1.6 mA
16			V_{OH}	M/Z	4.0				I_{OH} = –150 µA
17			V_{OL}				0.6		I_{OL} = 0.8 mA
18			V_{OH}	U/D	4.0				I_{OH} = –0.5 mA
19			V_{OL}				0.6		I_{OL} = 0.8 mA
20		DYN	tp	Start Convert (Note 6)	20			µs	
21			f_{CLK}		50		250	kHz	50% Duty Cycle
22				Rep Rate (Strobes)	78		470	Hz	$f_{CLK} \div 640$

NOTES:
1. Bit width over which reading is stable 90% of the time.
2. System Parameters are not directly tested.
3. f_{CLK} = 163.84 kHz, V_{REF} = 6.8 V.
4. All outputs disconnected.
5. Pin characteristics only during D_4 strobe time.
6. Minimum positive going pulse width to initiate a conversion.

ELECTRICAL CHARACTERISTICS (Cont'd)

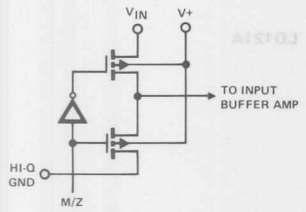
			CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS UNLESS NOTED OTHERWISE $V+ = 12\ V; V- = V_{DD} = -12\ V, V_{SS} = 5\ V, T_A = 25°C$
23	LD1200CJ LINEAR	POWER	V+		9	12	15	V	
24			V−		−9	−12	−15		
25			I+				3.5	mA	
26			I−				−3.5		
27		INPUT BUFF	I_{SOURCE}		−50	−100		µA	$V_{IN} = 2\ V$, Buff Out = 0 V
28			I_{SINK}		400	800			$V_{IN} = -2\ V$, Buff Out = 0 V
29			I_{IN}			2		pA	$V_{IN} = \pm 2.8V$
30			I_{IN}			40			$T_A = 70°C, V_{IN} = \pm 2.8V$
31			CMRR			−72		dB	
32			V_{IN}	(Note 7)	−5		5	V	
33		AZ BUFF	I_{SOURCE}			−100		µA	
34			I_{SINK}			800			
35			I_{STRG}			100		pA	$T_A = 70°C$
36			V_{OFFSET}		−50		50	mV	$V_{OUT} = 0\ V$
37				Switch Resistance (on) (Note 8)		6	20	kΩ	$V_{STRG} = -4\ V, I_{DS} = 30\ \mu A$
38		REF BUF	I_{SOURCE}	Pin 8	−400	−800		µA	V_{IL} (U/D IN), = 0.8 V, $V_O = 0\ V$
39			I_{SINK}	Pin 8		100			V_{IH} (U/D IN) = 2.0 V, $V_O = 2\ V$
40		INT	I_{SOURCE}	(Note 9)	−50	−100		µA	V_{IN} (Int. IN) = −100 mV, $V_O = 0\ V$
41			I_{SINK}		400	800			V_{IN} (Int. IN) = 100 mV, $V_O = 0\ V$
42				Output Swing	−10		8	V	
43		COMP	V_{OUT}		−5			V	R_L = 10k to +5 V, AZ FILTER IN = 100 mV
44			V_{OFFSET}			±5		mV	INTEGRATOR OUT = 0 V
45			I_{IH}	M/Z, U/D Inputs			20	µA	$V_{IH} = 2.0\ V$
46			I_{IL}				−100	µA	$V_{IL} = 0.8\ V$

Typical values are for Design Aid Only, not guaranteed and not subject to production testing.

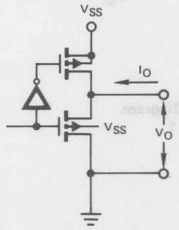
NOTES:

1. Bit width over which reading is stable 95% of the time.
2. System Parameters are not directly tested.
3. $f_{CLK} = 163.84$ kHz, $V_{REF} = 6.8\ V$.
4. All outputs disconnected.
5. Pin characteristic only during D_4 strobe time.
6. Minimum positive going pulse width to initiate a conversion.
7. Maximum voltage for V_{INPUT} (pin 1) or hi-quality GND (pin 2) for which linearity can be guaranteed. (Sum of normal and common mode input.)
8. V_{STRG} must be more positive than −4 volts.
9. Reference Source Impedance must be less than 10K Ω.

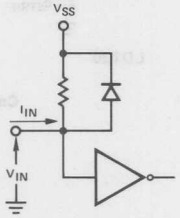
INPUT/OUTPUT SCHEMATICS



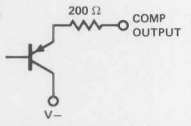
LD120 Input



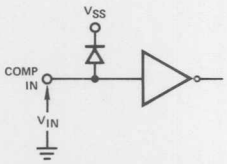
LD121A Output Buffers (Digits, Bits, Sign, M/Z U/D)



LD121A Clock Input Start Convert



LD120 Comparator Output



LD121A Comparator Input

FUNCTIONAL SYSTEM OPERATION

Timing: The external oscillator is divided to generate a 2-ϕ clock on the synchronous digital chip. A time base generator divides the clock frequency into sampling intervals of 49,152 pulses of which 16,384 pulses are the Auto-Zero interval and 32,768 pulses are the measure interval.

Auto-Zero Interval: The connection diagram in Figure 1 illustrates the system during the Auto-Zero interval. The input buffer is switched to reference ground and supplies a current equal to its offset voltage divided by R_2 to the integrator summing mode. The U/D buffer is toggled by the digital processor between V_{REF} and ground with a 50% duty cycle. This results in a current flow equal to V_{REF}/R_1 to the summing node half of the time. The AZ capacitor, C_{STRG}, assumes a voltage, V_{STRG}, that is equal to the average value of integrator output. The AZ buffer supplies a current to the summing node equal to the V_{STRG} voltage divided by R_3.

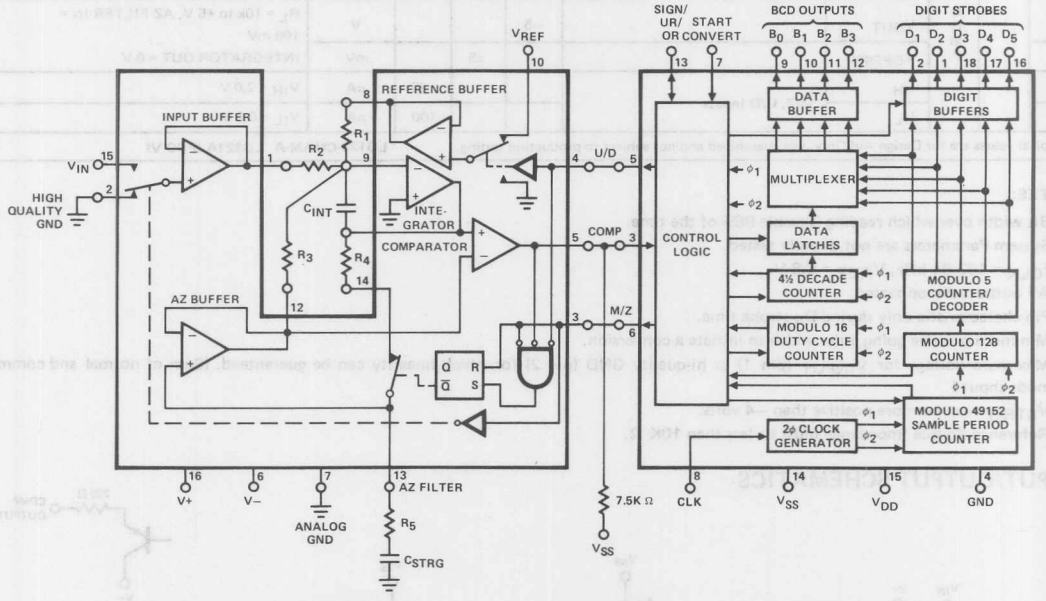
The system will reach an equilibrium when the sum of the DC currents into the summing node equal zero. At this time, the current through R_3 equals $-½\ V_{REF}/R_1$ plus the small currents necessary to cancel the offset of the input buffer and integrator input bias current. Capacitor C_{STRG} "stores" V_{STRG} when the AZ switch opens at the end of the Auto-Zero interval. The digital BCD counter is inactive during Auto-Zero. It is reset to zero during the last clock pulse of the Auto-Zero interval.

THE U/D CONTROL DURING THE MEASURE INTERVAL

The U/D buffer is switched to V_{REF} when the U/D control is low. In this state the currents through R_1 and R_3 sum to $½\ V_{REF}/R_1$. A high level on the U/D control connects the U/D buffer to ground. During this state the sum of the currents through R_1 and R_3 sum to $-½\ V_{REF}/R_1$. In one clock cycle, a charge equal to $V_{REF}/2R_1f_{IN}$ coulombs is either added or subtracted to the integrator capacitor. The BCD counter is decremented for each addition of this quantized charge and incremented for each subtraction of quantized charge.

THE MEASURE ALGORITHM

The input is connected to V_{IN} during the measure interval and supplies a current to the integrator equal to V_{IN}/R_2.



Connection Diagram
Figure 1

FUNCTIONAL SYSTEM OPERATION (Cont'd)

This causes the integrator output to move away from V_{STRG}. The digital processor attempts to keep the integrator output near V_{STRG} by adding or subtracting quantized charge to C_{INT}. The **net** amount of charge required to accomplish this is totaled by the BCD counter. The BCD count at the end of conversion equals the number of charge parcels necessary to cancel the input current supplied through R_2. The resulting count is proportional to the voltage at V_{IN}.

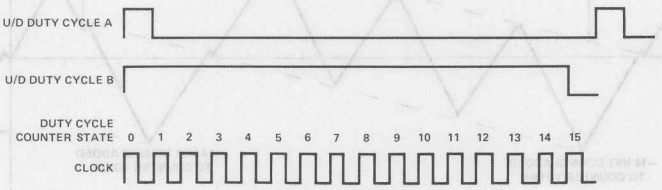
U/D DUTY CYCLE CONTROL DURING THE MEASURE INTERVAL

The digital processor contains a modulo 16 duty cycle counter that provides the U/D control output. This counter examines the state of the comparator once each 16 clock cycles during state 15. If the comparator is high, the U/D control will be high for one cycle and low for 15 cycles in the next 16 clock cycle period of the duty cycle counter. If the comparator output is low, the U/D control will be high for 15 cycles and low for one cycle in the next period of the duty cycle counter. Figure 2 illustrates these waveforms. The effect of these two duty cycles is to source or sink a net 14 charge parcels to C_{INT}, thus driving the integrator output toward V_{STRG} and accumulating counts in the BCD counter in groups of 14 counts. This dual duty cycle control technique results in a fixed number of U/D control transitions, regardless of the value of V_{IN}; therefore, these transitions cannot cause linearity error. The first few periods of the measure interval are illustrated in Figure 3 for a negative V_{IN}.

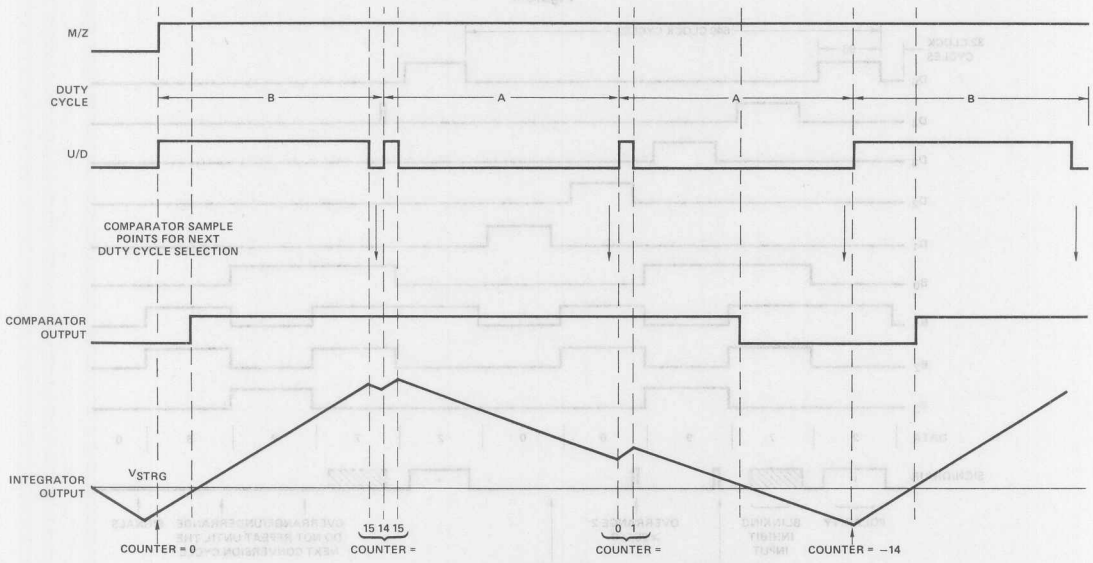
AUTO-ZERO OVERRIDE AT THE END OF MEASURE

The BCD counter contents equal a multiple of 14 counts at the end of the measure interval. A residual voltage on C_{INT} represents the remaining unresolved portion of the input voltage. This voltage is cancelled and the corresponding counts accumulated during a brief override period at the start of the AZ interval. Normal AZ interval action is inhibited until this residual count is resolved.

The override period starts at the end of the Measure Interval. The input buffer is switched to reference ground as no additional charge is desired from V_{IN}. The U/D control is set high. After the comparator goes high, the U/D control is switched low at the next state 8 of the duty cycle counter. The next transition of the comparator ends the



Modulo 16 Dual Duty Cycle Counter Waveforms
Figure 2



Measure Interval Timing ($V_{IN} \approx -1$ V)
Figure 3

FUNCTIONAL SYSTEM OPERATION (Cont'd)

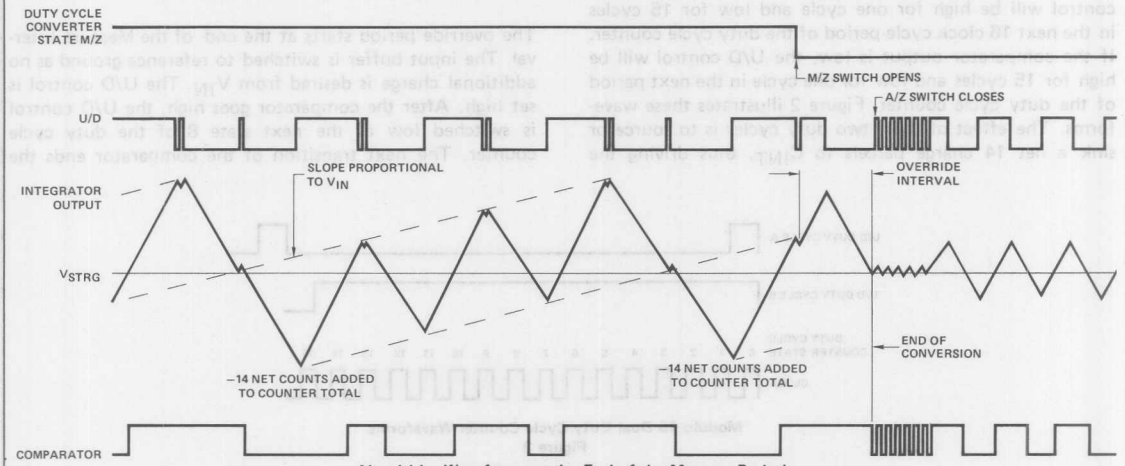
is indicated by the closing of the A/Z switch. The duty cycle counter now drives the U/D control high during states 0 through 7 and low during states 8 through 15 for the required AZ interval 50% duty cycle.

Figure 4 illustrates the events at the end of the measure interval. The slope of the dotted lines is proportional to the unknown current through R_2.

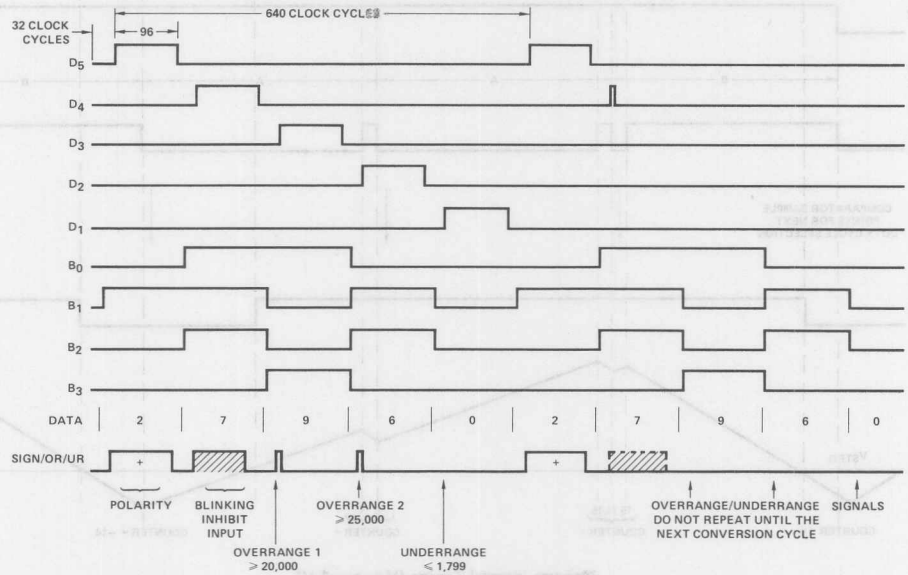
The self oscillation following the override period keeps V_{INT} near V_{STRG} until sync is achieved with the duty cycle counter. This feature eliminates large transients on C_{STRG} and results in highly stable Auto-Zero loop characteristics.

The BCD contents are time multiplexed in a digit serial, bit parallel fashion through 4 push-pull TTL compatible output buffers. A high level (sourcing current from V_{SS}) indicates a one and a low level (sinking current to ground) indicates a zero. B_0 is the least significant Bit. Figure 5 illustrates the timing relationship. All BCD outputs are valid during digit strobe time.

Digit Strobes—(Pins 1, 2, 16, 17 and 18): Figure 5 indicates the operation of these outputs. The strobes are TTL compatible. Only one strobe is high at one time. The strobe period



Alogrithim Waveforms at the End of the Measure Period
Figure 4



LD121 Digital Output Timing Diagram
Figure 5

FUNCTIONAL SYSTEM OPERATION (Cont'd)

is equal to 640 clock cycles with a 15% duty cycle. An inter-digit blanking period of 32 clock cycles permits easy interface with gas discharge displays. The strobe sequence is D_5 (MSD), D_4, D_3, D_2, D_1 (LSD).

Clock Input (Pin 8): Pin 8 requires an external clock input. The system operates from the positive clock transition allowing a 30 to 70% duty cycle in the external oscillator waveform. To maintain the linearity specifications of the A/D converter set the short term stability of this oscillator should be better than 1 part in 2×10^4.

Sign/Overrange/Underrange (Pin 13): This pin operates as a TTL compatible output during D_1, D_2, D_3 and D_5 strobe times and as an input during D_4 strobe time. Figure 5 indicates the timing relationship. Information is presented to this output as follows:

At D_5 Time — Polarity is indicated by a high level for positive and a low level for negative. It is valid approximately 0.25 μsec after D_5 goes high until the end of each D_5 strobe.

At D_4 Time — The output buffer assumes a high impedance state. An input latch samples the voltage level imposed on this pin during D_4 time. A high level will inhibit the overrange blinking (digit strobes are suppressed during zero interval). An internal pull down resistor will hold the pin voltage low if the pin is unconnected or the load is high impedance. An alternative method for selecting overrange blinking is the choice of output buffer. A TTL buffer connected to pin 13 provides a pullup inhibiting overrange blinking. A NPN buffer driver provides a pulldown yielding normal overrange blinking.

At D_3 Time — If the count is equal to or greater than 20,000, a single positive going pulse will occur at the beginning of the first D_3 time after the end of conversion cycle. The pulse width equals one clock cycle. The overrange blinking is momentarily inhibited when overrange pulses are present to prevent the display blinking feature from interfering with the decoding of the overrange output.

At D_2 Strobe Time — A second overrange pulse occurs at the beginning of the first D_2 time, after the end of conversion, if the count is equal or exceeds 25,000 counts.

At D_1 Strobe Time — A single pulse occurs at the beginning of the first D_1 time after the end of conversion, if the count is less than 1800 counts.

All overrange and underrange signals are one clock pulse wide. They occur only once per measure/zero cycle.

Start Conversion (Pin 7): A low level on this TTL compatible input holds the system in the zero mode continuously. A positive going pulse at least one clock time wide initiates one conversion cycle within 16 clock cycles after system has completed minimum auto zero cycle. The digital data is valid after 32,850 clock cycles. A static high level on this input provides normal cyclical operation. An internal pull up resistor allows this input to remain unconnected when conversion control is not desired.

APPLICATIONS

1. The recommended supply voltages are:

 $V+ = 12\ V \pm 10\%$ $\quad V_{SS} = 5\ V \pm 10\%$
 V_{DD}, $V- = -12\ V \pm 10\%$ $\quad V_{REF} = 2\ V$ to $10\ V$

2. The reading is essentially the proportionality of V_{IN} compared to V_{REF} as shown in the gain equation:

$$\frac{\text{READOUT}}{\text{COUNT}} = (V_{IN} - V_{HI\text{-}Q\ GND}) \bullet \frac{R_1}{R_2} \bullet \frac{65{,}536}{V_{REF}}$$

 R_1 is independent of the U/D switch resistance due to the incorporation of the U/D buffer amplifier in the LD120. Gain can be calibrated either by varying V_{REF} or trimming the resistance of R_1 to obtain the correct full scale reading.

3. The output of the integrator should always be more positive than −9 V (for $V_{DD} = -12$ V) to obtain specified accuracy:

 $V_O\ (\text{min}) > -9\ V$

$$V_{O\ (\text{min})} = -\frac{V_{REF}\ R_3}{2R_1} - \frac{15}{f_{CLK}\ C_{INT}}\left[\frac{V_{REF}}{2R_1} + \frac{V_{IN\ (\text{max})}}{R_2}\right]$$

 Change value of C_{INT} to set V_{INT}(P-P).

 Large integrator swing provides the best performance. V_{INT} (P-P) = 6 to 8 volts is recommended.

$$V_{INT\ (\text{P-P})} = \frac{30}{f_{CLK}\ C_{INT}}\left[\frac{V_{REF}}{2R_1} + \frac{V_{IN\ (\text{max})}}{R_2}\right]$$

4. Although any oscillator frequency from 50 kHz to 250 kHz can be used, frequencies that provide integer number of line frequency cycles per measure period provide maximum line noise rejection. These frequencies are:

$$f_{CLK} = \frac{32{,}768\ F_{LINE}}{n},\ n = 8, 9, 10, \ldots 40$$

 $f_{CLK} = 163{,}840$ is popular since it provides both 50 and 60 Hz rejection.

5. The sampling rate = $f_{CLK}/49{,}152$ cycles/sample.

6. After a start conversion pulse, data is valid 32,850 clock pulses later and remains valid until at least 32,768 clock pulses after the next start pulse. During continuous cycle operation, data is assured valid when M/Z is high or 100 clock cycles after the one/zero transition of M/Z.

7. Any capacitive coupling between U/D and Comp. is detrimental to proper algorithm operation. PC board layouts should not allow these traces to be adjacent.

APPLICATIONS (Cont'd)

8. All power supplies should be capacitively bypassed to ground for maximum count stability.

9. C_{INT} and C_{STRG} should be selected for low leakage. Silvered mica is recommended for C_{INT} and mylar for C_{STRG}. Polypropylene capacitors also work well for both C_{STRG} and C_{INT}.

10. For a given leakage into C_{STRG} of I_{STRG}:

$$\Delta V_{STRG} = \frac{\Delta t\, I_{AZ}}{C_{STRG}}$$

where Δt = a measure interval $= \frac{2}{3} \frac{1}{F_{SAMPLE}}$

ΔV_{STRG} will inject a ΔI integrator of $\Delta V_{STRG}/R_3$

Now a ΔI integrator would have been equivalent to a $\Delta V_{IN}/R_2$

So the equivalent input drift is

$$\Delta V_{IN} = \frac{1}{2} \frac{R_2}{R_3} \frac{2}{3} \frac{I_{STRG}}{F_{SAMPLE} \bullet C_{STRG}}$$

the ½ factor is provided by integrator action.

Example: We wish to see 1 count (0.1 mV of ΔV_{IN} on the 2 V range) of drift for the circuit of Figure 7 with I_{STRG} = 100 pA @ 70°C. What C_{STRG} is needed?

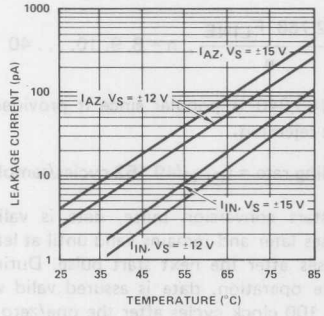
Answer:

$$C_{STRG} = \frac{R_2}{R_3} \frac{1}{3} \frac{I_{STRG}}{F_{SAMPLE} \cdot \Delta V_{IN}} =$$

$$\frac{100K\,\Omega}{62K\,\Omega} \times \frac{1}{3} \times \frac{10^{-10}\ F}{3\ Hz \times 10^{-4}\ V}$$

$= 0.18\,\mu F$ Minimum

Typical Leakage Over Temperature



11. Interfacing the LD120/LD121A to Microprocessors: A description of interfacing the LD120/LD121A to the 8080 μP is given in AN77-3. Some of the timing details warrant description here.

The end-of-conversion is determined by gating $\overline{M/Z} \cdot \overline{U/D} \cdot \overline{COMP}$. At this time, all BCD latches are updated with the contents of the latest conversion.

We recommend using the positive edge of M/Z to interrupt the processor. Next, test for a high D_5 digit strobe (MSD). Once D_5 is high load the BCD data from B_0–B_3 lines and the polarity information from the SIGN/OR/UR line. Next delay 128 LD121A clock times (this assures that the D_4 data is valid) then load B_0–B_3 lines containing the D_4 data. Next delay another 128 LD121A clock times (this assures that the D_3 data is valid) then load B_0–B_3 lines containing the D_3 data. Repeat this process for D_2 and finally the D_1 (LSD) data load. In flowchart form (see Figure 6).

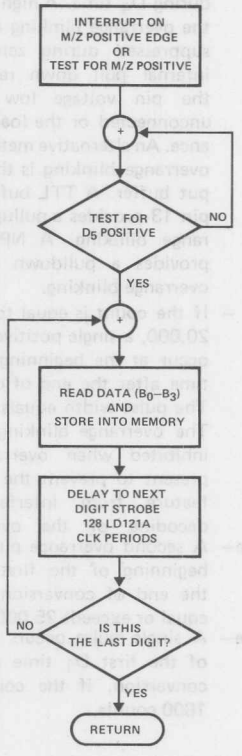


Figure 6

CIRCUIT BENEFITS

- Overrange Blinking
- 0 → ±1.9999 Input Voltages
- Zero Adjust to Null Offset Introduced by PC Board Leakages and Comparator

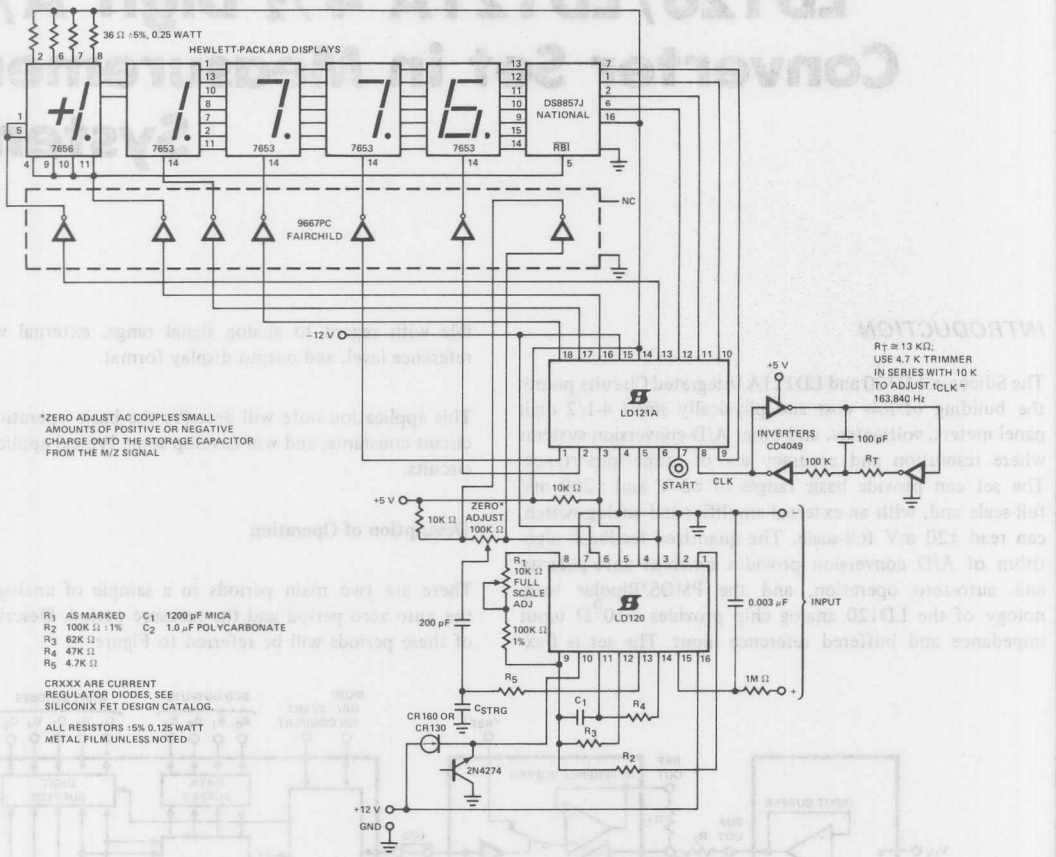


Figure 7

Siliconix

Function/Application of the LD120/LD121A 4½ Digit A/D Converter Set in Measurement Systems

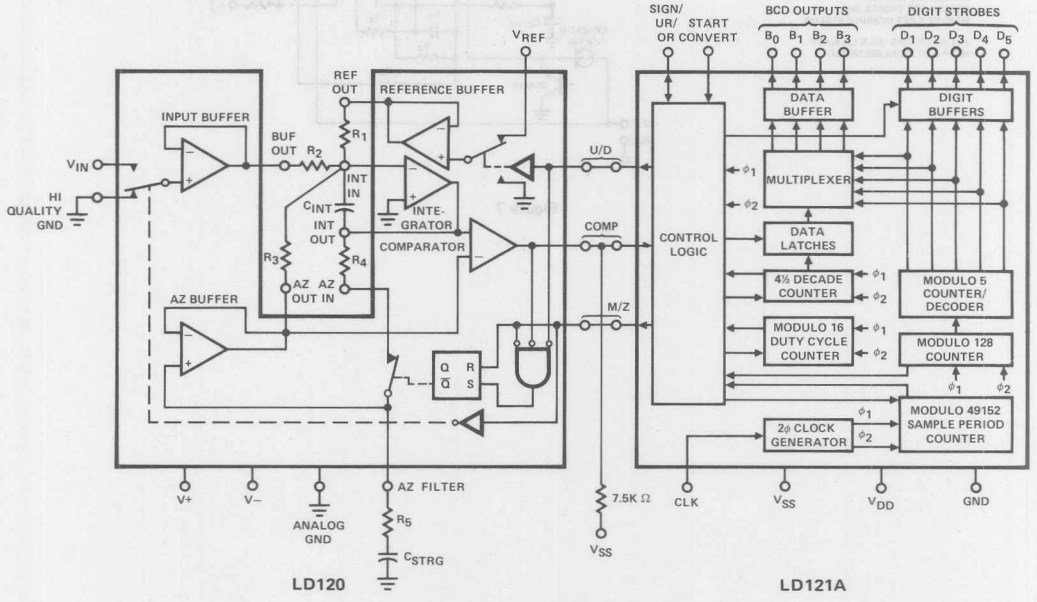
INTRODUCTION

The Siliconix LD120 and LD121A Integrated Circuits permit the building of low cost and physically small 4-1/2 digit panel meters, voltmeters, and other A/D conversion systems where resolution and accuracy are of prime importance. The set can provide basic ranges of ±2 V and ±200 mV full-scale and, with an external amplifier and analog switch, can read ±20 mV full-scale. The quantized feedback algorithm of A/D conversion provides inherent auto-polarity and auto-zero operation, and the PMOS/Bipolar technology of the LD120 analog chip provides $>10^9\Omega$ input impedance and buffered reference input. The set is flexible with regard to analog signal range, external voltage reference level, and output display format.

This application note will describe the basic operation and circuit constants, and will develop some typical applications circuits.

Description of Operation

There are two main periods in a sample of analog data; the auto zero period and the measure period. Descriptions of these periods will be referred to Figure 1.



Connection Diagram
Figure 1

Auto-Zero Interval

In the auto-zero period, the input buffer is connected to high-quality ground and the auto-zero buffer is connected to the integrator output. Ignoring up/down and transient waveforms for the moment, the DC currents presented to the integrator are:

$$I_{INT} = I_{BIAS,\,INT} \equiv \frac{V_{OFFSET,\,INPUT\ BUFFER}}{R_2} + \frac{V_{OFFSET,\,AZ\ BUFFER}}{R_3} + \frac{V_{OFFSET,\,REFERENCE\ BUFFER}}{R_1} + \frac{V_{AZ,\,OFFSET}}{R_3} + \frac{V_{HI\text{-}Q}}{R_2}.$$

$V_{AZ,\,OFFSET}$ is the fraction of the auto-zero voltage across C_{AZ} which will null all the other quantities mentioned above. Also being injected into the integrator input is $V_{REF}/2R_1$ since the up/down line is being toggled at 50% duty cycle by the LD121A. When the dynamics of the system settle out toward the end of the zero period, C_{AZ} will have the voltage

$$V_{AZ} = V_{AZ,\,OFFSET} - \frac{R_3}{2R_1} V_{REF}.$$

$-V_{REF}\ R_3/2R_1$ provides a reference quantity of exactly negative one-half the integrator input current injected by the reference current through R_1.

The auto-zero period is 16,384 clock times long.

Measure Interval

During the measure interval, the input buffer is connected to V_{IN} and the auto-zero capacitor is disconnected from the integrator output. The quantity $V_{AZ,\,OFFSET}$ remains on C_{AZ}, and analog offsets are nulled out. Due to the quantity $-V_{REF}\ R_3/2R_1$ being held on C_{AZ}, an effective $V_{REF}/2$ or $-V_{REF}/2$ is applied through R_1 when U/D is 0 and 1, respectively.

Referring to Figure 2, the U/D waveforms are of 2 kinds: 1 clock time up and 15 down; and 15 clock times up and 1 down. The LD121A logic generates these waveforms in response to the LD120 comparator output. The system attempts to return the integrator output to V_{AZ} regardless of the input. Since the integrator sees both input and reference currents simultaneously, its output does not vary far from V_{AZ}.

The BCD counter counts up once per clock time when U/D=1 and down once per clock time when U/D=0, causing the displayed count to be proportional to the amount of $V_{REF}/2R_1$ that was required to null V_{IN}/R_2 during the measure interval. The charge balancing in the measure interval calculates so:

$$Q = \frac{V_{IN} - V_{HI\text{-}Q}}{R_2}\ \Delta t \equiv \text{Count}\ \frac{1}{f_{OSC}}\ \frac{V_{REF}}{2R_1}$$

where $\Delta t = 32{,}768/f_{OSC}$ and is the measure period.

Rearranging,

$$\text{Count} = \frac{V_{IN} - V_{HI\text{-}Q}}{V_{REF}}\ \frac{R_1}{R_2} \cdot 65{,}536.$$

The measure interval cannot resolve single counts; it can only resolve multiples of 14 counts. Immediately after the measure and into the auto-zero period is the override period. The input buffer is reconnected to $V_{HI\text{-}Q}$ and the C_{AZ} switch is left open. The LD121A sends the integrator positive with respect to V_{AZ} (see Figure 3), then returns it to V_{AZ} potential, stopping when the LD120 comparator changes states, keeping track of the count in single clock times. The override period can exist a maximum of 56 clock times into the zero period, assuming a non-overload V_{IN}.

Since only 14 of the 16 counts in the U/D waveform produce net counts, there are ±28,672 counts maximum out of the 32,768 clock times available.

Component Selection

R_1 and R_2: The nominal currents into the integrator are 20 μA full-scale through R_2 and 80 μA through R_1. These values are chosen for minimum system noise consistent with maximum amplifier linearities. Then

$$R_2 = \frac{V_{IN}\,(F.S.)}{20\ \mu A},\quad R_1 = \frac{V_{REF}}{80\ \mu A}.$$

V_{REF} should be in the range of 2 V to 8 V, for reasons of system gain stability and noise characteristics. Some trimming of either R_2 or R_1 is required for exact full-scale reading.

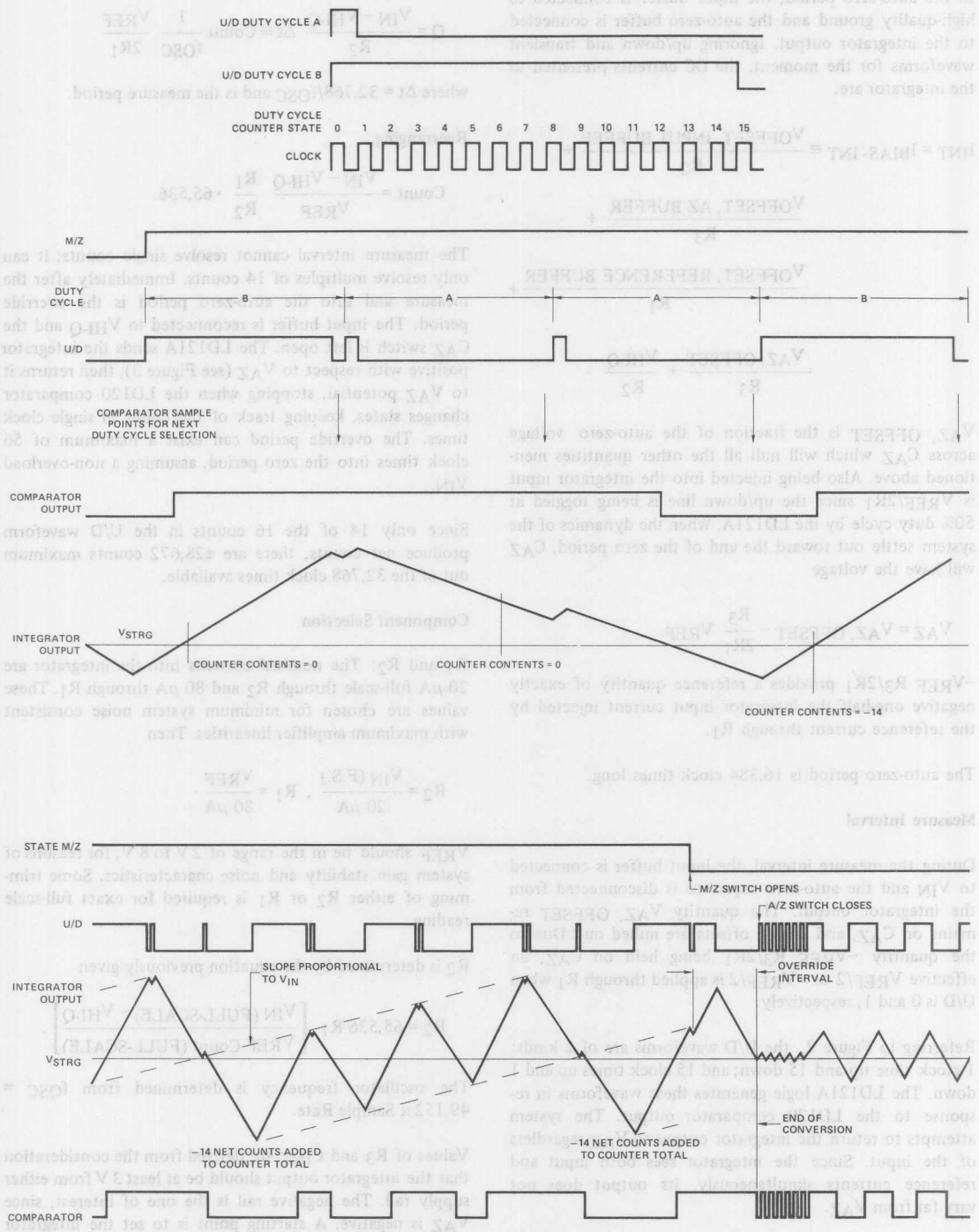
R_2 is determined by the equation previously given

$$R_2 = 65{,}536\ R_1 \left[\frac{V_{IN}\,(FULL\text{-}SCALE) - V_{HI\text{-}Q}}{V_{REF}\ Count\ (FULL\text{-}SCALE)}\right].$$

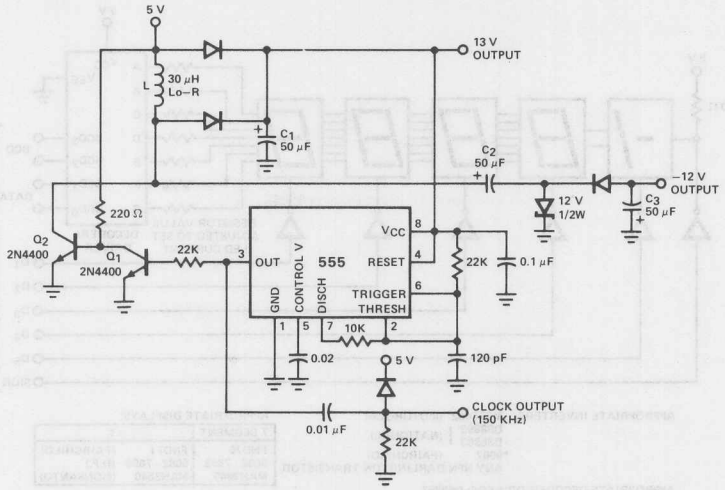
The oscillator frequency is determined from f_{OSC} = 49,152 x Sample Rate.

Values of R_3 and C_{INT} are derived from the consideration that the integrator output should be at least 3 V from either supply rail. The negative rail is the one of interest, since V_{AZ} is negative. A starting point is to set the integrator AC swing at about 6 V p-p. Then

$$C_{INT} \equiv \frac{V_{REF}}{R_1} \cdot \frac{1}{6\ V} \cdot \frac{30}{f_{OSC}}$$



Up/Down and Integrator Waveforms
Figure 2



LD120/121A Power Supply and Clock
Figure 3

The factor of 30 results from the fact that 2 cycles, 1 up and 1 down, each having an effective 15 clock times before folding back for 1 clock time, are required to cause the 6 V p-p swing. The envelope of integrator waveform can be almost completely above V_{AZ} or below it; so a V_{AZ} = −3 V is appropriate. Neglecting the offset components of V_{AZ}, which are relatively small, we have

$$-V_{AZ} \simeq V_{REF} \frac{R_3}{2R_1} + V_{HI\text{-}Q} \frac{R_3}{R_2},$$

and setting $V_{AZ} \equiv -3$ V,

$$R_3 \equiv \frac{6R_1 R_2}{R_2 V_{REF} + 2R_1 V_{HI\text{-}Q}} \ \Omega.$$

C_{AZ} is chosen from the range of 0.1 to 1 μF, as determined by zero drift considerations given in appendix A.

R_4 and R_5 are selected in consideration of settling time of the system in the auto-zero period. Typical values are 47K and 4.7K for C_{INT} = 1200 pF at 3 samples/second.

As for component quality, R_3, R_4, and R_5 are non-critical. R_1 and R_2 should be metal film or wirewound. C_{INT} should be mylar or better quality and C_{AZ} must be mylar, polycarbonate, or polypropylene, the latter being best with regards to dielectric absorption characteristic.

Finally, the oscillator must be short term stable, even though long term drift is not a problem.

APPLICATIONS CIRCUITS

Power Supplies

The plus and minus 12 V supplies can be obtained from a standard 5 V supply, as well as the required oscillator signal, with the circuit in Figure 3.

The 13 V output is pulled to 4.3 V upon connecting 5 V input. This allows the 555 to start oscillating, driving Q_1 and Q_2. Q_2 pulls current through L for approximately 50% of the time, and releases it to allow the flyback voltage to charge C_1. The negative edge of Q_2's collector waveform charges C_3 through its associated rectifier circuitry, and the 12 V zener absorbs all unused energy available from L in shunt regulator style.

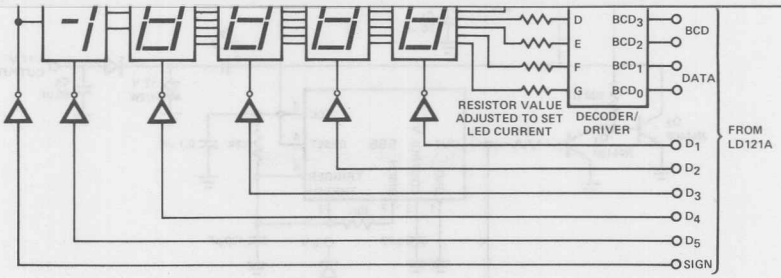
The circuit performs adequately for a supply of 4.5 V to 5.5 V input, and the 555 being run from the 13 V output, is not modulated by the 5 V power line noise.

Display Formats

Figures 4 and 5 show common cathode and anode type light-emitting diode (LED) display circuits. Both are multiplexed to conserve supply current.

The duty cycle of each strobe is 15%. If an average LED current of 5 mA is desired, each digit strobe switch must be able to pass 5 mA x 7 segments/0.15 = 233 mA, necessitating the use of strong drivers. Also the decoder/driver must be able to pass 5/0.15 or 33 mA. The use of high-efficiency LED's, running at an average of 3 mA, would be advisable, but not necessary.

Figure 5 shows a simple circuit for leading zero blanking when a decoder/driver has that function built in. There are 2 flip flops in the circuit. D_5 initiates the G_3/G_4 latch to begin a scan in the order D_5-D_4-D_3-D_2-D_1. G_3 enables the G_1/G_2 latch until D_X resets G_4 and G_3, disabling G_1/G_2. G_1 and G_2 form a ones-catching latch through RBI and RBO; RBO = 1 resets the latch, disabling RBI. Thus either D_X or RBO can terminate a zero blanking sequence.



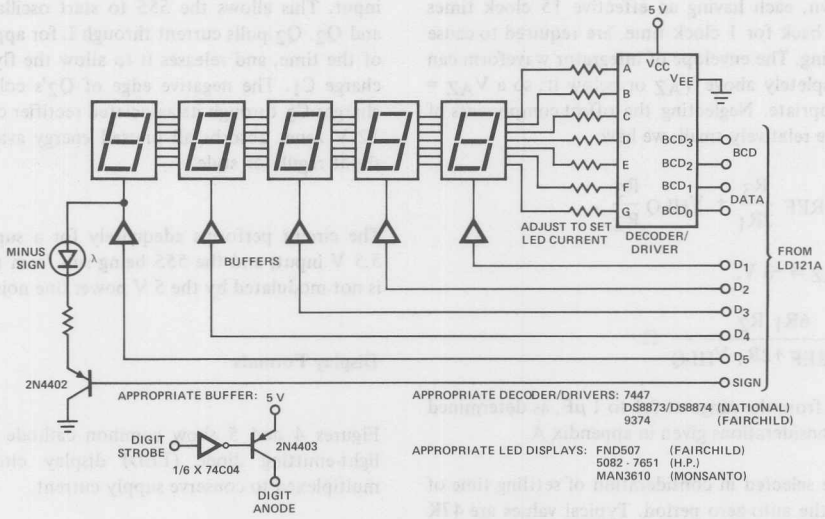
APPROPRIATE INVERTERS: MC75452 (MOTOROLA)
DS8892, DS8863 (NATIONAL)
*9967 (FAIRCHILD)
ANY NPN DARLINGTON TRANSISTOR

APPROPRIATE DISPLAYS:

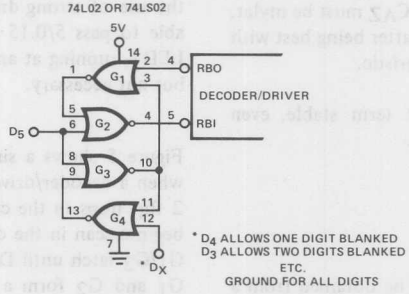
7 SEGMENT	±1	
FND70	FND71	(FAIRCHILD)
5082 - 7653	5082 - 7656	(H.P.)
MAN3640	MAN3640	(MONSANTO)

APPROPRIATE DECODER/DRIVERS: DS8857
74C48

Common Cathode LED Display (±19,999 Counts max. with Blinking)
Figure 4



Common Anode LED Display (±28,672 Counts max. without Blinking)
Figure 5a



* D_4 ALLOWS ONE DIGIT BLANKED
D_3 ALLOWS TWO DIGITS BLANKED
ETC.
GROUND FOR ALL DIGITS

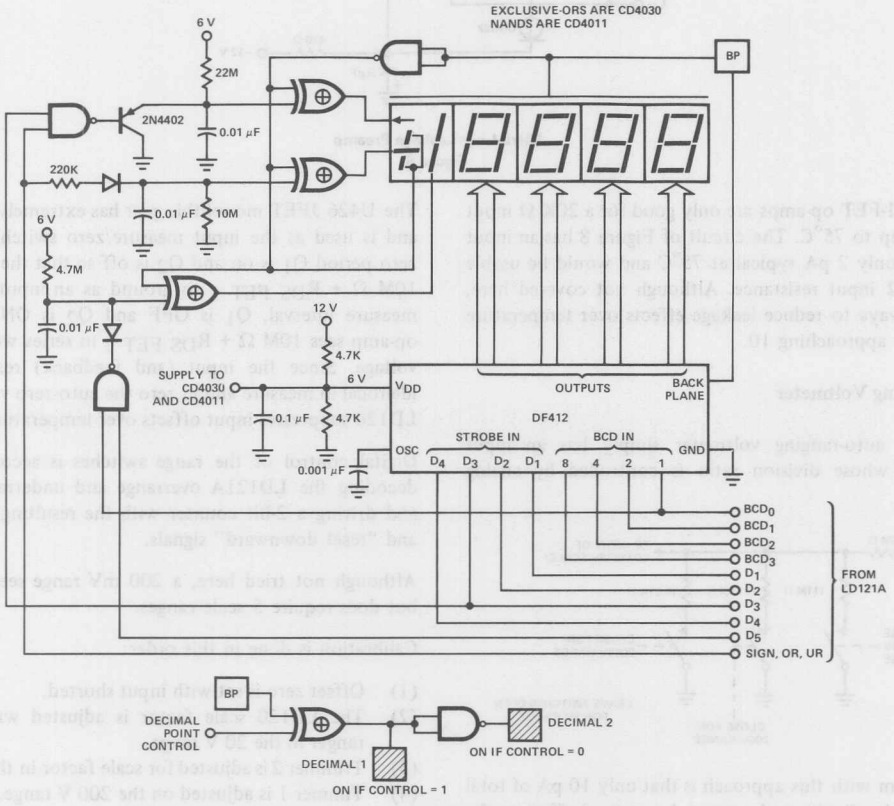
Leading Zero Blanking
Figure 5b

Figure 6 shows an LCD display circuit. The Siliconix DF412 accepts BCD data in strobe fashion, latches it, and presents decoded 7-segment drive to the LCD display. The overrange, sign, and leading "1" are provided by CMOS decoding and RC memory circuits through the exclusive-or LCD drivers. The effective LCD drive is 12 V p-p with a 6 V supply for the DF412 and CD4030.

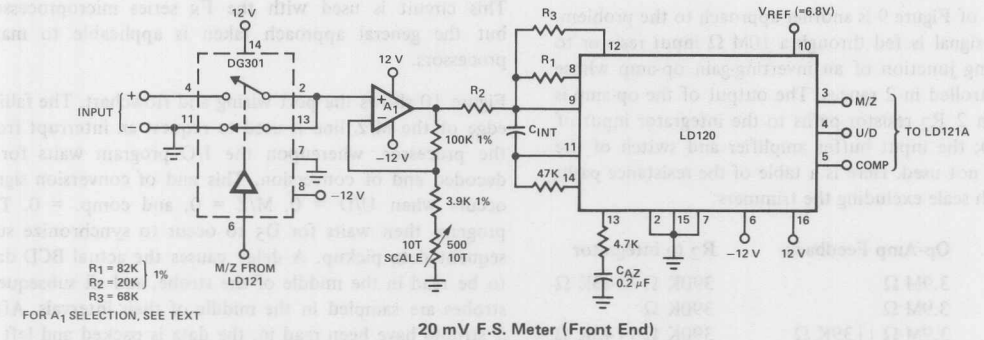
Preamplifiers

A feature of the quantized-feedback conversion is the ability to use external preamplifiers within the auto-zero loop. This allows a preamp that is quiet but has poor DC characteristics to be used down to a stable 1 μV/LSB sensitivity. This is necessary for sensitivities greater than 200 mV full-scale because the PMOS transistors of the LD120 do not have good 1/F noise characteristics.

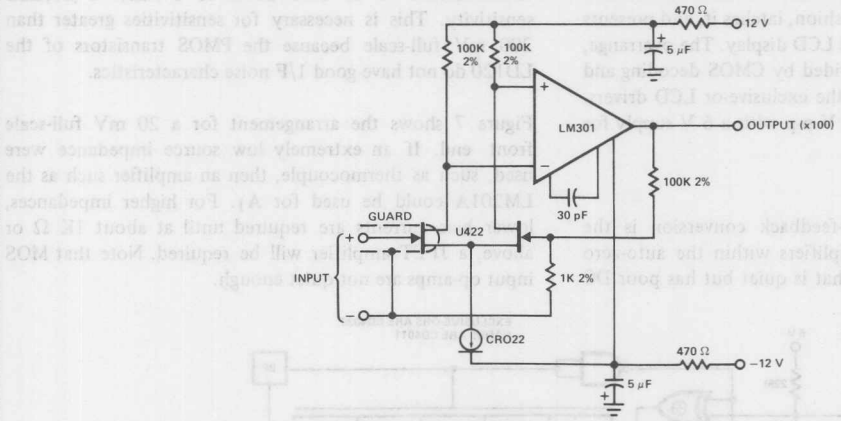
Figure 7 shows the arrangement for a 20 mV full-scale front end. If an extremely low source impedance were used, such as thermocouple, then an amplifier such as the LM201A could be used for A_1. For higher impedances, lower bias currents are required until at about 1K Ω or above, a JFET amplifier will be required. Note that MOS input op-amps are not quiet enough.



LCD Display
Figure 6



20 mV F.S. Meter (Front End)
Figure 7

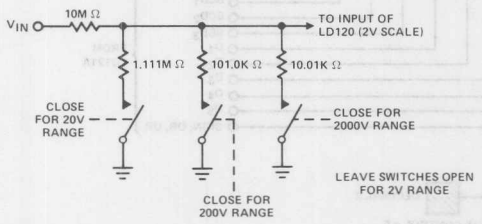


Ultra-Low-Leakage Preamp
Figure 8

Even the BI-FET op-amps are only good for a 20K Ω input resistance up to 75°C. The circuit of Figure 8 has an input leakage of only 2 pA typical at 75°C and would be usable with 1M Ω input resistance. Although not covered here, there are ways to reduce leakage effects over temperature by a factor approaching 10.

Auto-Ranging Voltmeter

The usual auto-ranging voltmeter simply has an input attenuator whose division ratio is controlled by analog switches:



The problem with this approach is that only 10 pA of total leakage at the divider node causes 1 count of offset on the 2 V range. 10 pA is not easily met over temperature.

The circuit of Figure 9 is another approach to the problem. The input signal is fed through a 10M Ω input resistor to the summing junction of an inverting-gain op-amp whose gain is controlled in 2 ranges. The output of the op-amp is fed through 2 R_2 resistor paths to the integrator input of the LD120; the input buffer amplifier and switch of the LD120 are not used. Here is a table of the resistance paths used in each scale excluding the trimmers:

Range	Op-Amp Feedback	R_2 to integrator
2 V	3.9M Ω	390K Ω \|\| 43K Ω
20 V	3.9M Ω	390K Ω
200 V	3.9M Ω \|\| 39K Ω	390K Ω \|\| 43K Ω
2000 V	3.9M Ω \|\| 39K Ω	390K Ω

The U426 JFET monolithic pair has extremely low leakage and is used as the input measure/zero switch. During the zero period Q_1 is on and Q_2 is off so that the op-amp sees 10M Ω + $R_{DS\ FET\ 1}$ to ground as an input. During the measure interval, Q_1 is OFF and Q_2 is ON so that the op-amp sees 10M Ω + $R_{DS\ FET\ 2}$ in series with the input voltage. Since the input (and feedback) resistances are identical in measure and in zero the auto-zero voltage of the LD120 suppresses input offsets over temperature.

Digital control of the range switches is accomplished by decoding the LD121A overrange and underrange outputs and driving a 2-bit counter with the resulting "count up" and "reset downward" signals.

Although not tried here, a 200 mV range seems possible, but does require 5 scale ranges.

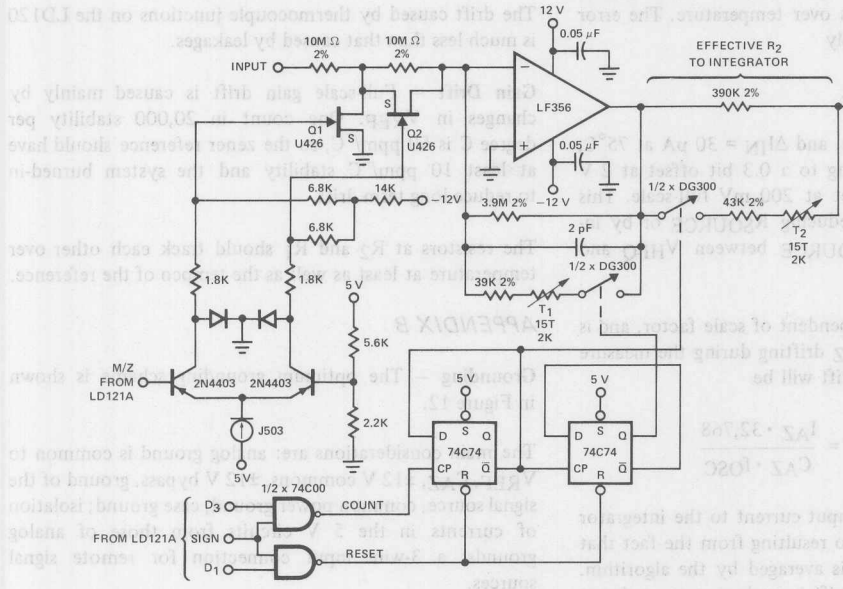
Calibration is done in this order:

(1) Offset zero is set with input shorted.
(2) The LD120 scale factor is adjusted with the auto ranger in the 20 V range.
(3) Trimmer 2 is adjusted for scale factor in the 2 V range.
(4) Timmer 1 is adjusted on the 200 V range.

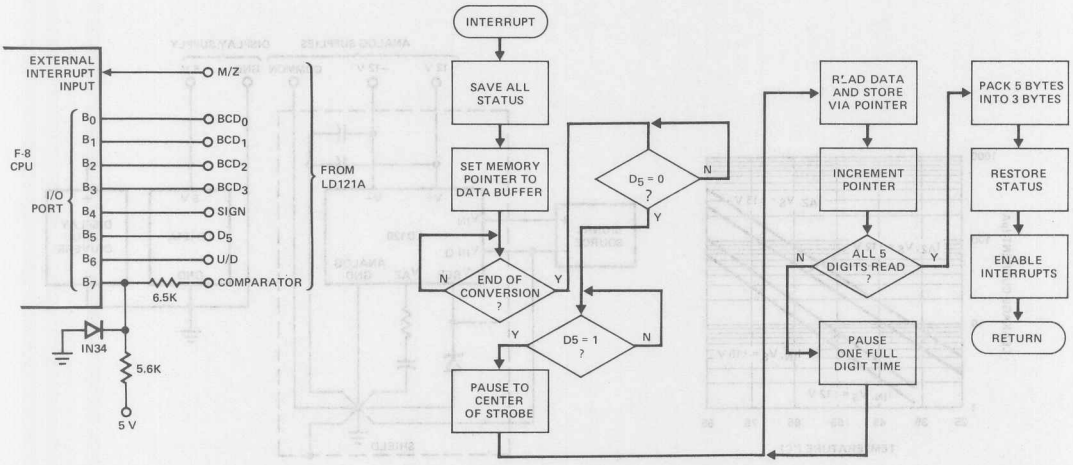
Microprocessor Interface

This circuit is used with the F8 series microprocessor, but the general approach taken is applicable to many processors.

Figure 10 shows the port wiring and flowchart. The falling edge of the M/Z line is used to request an interrupt from the processor, whereupon the I/O program waits for a decoded end of conversion. This end of conversion signal occurs when U/D = 0, M/Z = 0, and comp. = 0. The program then waits for D_5 to occur to synchronize subsequent data pickup. A delay causes the actual BCD data to be read in the middle of the strobe, and all subsequent strobes are sampled in the middle of their intervals. After 5 strobes have been read in, the data is packed and left in a location of memory.



Auto-Ranging Amplifier; 2–2000 V Ranges
Figure 9



F-8/LD121A Interface
Figure 10

APPENDIX A: ERROR TERMS

$$\Delta V_{IN} = \Delta I_{IN} \cdot R_{SOURCE}.$$

For a 1M Ω input resistance, and ΔI_{IN} = 30 pA at 75°C, ΔV_{IN} = 30 μV, corresponding to a 0.3 bit offset at 2 V full-scale, and 3 count offset at 200 mV full-scale. This offset can be reduced by reducing R_{SOURCE} or by inserting a compensating R_{SOURCE} between $V_{HI\text{-}Q}$ and ground.

The drift due to I_{AZ} is independent of scale factor, and is caused by the voltage on C_{AZ} drifting during the measure interval. The magnitude of drift will be

$$\Delta V_{AZ} = \frac{I_{AZ} \cdot T_{MEASURE}}{C_{AZ}} = \frac{I_{AZ} \cdot 32{,}768}{C_{AZ} \cdot f_{OSC}}$$

This will cause an effective input current to the integrator of $\Delta V_{AZ}/2R_3$, the factor two resulting from the fact that the ramp of auto-zero drift is averaged by the algorithm. This input current due to drift is analogous to an input signal of $\Delta V_{AZ}\ R_2/2R_3$, so the count drift is

$$\Delta\text{Count} = \frac{\Delta I_{AZ}}{C_{AZ}\, f_{OSC}\, V_{REF}} \cdot \frac{R_1}{2R_3} \cdot 2.15 \times 10^9$$

So given ΔI_{AZ} = 100 pA when up at 70°C, R_1 = 60K = R_3,

Gain Drift – Full-scale gain drift is caused mainly by changes in V_{REF}. One count in 20,000 stability per degree C is 50 ppm/°C, so the zener reference should have at least 10 ppm/°C stability and the system burned-in to reduce long term drift.

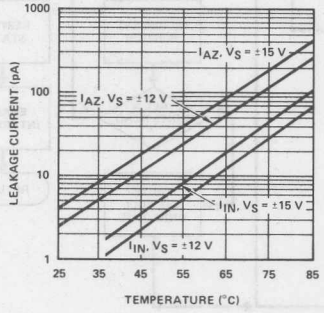
The resistors at R_2 and R_1 should track each other over temperature at least as well as the tempco of the reference.

APPENDIX B

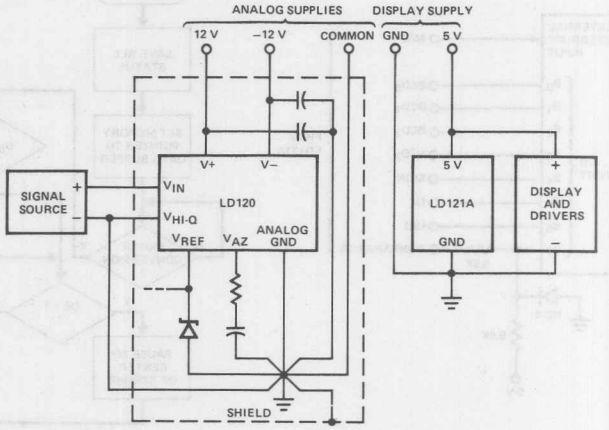
Grounding – The optimum grounding scheme is shown in Figure 12.

The main considerations are: analog ground is common to V_{REF}, C_{AZ}, ±12 V commons, ±12 V bypass, ground of the signal source, common power ground, case ground; isolation of currents in the 5 V circuits from those of analog grounds; a 3-wire input connection for remote signal sources.

These connection methods will alleviate AC and DC pickup in signal inputs and integrator positive input (analog ground) from noise currents caused by the display and AC environment.



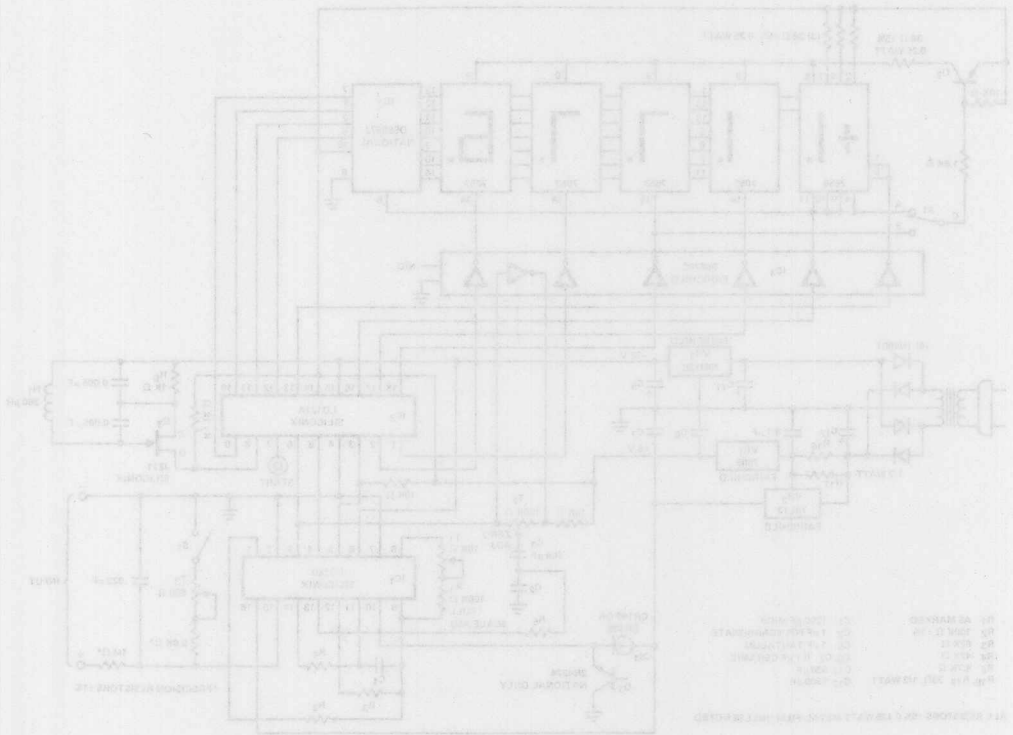
Typical Leakage Over Temperature
Figure 11



LD120/LD121A Grounding System
Figure 12

APPENDIX C: TROUBLESHOOTING

Problem	Causes
Jittery Display	f_{OSC} is not stable (short-term)
	AC voltage on V_{IN}, V_{HI-Q}, power supplies, or V_{REF}
	AC fields passing through unshielded circuit board
	R_1, R_2, or R_3 being carbon composition type
	Excessively small full-scale sensitivity implemented
	V_{AZ} or V_{REF} too small
Offset Drift	Excessive input resistance or C_{AZ} too small (see appendix A)
	Circuit board leakages excessive due to flux or moisture absorption
	A variable offset in grounding system
	Poor quality capacitors for C_{INT} or C_{AZ}
	Sample rate too slow (<1 sec)
	Thermocouple junctions in the 200 mV range
Poor Linearity	Poor quality C_{INT}
	V+ or V– less than 10 V
	Circuit board leakages to C_{INT}
	Noise pickup on U/D or loading of U/D
	V_{REF} modulated by display ground currents
No digit strobes from LD121A	Clock not functioning
	Some terminal of the LD121A more positive than V_{SS}



Siliconix

Design Aid of the LD120/LD121A 4½ Digit DVM

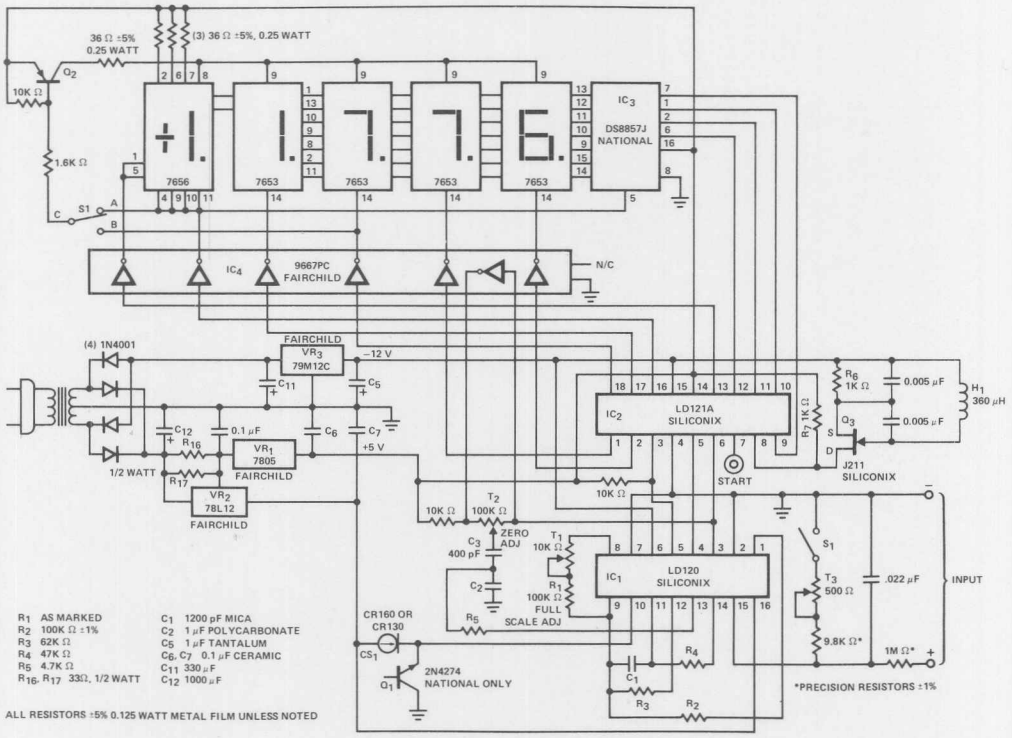
INTRODUCTION

The 4 1/2 Digit AC powered DVM schematic, P.C. board layout and parts list are intended to aid and speed the evaluation of the Siliconix LD120/LD121A precision A/D converter. As all converters of this resolution are sensitive to trace layout, this pattern demonstrates proper grounding and signal protection. A switchable 100:1 input signal divider is provided to enable the demonstrator to become a useful laboratory DVM after the evaluation of the system has been completed.

The metal pattern and component placement diagram are both printed to a 1:1 scale. The component placement art is intended to be silk-screened on the top side of the board to provide easy component installation. It can, however, be used simply as a loading diagram.

The demonstrator DVM features,

- ±1 count linearity
- 0.75 count LSD count stability (2 V scale)
- 1M Ω source impedance seen by converter input
- Auto Polarity
- Auto Zero cycle
- 200 mV F.S. range with:
 - less than 2 counts instability
 - ±1 count linearity
 - 10 μV resolution



CONSTRUCTION HINTS

1. A solid line between two holes represents a jumper wire.
2. A copper dot is placed by pin one of the IC's.
3. The dotted area denotes the power supply. If bench power supplies are available, connect to the pads marked +15 and −15. The positive source must supply 300 mA. The negative source must supply 30 mA.
4. The tab of the CR160 aligns to + mark.
5. The LD120 should be socket mounted.
6. The 2N4274 voltage reference must be selected for a reference voltage equal to or greater than 6.6 V. A 6.6 V to 6.8 V zener reference may be substituted.
7. The CR160 current source may be replaced with a 36K Ω resistor. Some degradation in stability and gain tempco may result.
8. The display board may be directly soldered to the circuit board, eliminating the edge connector.
9. C_3 is a mica dielectric.
 C_1 may be mica or polycarbonate dielectric.
 C_2, and C_6 may be mylar or polycarbonate dielectric.
 C_{10} is tantalum dielectric.
 C_{11} and C_{12} are electrolytic dielectric.
 C_4, C_5, C_7, C_8 and C_9 are ceramic disc capacitors.
10. All resistors are ±5% metal film unless otherwise noted.
11. Regulators VR_1 and VR_2 operate too hot to touch ≈ (85°C or 185°F)
12. Total power dissipation is 6 watts.
13. Break off steel screw tab from transformer nearest analog input. Connect other tab to earth ground wire from the power cord.
14. CLEAN BOARD THOROUGHLY after assembly. Any salts, finger oil, or solder flux remaining in analog circuitry may allow leakage currents detrimental to high quality performance.
15. LED displays are intensity coded. To avoid an unattractive display, check these codes for uniformity.

LAYOUT PRECAUTIONS

The following layout precautions have been taken and should be observed on the user's P.C. board:

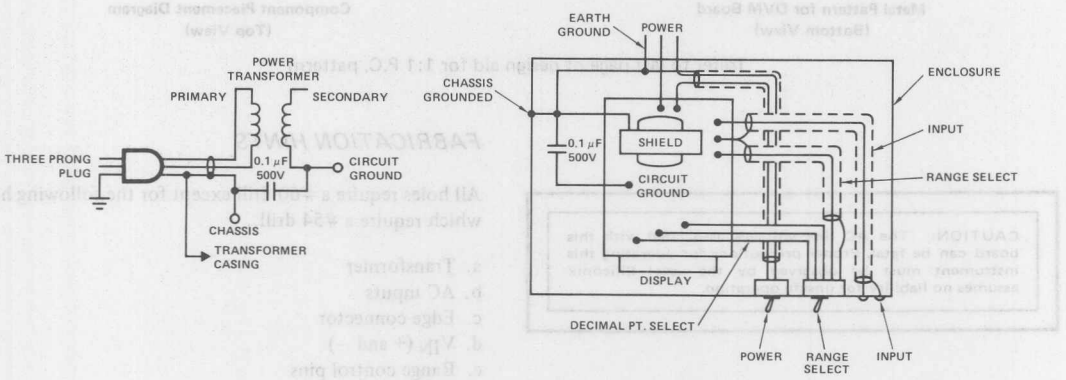
1. $V_{IN}^{(+)}$ trace is adjacent to ground only.
2. Traces from LD120 pins 9, 13, 15 are not adjacent to signal traces carrying AC signals.
3. U/D and comp. signals (LD120 pins 4 and 5) are separated by digital ground.
4. Digital circuitry ground paths return to the transformer (or power supply) via a different path than analog grounds from LD120.
5. The path from $V^{(-)}$ input to Hi-Quality ground (pin 2) does not carry any other currents.
6. The ground path from the reference and C_{STRG} (C_2) travel directly to Analog Ground (pin 7 of LD120).
7. Int Input (LD120, pin 9) node connections are kept short and compact. This node has a relatively high impedance and is therefore subject to AC line noise pick up.
8. The +5 V supply to the LD121A should not share a current path with the display currents.

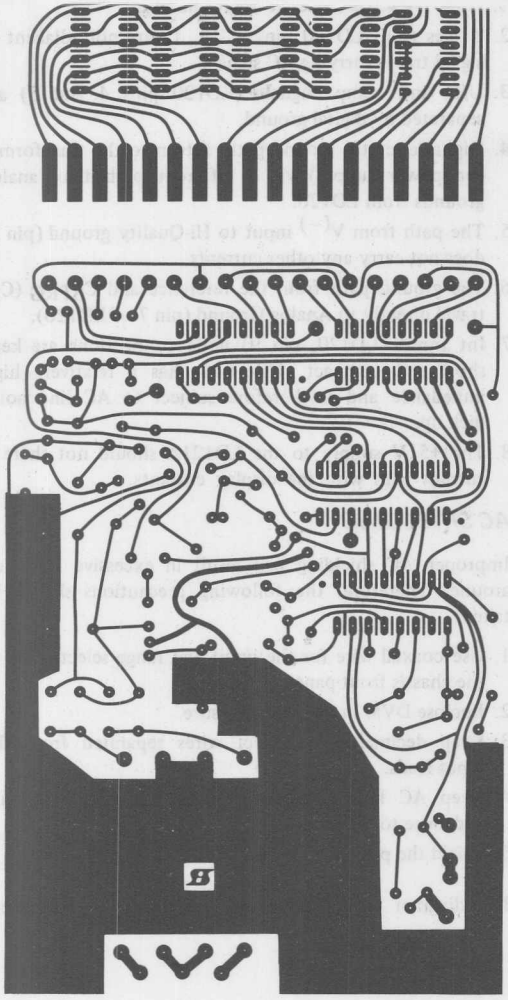
AC SHIELDING

Improper AC shielding will result in excessive LSD run around. Therefore, the following precautions should be taken:

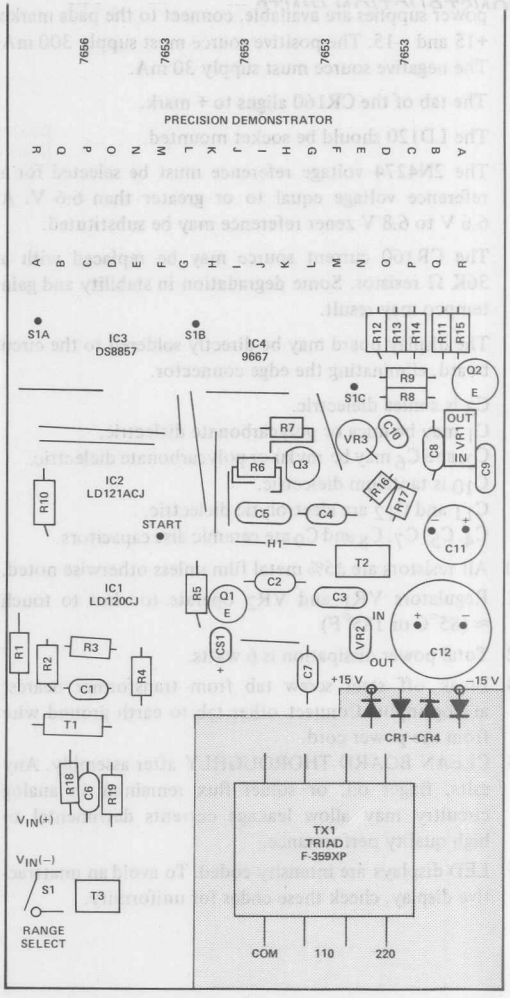
1. Use coaxial wire for the input and range select leads to the chassis front panel.
2. Enclose DVM in a metal enclosure.
3. Keep decimal point select wires separated from the input leads.
4. Keep AC line cord enclosed in box to a minimum and close to the chassis.
5. Shield the power switch leads with earth ground.

The diagram below illustrates good packaging practice:





Metal Pattern for DVM Board
(Bottom View)



Component Placement Diagram
(Top View)

(refer to last page of design aid for 1:1 P.C. pattern)

CAUTION: The AC line voltages associated with this board can be fatal. Proper precautions for operating this instrument must be observed by the user! Siliconix assumes no liability for unsafe operation.

FABRICATION HINTS

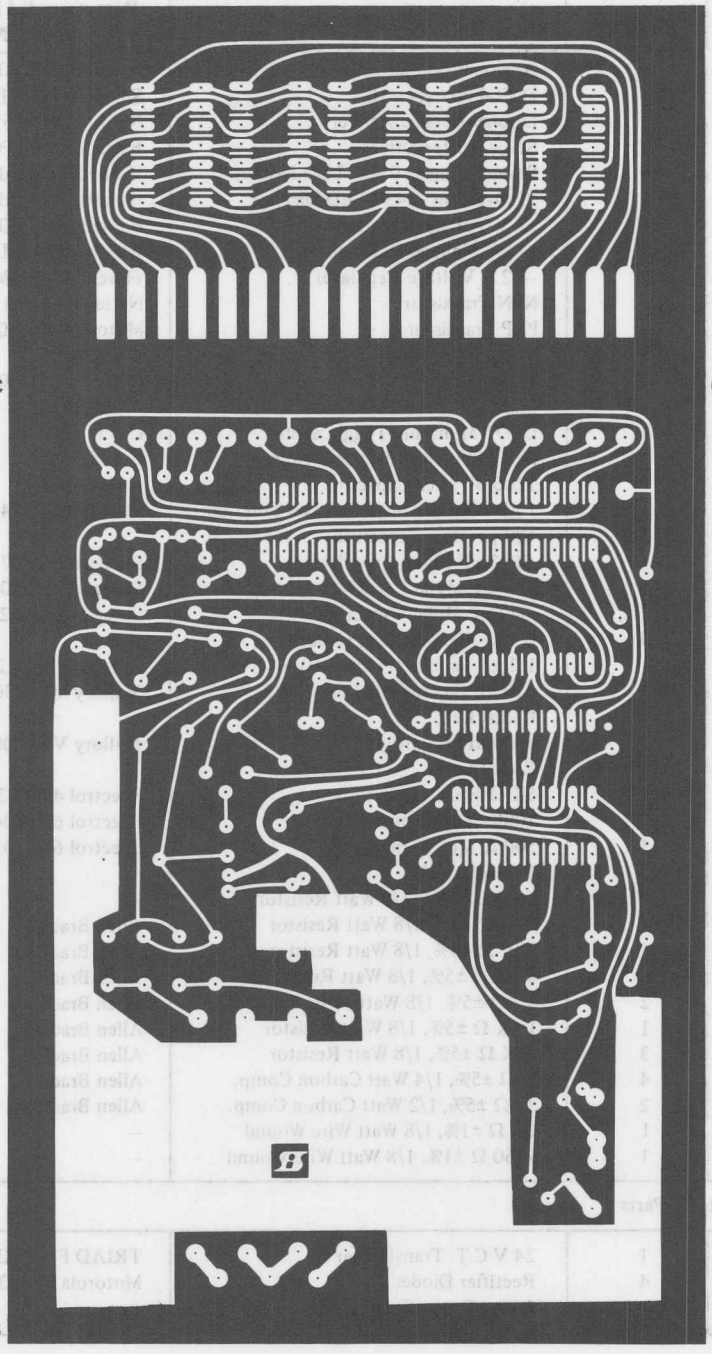
All holes require a #60 drill except for the following holes which require a #54 drill:

a. Transformer
b. AC inputs
c. Edge connector
d. V_{IN} (+ and –)
e. Range control pins
f. Decimal point select

Numbers	Quantity	Description	and Part Number
IC_1	1	Analog Processor IC	Siliconix LD120CJ
IC_2	1	Digital Processor IC	Siliconix LD121ACJ
IC_3	1	Display Decoder/Driver	National DS8857J
IC_4	1	Seven Buffer/Driver	Fairchild 9667PC
LED 1–4	4	Seven Segment 0.43" LED Display	Hewlett-Packard 5082-7653
LED 5	1	±1 Overflow 0.43" LED Display	Hewlett-Packard 5082-7656
VR_1	1	+5 V Voltage Regulator	Fairchild μA7805UC
VR_2	1	+12 V Voltage Regulator	Fairchild μA78L12AWC
VR_3	1	−12 V Voltage Regulator	Fairchild μA79M12HC
Q_1	1	NPN Transistor	National (Only) 2N4274
Q_2	1	PNP Transistor	Motorola 2N4402
Q_3	1	N-Channel JFET	Siliconix J211
CS_1	1	1.3 or 1.6 mA Current Source	Siliconix CR130 or CR160
H_1	1	360 μH Inductor ±5%	–
S_1	1	DPDT Miniature Toggle Switch	C & K 7201
S_2	1	SPST Miniature Toggle Switch	C & K 7101
C_1	1	1200 pF Mica Capacitor	–
C_2	1	1 μF Polycarbonate Stocked Foil Cap.	Siemens B32 541-1.00/5/100
C_3	1	400 pF Mica Capacitor	
C_4	1	.0047 μF Mylar Capacitor	Sprague 192P4729R8
C_5	1	.047 μF Mylar Capacitor	Sprague 192P504739R8
C_6	1	.022 μF Mylar Capacitor	Sprague 192P2239R8
C_{7-9}	3	0.1 μF Ceramic Disc Capacitor	–
C_{10}	1	1.2 μF Tantalum Cap – 10 V	Sprague 198D125X90225H1
C_{11}	1	330 μF Electrolytic Cap – 25 V Radial Lead	Mallory VTT330J25
C_{12}	1	1000 μF Electrolytic Cap – 25 V Radial Lead	Mallory VTT1000M25
T_1	1	5K Ω Multiturn Trimpot	Spectrol 43P502
T_2	1	100K Ω Multiturn Trimpot	Spectrol 64Y104
T_3	1	500 Ω Multiturn Trimpot	Spectrol 64Y501
–	2	Bannana Jacks	–
R_{1-2}	2	100K Ω ±1%, 1/8 Watt Resistor	–
R_3	1	62K Ω ±5%, 1/8 Watt Resistor	Allen Bradley
R_4	1	47K Ω ±5%, 1/8 Watt Resistor	Allen Bradley
R_5	1	4.7K Ω ±5%, 1/8 Watt Resistor	Allen Bradley
R_6, R_7	2	1K Ω ±5%, 1/8 Watt Resistor	Allen Bradley
R_8	1	1.6K Ω ±5%, 1/8 Watt Resistor	Allen Bradley
R_{9-11}	3	10K Ω ±5%, 1/8 Watt Resistor	Allen Bradley
R_{12-15}	4	36Ω ±5%, 1/4 Watt Carbon Comp.	Allen Bradley
R_{16-17}	2	33 Ω ±5%, 1/2 Watt Carbon Comp.	Allen Bradley
R_{18}	1	1M Ω ±1%, 1/8 Watt Wire Wound	–
R_{19}	1	9760 Ω ±1%, 1/8 Watt Wire Wound	–
AC Power Supply Parts			
TX 1	1	24 V C.T. Transformer	TRIAD F-359XP
CR_{1-4}	4	Rectifier Diodes	Motorola IN4002
–	1	3-Wire Power Cord w/Plug	–

Metal Pattern

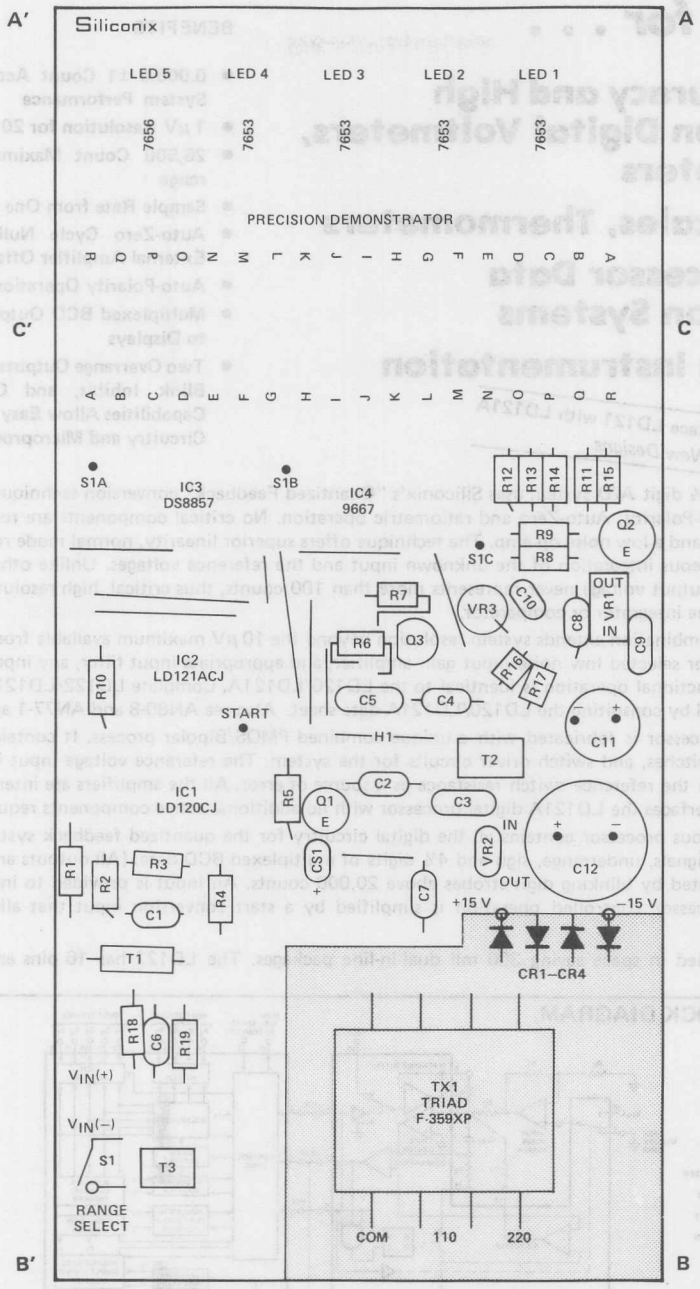
Scale 1:1



LD120/LD121A 4 1/2 Digit DVM

Component Placement Diagram

Scale 1:1



LD120/LD121A 4 1/2 Digit DVM

designed for . . .

- **High Accuracy and High Resolution Digital Voltmeters, Panel Meters**
- **Digital Scales, Thermometers**
- **Microprocessor Data Acquisition Systems**
- **Scientific Instrumentation**

BENEFITS

- 0.005% ±1 Count Accuracy, Ensures High System Performance
- 1 μV Resolution for 20 mV Full Scale
- 28,500 Count Maximum for 142% Overrange
- Sample Rate from One to Five/Second
- Auto-Zero Cycle Nulls Out Internal and External Amplifier Offsets
- Auto-Polarity Operation with One Reference
- Multiplexed BCD Output for Easy Interface to Displays
- Two Overrange Outputs, Underrange Output, Blink Inhibit, and Convert-On-Command Capabilities Allow Easy Interface to External Circuitry and Microprocessors

DESCRIPTION

Replace LD121 with LD121A for New Designs

The LD122/LD121A 4½ digit A/D system uses Siliconix's "Quantized Feedback" conversion technique. Intrinsic features of this system are Auto-Polarity, Auto-Zero and ratiometric operation. No critical components are required except for a stable voltage reference and a low noise op amp. The technique offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts, thus critical, high resolution performance is not required of either the integrator or comparator.

The LD122/LD121A combination extends system resolution beyond the 10 μV maximum available from the LD120/121A system. By adding a user selected low noise input gain amplifier, and appropriate input filter, any input resolution can be achieved. Otherwise functional operation is identical to the LD120/LD121A. Complete LD122/LD121A functional information may be obtained by consulting the LD120/LD121A data sheet. Also see AN80-8 and AN77-1 application notes.

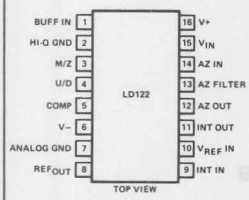
The LD122 analog processor is fabricated with a unique combined PMOS/Bipolar process. It contains all the necessary amplifiers, MOSFET switches, and switch driver circuits for the system. The reference voltage input is fully buffered on the LD122 to eliminate the reference switch resistance as a source of error. All the amplifiers are internally compensated. The LD122 directly interfaces the LD121A digital processor with no additional active components required.

The LD121A synchronous processor contains all the digital circuitry for the quantized feedback system. Device outputs supply two overrange signals, underrange, sign and 4½ digits of multiplexed BCD data. (All outputs are TTL compatible.) Overrange is also indicated by blinking digit strobes above 20,000 counts. An input is provided to inhibit this feature at user option. Microprocessor controlled operation is simplified by a start conversion input that allows conversion-on-command.

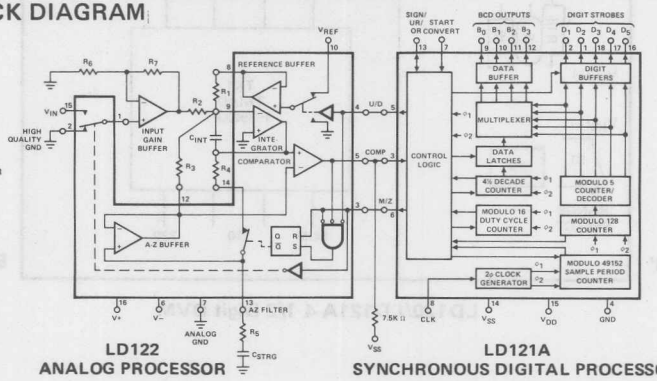
Both devices are supplied in space saving 300 mil dual-in-line packages. The LD122 has 16 pins and the LD121A has 18 pins.

FUNCTIONAL BLOCK DIAGRAM

Dual-In-Line Package



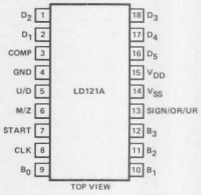
ORDER NO. LD122CJ
SEE PACKAGE 8



LD122
ANALOG PROCESSOR

LD121A
SYNCHRONOUS DIGITAL PROCESSOR

Dual-In-Line Package



ORDER NO. LD121ACJ
SEE PACKAGE 19

SWITCH STATES ARE FOR A LOGIC "0" AT U/D AND M/Z INPUTS

ABSOLUTE MAXIMUM RATINGS

V_{IN}(Pin 15, 2 LD122) $V- < V_{IN} < V+$
$V+ - V^-$ (LD122) 32 V
$V_{SS} - V_{DD}$ (LD121A) 20 V
Any Pin (LD121A) V_{DD} to V_{SS} ±0.3
V_{REF} +V

Operating Temperature 0 to 70°C
Storage Temperature −65 to 125°C
Power Dissipation (Package)* 750 mW

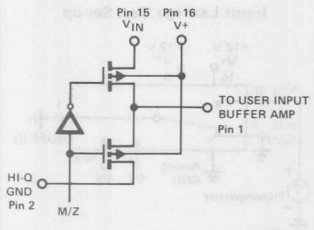
* Device mounted with all leads welded or soldered to PC Board. Derated 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS

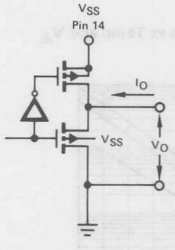
All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

			CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS UNLESS NOTED OTHERWISE $V+ = 12$ V; $V- = V_{DD} = -12$ V, $V_{SS} = 5$ V, $T_A = 25°C$
1	SYSTEM (Notes 2 and 3)		Linearity		−1	±1/4	1	Count	2 V Scale
					−2	±1/2	2		200 mV Scale
2			Noise (Note 1)			1/3	1	Count	2 V Scale
						1/2	2		200 mV Scale
3		NMRR				40		dB	f_L = 50 or 60 Hz
		PSRR				80			
4			Gain T.C.			5	15	ppm/°C	
5			Zero Drift			1	5	Count	T_A = 25 to 75°C, C_{STRG} = 1 µF, $R_{IN} \leq$ 100K Ω
6	LD121ACJ DIGITAL	POWER	V_{SS}		4.5	5	5.5	V	Range Over Which Functionality is Guaranteed
7			V_{DD}		−10.8	−12	−13.2		
8			I_{SS}	(Note 4)		14	25	mA	
9			I_{DD}			−14	−25		
10		INPUTS	V_{INH}	Comparator Input, Sign/UR/OR/ Blink (Note 5), Start, CLK IN	4.0			V	Guaranteed Input Threshold Voltages
11			V_{INL}				0.5		
12			I_{INH}	Sign/OR/UR (Note 5)		170	300	µA	V_{IN} = 5 V
13			I_{INL}	Start Convert, Clock		−150	−400		V_{IN} = 0 V
14		OUTPUTS	V_{OH}	Bit Lines, Sign/OR/UR Digit Strobes	2.4			V	I_{OH} = −40 µA
15			V_{OL}				0.6		I_{OL} = 1.6 mA
16			V_{OH}	M/Z	4.0				I_{OH} = −150 µA
17			V_{OL}				0.6		I_{OL} = 0.8 mA
18			V_{OH}	U/D	4.0				I_{OH} = −0.5 mA
19			V_{OL}				0.6		I_{OL} = 0.8 mA
20		DYN	tp	Start Convert (Note 6)	20			µs	
21			f_{CLK}		50		250	kHz	50% Duty Cycle
22				Rep Rate (Strobes)	78		470	Hz	$f_{CLK} \div 640$

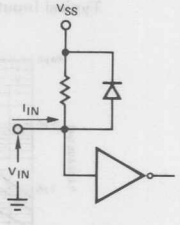
INPUT/OUTPUT SCHEMATICS



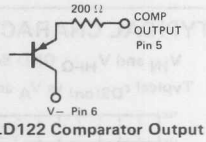
LD122 Input



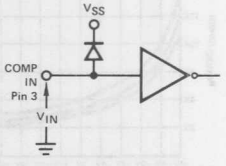
LD121A Output Buffers (Digits, Bits, Sign, M/Z U/D)



LD121A Clock Input Start Convert



LD122 Comparator Output



LD121A Comparator Input

ELECTRICAL CHARACTERISTICS (Cont'd)

			CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS UNLESS NOTED OTHERWISE V+ = 12 V; V– = V_{DD} = –12 V, V_{SS} = 5 V, T_A = 25°C
23	LD122CJ LINEAR	POWER	V+		9	12	15	V	
24			V–		–9	–12	–15		
25			I+				3.5	mA	
26			I–				–3		
27			I_{GND}		0		–2	mA	M/Z, U/D = 2.4 V
28		INPUT SWITCH	V_A	(Note 7)	–3		+3	V	
29			$r_{DS(on)}$	On Resistance, V_{IN} or Hi-Q Switches			5.5	kΩ	V_A = +1 V
30							8.0		V_A = –1 V
31			$I_{LEAKAGE}$	Leakage Current, Switch ON or OFF		2		pA	V_A = ±2.8 V
32									
33									
34		AZ BUFF	I_{SOURCE}			–100		μA	
35			I_{SINK}			800			
36			I_{STRG}			100		pA	T_A = 70°C
37			V_{OFFSET}		–50		50	mV	V_{OUT} = 0 V
38				Switch Resistance (on) (Note 8)		6	20	kΩ	V_{STRG} = –4 V, I_{DS} = 30 μA
39		REF BUF	I_{SOURCE}	Pin 8	–400	–800		μA	V_{IL} (U/D IN), = 0.8 V, V_O = 0 V
40			I_{SINK}	Pin 8		100			V_{IH} (U/D IN) = 2.0 V, V_O = 2 V
41		INT	I_{SOURCE}	(Note 9)	–50	–100		μA	V_{IN} (Int. IN) = –100 mV, V_O = 0 V
42			I_{SINK}		400	800			V_{IN} (Int. IN) = 100 mV, V_O = 0 V
43				Output Swing	–10		10	V	
44		COMP	V_{OUT}		–5			V	R_L = 10k to +5 V, AZ FILTER IN = 100 mV
45			V_{OFFSET}			±5		mV	INTEGRATOR OUT = 0 V
46			I_{IH}	M/Z, U/D Inputs			20	μA	V_{IH} = 2.0 V
47			I_{IL}				–100	μA	V_{IL} = 0.8 V

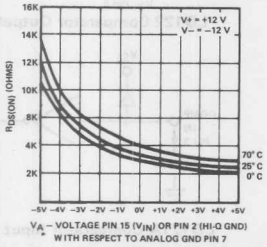
Typical values are for Design Aid Only, not guaranteed and not subject to production testing. LD122 - CMAM-C LD121A - IPDC VI

NOTES:

1. Bit width over which reading is stable 95% of the time.
2. System Parameters are not directly tested.
3. f_{CLK} = 163.84 kHz, V_{REF} = 6.8 V.
4. All outputs disconnected.
5. Pin characteristic only during D_4 strobe time.
6. Minimum positive going pulse width to initiate a conversion.
7. Maximum voltage range for V_{INPUT} (pin 1) or hi-quality GND (pin 2).
8. V_{STRG} must be more positive than –4 volts.
9. Reference Source Impedance must be less than 10K Ω.

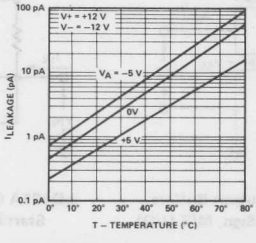
TYPICAL CHARACTERISTICS

V_{IN} and $V_{Hi\text{-}Q}$ GND Switches Typical $r_{DS(on)}$ vs V_A and Temp



V_A – VOLTAGE PIN 15 (V_{IN}) OR PIN 2 (HI-Q GND) WITH RESPECT TO ANALOG GND PIN 7

Typical Input Leakage vs Temp and V_A



Input Leakage Test Set-up

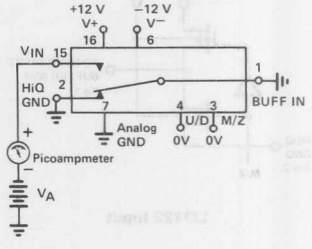
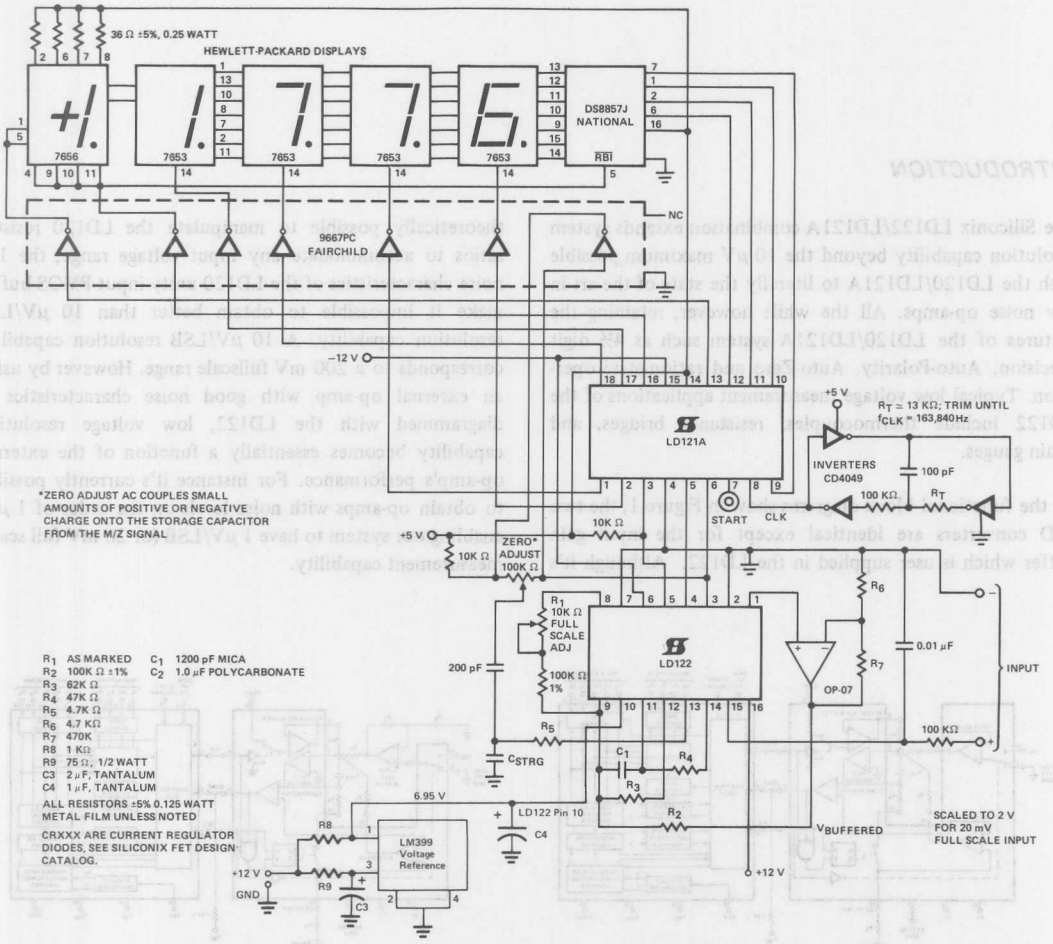


Figure 1 shows the arrangement for a 20 mV full scale, 1 μV resolution DVM. The OP-07 provides the necessary low noise operation to achieve stable 1 μV readouts. Proper layout is necessary for the LD122 and OP-07 front end circuitry to reduce stray RF and hum pickup. Having the OP-07 included in the Auto-zero loop cancels front end amplifier bias-offsets, and more important drift with temperature. Reference drift is reduced by using an LM399 precision voltage reference with built in heater.

CIRCUIT BENEFITS

- 1 μV Resolution
- Overrange Blinking
- 0 → 19.999 mV Input Voltages
- Zero Adjust to Null Offset Introduced by PC Board Leakages and Comparator

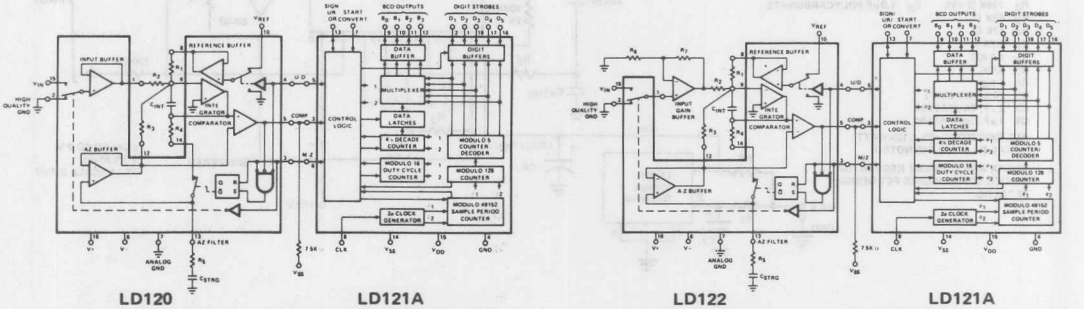


Function/Application of the LD122/LD121A ±4½ Digit A/D Converter Set in Measurement Systems

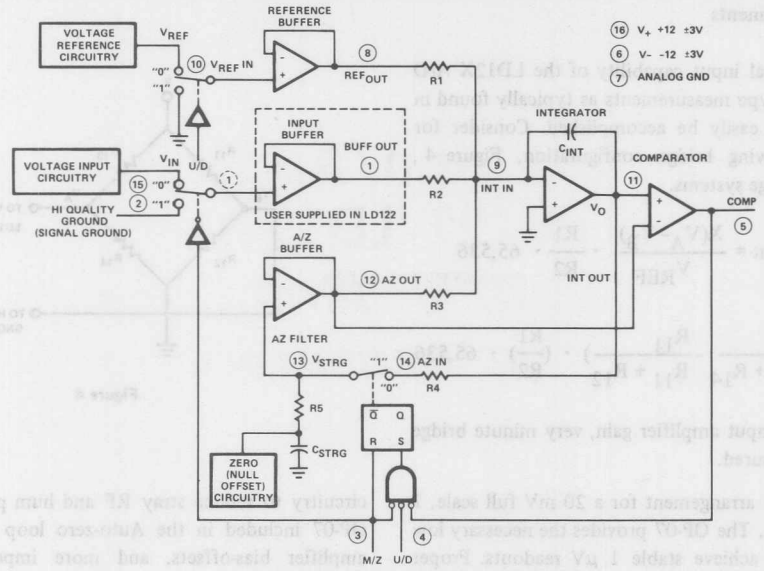
INTRODUCTION

The Siliconix LD122/LD121A combination extends system resolution capability beyond the 10 μV maximum possible with the LD120/LD121A to literally the state of the art in low noise op-amps. All the while however, retaining the features of the LD120/LD121A system such as 4½ digit precision, Auto-Polarity, Auto-Zero and ratiometric operation. Typical low voltage measurement applications of the LD122 include thermocouples, resistance bridges, and strain gauges.

As the functional block diagrams show in Figure 1, the two A/D converters are identical except for the input gain buffer which is user supplied in the LD122. Although it's theoretically possible to manipulate the LD120 resistor ratios to accommodate any input voltage range, the 1/F noise characteristics of the LD120 unity input PMOS buffer make it impossible to obtain better than 10 μV/LSB resolution capability. A 10 μV/LSB resolution capability corresponds to a 200 mV fullscale range. However by using an external op-amp with good noise characteristics as diagrammed with the LD122, low voltage resolution capability becomes essentially a function of the external op-amp's performance. For instance it's currently possible to obtain op-amps with noise levels on the order of 1 μV, enabling our system to have 1 μV/LSB (or 20 mV full scale) measurement capability.



Switch States are for a Logic "0" at U/D and M/Z Inputs
Figure 1



Analog Processor Expansion Diagram
Figure 2

Since the LD122/LD121A converter is essentially a LD120/LD121A system suitably modified (in Figure 2) and numerous dissertations on the quantized feedback technique can be found in the Siliconix LSI Data Book, discussion of basic converter operation will be foregone in favor of specific precautions, guidelines and applications to follow when doing very low voltage measurements. For those desiring basic operational information I refer you to the LD120/LD121A data sheet and application note AN77-1.

APPLICATIONS INFORMATION

Features and Applications

With its long list of high performance features:

- Wide choice of input voltage ranges
- High resolution 4½ digit operation
- 0.005% ± 1 count accuracy
- Highly linear operation with simultaneous unknown-reference integration
- Auto Polarity operation with only 1 external reference
- Fully buffered inputs
- TTL output drive
- Automatic Zeroing cycle

Applications Tailor Made for the LD122/LD121A include:

- Microvolt Digital Volt Meters
- Thermocouple Temperature Measurement Systems
- High Precision strain gauge measurement systems
- Scientific Instrumentation and others

LD122-LD120 Similarities

Probably the best way to think of the LD122 is as if it were an LD120 with the V_{IN} input amplified. So anywhere you see an expression for the differential LD120 input (V_{IN}-V_{HI-Q}) substitute X(V_{IN}-V_{HI-Q}) where X is the gain of the user supplied input buffer. Doing so, our A/D output count relation becomes:

$$\text{Output Count} = \frac{X(V_{IN}-V_{HI-Q})}{V_{REF}} \cdot \frac{R1}{R2} \cdot 65{,}536$$

Now in addition to being able to scale the converter for different input ranges by changing the R1/R2 ratio, we can also alter the input buffer gain = X.

Figure 3 shows a typical application of the LD122/LD121A chip set. The system is set up to indicate full scale if 2V (100 μV/LSB) is applied to R2 by the input gain buffer. However the input gain X is 100 so that a 20mV (1μV/LSB) signal applied to the input buffer results in a fullscale reading. If the input gain were only 10, then a 200mV (10μV/LSB) signal would be necessary to cause a full scale reading.

Differential Measurements

Using the differential input capability of the LD12X A/D series, ratiometric type measurements as typically found in bridge circuits can easily be accomplished. Consider for example the following bridge configuration, Figure 4, typical of strain gauge systems.

$$\text{where Output Count} = \frac{X(V_A - V_B)}{V_{REF}} \cdot \frac{R1}{R2} \cdot 65{,}536$$

$$= X\left(\frac{V}{V_{REF}}\right)\left(\frac{R_{14}}{R_{13}+R_{14}} - \frac{R_{11}}{R_{11}+R_{12}}\right) \cdot \left(\frac{R1}{R2}\right) \cdot 65{,}536$$

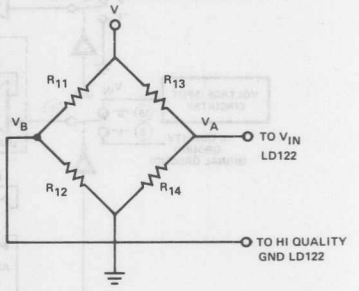


Figure 4

Using appropriate input amplifier gain, very minute bridge changes can be measured.

Figure 3 shows the arrangement for a 20 mV full scale, 1 μV resolution DVM. The OP-07 provides the necessary low noise operation to achieve stable 1 μV readouts. Proper layout is necessary for the LD122 and OP-07 front end circuitry to reduce stray RF and hum pickup. Having the OP-07 included in the Auto-zero loop cancels front end amplifier bias-offsets, and more important drift with temperature.

CIRCUIT BENEFITS

- 1 μV Resolution
- Overrange Blinking
- 0 → 19.999 Input Voltages
- Zero Adjust to Null Offset Introduced by PC Board Leakages and Comparator

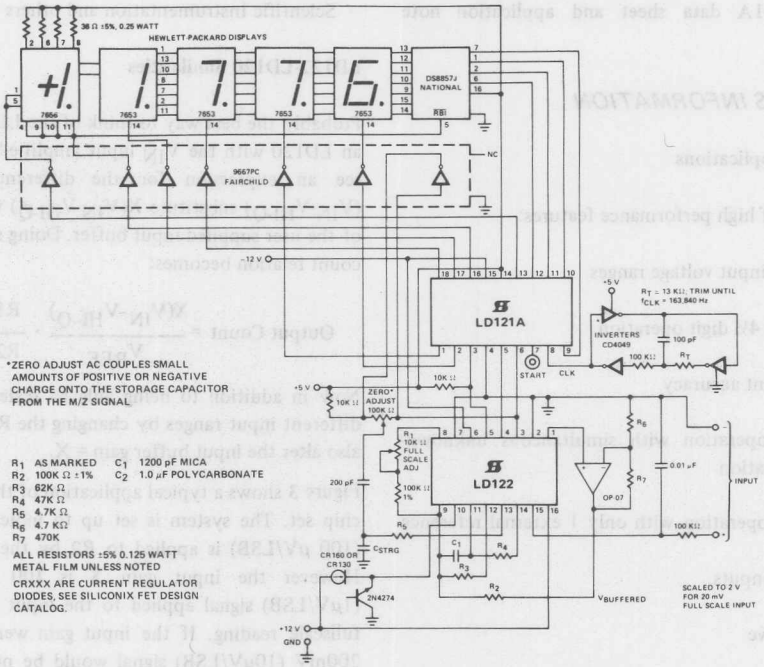
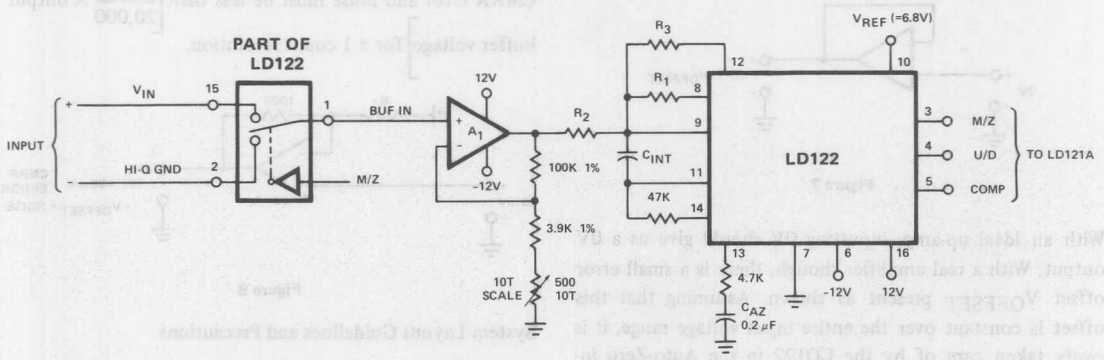


Figure 3

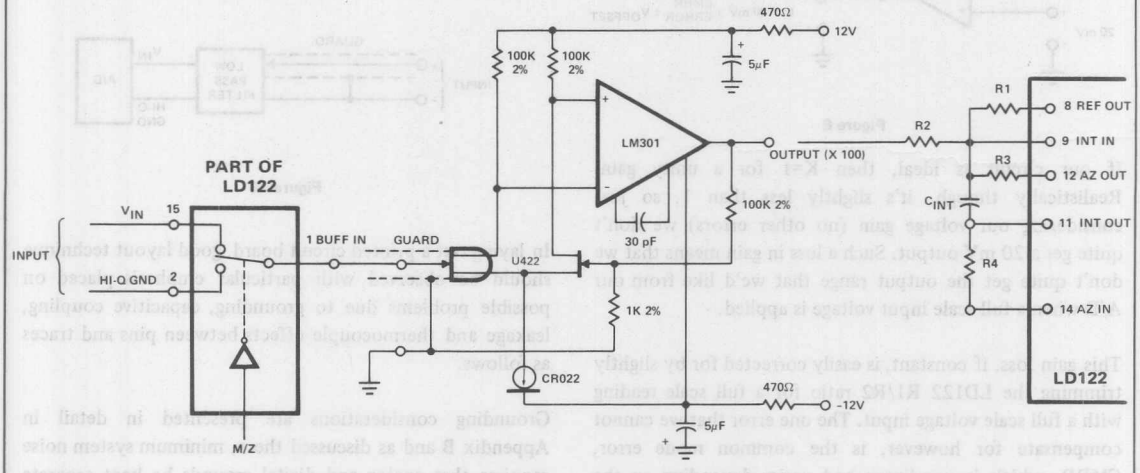
Input Gain Buffers

Figure 5 shows the arrangement for a 20 mV full-scale front end. If an extremely low source impedance were used, such as thermocouple, then an amplifier such as the LM201A could be used for A_1. For higher impedances, lower bias currents are required until at about 1K Ω or above, a JFET amplifier will be required. Note that MOS input op-amps are not quiet enough.

Even the BI-FET op-amps are only good for a 20K Ω input resistance up to 75°C. The circuit of Figure 6 has an input leakage of only 2 pA typical at 75°C and would be usable with 1M Ω input resistance. Although not covered here, there are ways to reduce leakage effects over temperature by a factor approaching 10.



20 mV F.S. Meter (Front End)
Figure 5



Ultra-Low-Leakage Preamp
Figure 6

Input Buffer Selection Considerations

common mode voltage, prohibit such an ideal situation and must be reckoned with when choosing an op-amp.

Consider first of all the following unity gain voltage follower configuration in Figure 7.

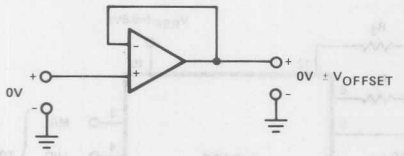


Figure 7

With an ideal op-amp, inputting 0V should give us a 0V output. With a real amplifier though, there is a small error offset V_{OFFSET} present as shown. Assuming that this offset is constant over the entire input voltage range, it is easily taken care of by the LD122 in the Auto-Zero interval where such error offsets are easily corrected for.

Suppose that we now input a 20 mV signal to our unity buffer. See Figure 8.

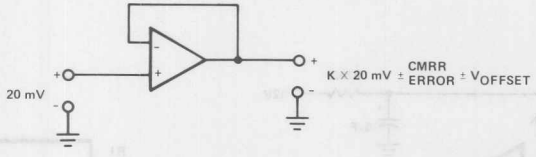


Figure 8

If our circuit is ideal, then K=1 for a unity gain. Realistically though, it's slightly less than 1, so just considering our voltage gain (no other errors) we don't quite get a 20 mV output. Such a loss in gain means that we don't quite get the output range that we'd like from our A/D when a full scale input voltage is applied.

This gain loss, if constant, is easily corrected for by slightly trimming the LD122 R1/R2 ratio for a full scale reading with a full scale voltage input. The one error that we cannot compensate for however, is the common mode error, CMRR, which is non-linear and varies depending on the input-voltage. This being the case, we'd like the maximum error attributable to CMRR to be less than 1 count of the A/D. If we were using the above buffer with an LD122/LD121A to measure down to 1 μV/(count or LSB) (20 mV range) then the maximum CMRR error must be less than 1 μV.

CMRR error must be less than $\frac{1}{20{,}000} \cdot 2V$ (i.e. for ± 1 count operation CMRR better than 86 dB over the input voltage range) or 100 μV over the entire voltage range. If noise is significant, (thermal, junction, etc.) the sum of CMRR error and noise must be less than $\left[\frac{1}{20{,}000} \times \text{output buffer voltage}\right]$ for ± 1 count resolution.

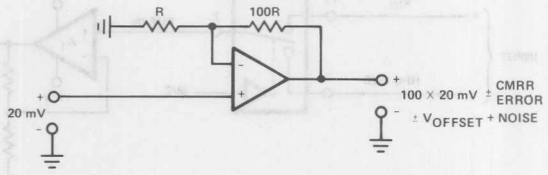


Figure 9

System Layout Guidelines and Precautions

When operating in the microvolt region extreme care must be taken with system layout and component selection, particularly in the front end, to minimize stray noise pick up. For instance the voltage inputs to the A/D should be shielded and put through a low pass filter as illustrated in Figure 10.

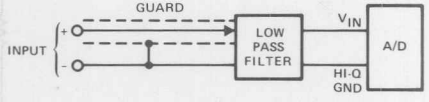


Figure 10

In laying out a printed circuit board, good layout technique should be observed with particular emphasis placed on possible problems due to grounding, capacitive coupling, leakage and thermocouple effects between pins and traces as follows.

Grounding considerations are presented in detail in Appendix B and as discussed there, minimum system noise requires that analog and digital grounds be kept separate until terminated at the power supply.

Capacitive coupling and leakage problems are particularly noticeable with the LD122 analog chip, but can be minimized through the use of a 2 sided glass-epoxy board, with guard traces driven from low impedance sources. Of foremost concern with the LD122 is capacitive coupling between pins 4 (U/D in) and 5 (COMP out) as diagrammed in the chip pin out below. As shown, a digital ground trace between pins 4 and 5 is recommended to reduce these inter-pin effects. The general rule of thumb to follow here is to guard [high impedance analog inputs and pulse width critical digital waveforms] from [voltage supplies and digital signals] by driving [the guard rings and traces] with [low impedance sources having potentials close to the guarded pins].

Following this approach it might also be wise to isolate pin 10 ($V_{REF}IN$) with traces from pin 8 (REF_{OUT}) and pin 13 (A/Z filter) with a trace from pin 12 (A/Z out) as shown in Figure 11.

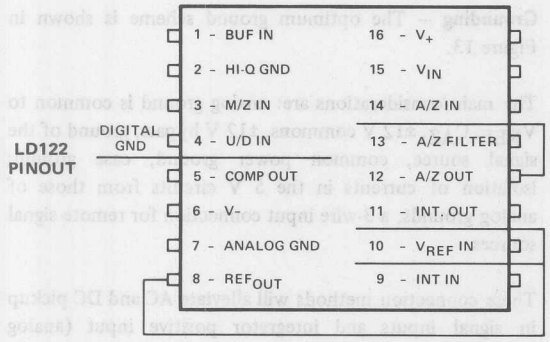


Figure 11

Down in the microvolt region ordinarily insignificant sources of noise can become major problems unless adequately accounted for in the system layout. Probably the most insidious of which are thermal effects in the form of thermocouple junctions and board temperature gradients. Recall that 2 dissimilar metals placed together form a thermocouple junction and when heated can supply a small output voltage. Even at room temperature the effects are appreciable in the microvolt region and numerous junctions are possible on a circuit board where we go from gold plated edge connector to tin plated copper trace to solder to kovax IC lead to semiconductor interface. Board temperature gradients can effect minute resistance and thermocouple changes resulting in unequal voltage potentials and noise over even the most carefully balanced signal paths. Therefore, layout in terms of optimum package placement, minimum input lead length and minimizing temperature gradients should be considered. Generally speaking, the input gain buffer as well as any input circuitry should be electrically and thermally shielded for best results.

In any measurement application component quality and stability is always a question and a few words concerning LD122 resistor and capacitor selection are appropriate here. Ordinarily R1 and R2 quality are critical to proper circuit operation and they and any accompanying trimming components are recommended to be wirewound or metal film since carbon and oxide film resistors can generate large amounts of thermal noise.

In addition, since we are talking about gain setting resistances, they should track each other over the operational temperature range lest a gain error result.

When a user supplied input buffer of appreciable gain is used, the burden of quality becomes shifted to the input buffer components since any noise there is appreciably magnified, while R2 now faces a large input signal in relation to its possible noise contribution. The gain setting resistors must therefore be of appropriate quality. In either case, resistor quality should be appropriate to its relative noise contribution.

The integrator capacitor C_{INT} should be mylar or better quality. The autozero capacitor C_{STRG} should be mylar, polystyrene, polycarbonate, or polyproplene, the latter being best with regards to dielectric absorption. Resistors R3, R4, R5 quality is not critical, but should be long term stable. Above all, capacitive losses (leakage, dielectric absorption, etc.) must be kept to a minimum for proper operation as Appendix A explains.

APPENDICES

APPENDIX A: ERROR TERMS

Zero Drift – The main source of zero drift is leakage from the input and auto zero buffers. Figure 12 shows typical input and auto zero leakages over temperature. The error component due to I_{IN} is simply

$$\Delta V_{IN} = \Delta I_{IN} \cdot R_{SOURCE}$$

For a 1M Ω input resistance, and ΔI_{IN} = 30 pA at 75°C, ΔV_{IN} = 30 μV, corresponding to a 0.3 bit offset at 2 V full-scale, and 3 count offset at 200 mV full-scale. This offset can be reduced by reducing R_{SOURCE} or by inserting a compensating R_{SOURCE} between $V_{HI\text{-}Q}$ and ground.

The drift due to I_{AZ} is independent of scale factor, and is caused by the voltage on C_{AZ} drifting during the measure interval. The magnitude of drift will be

$$\Delta V_{AZ} = \frac{I_{AZ} \cdot T_{MEASURE}}{C_{AZ}} = \frac{I_{AZ} \cdot 32{,}768}{C_{AZ} \cdot f_{OSC}}$$

This will cause an effective input current to the integrator of $\Delta V_{AZ}/2R_3$, the factor two resulting from the fact that the ramp of auto-zero drift is averaged by the algorithm. This input current due to drift is analogous to an input signal of $\Delta V_{AZ}\, R_2/2R_3$, so the count drift is

$$\Delta\text{Count} = \frac{\Delta I_{AZ}}{C_{AZ} f_{OSC} V_{REF}} \cdot \frac{R_1}{2R_3} \cdot 2.15 \times 10^9$$

So given ΔI_{AZ} = 100 pA when up at 70°C, R_1 = 60K = R_3, C_{AZ} = 0.1 μF, f_{OSC} = 150KHz, and V_{REF} = 6.2 V, ΔCount = 1.16 due to ΔI_{AZ} only.

The drift caused by thermocouple junctions on the LD120 is much less than that caused by leakages.

Gain Drift – Full-scale gain drift is caused mainly by changes in V_{REF}. One count in 20,000 stability per degree C is 50 ppm/°C, so the zener reference should have at least 10 ppm/°C stability and the system burned-in to reduce long term drift.

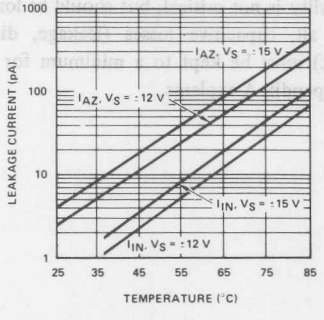
The resistors at R_2 and R_1 should track each other over temperature at least as well as the tempco of the reference.

APPENDIX B

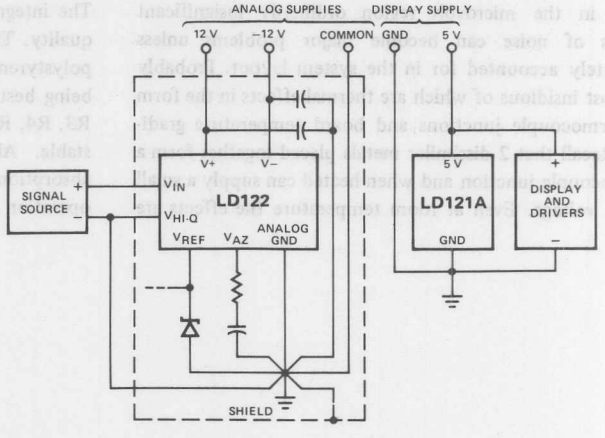
Grounding – The optimum ground scheme is shown in Figure 13.

The main considerations are: analog ground is common to V_{REF}, C_{AZ}, ±12 V commons, ±12 V bypass, ground of the signal source, common power ground, case ground; isolation of currents in the 5 V circuits from those of analog grounds; a 3-wire input connection for remote signal sources.

These connection methods will alleviate AC and DC pickup in signal inputs and integrator positive input (analog ground) from noise currents caused by the display and AC environment.



Typical Leakage Over Temperature
Figure 12



LD120/LD121A Ground System
Figure 13

APPENDIX C: TROUBLESHOOTING

Problem	Causes
Jittery Display	f_{OSC} is not stable (short-term)
	AC voltage on V_{IN}, V_{HI-Q}, power supplies, or V_{REF}
	AC fields passing through unshielded circuit board
	R_1, R_2, or R_3 being carbon composition type
	Excessively small full-scale sensitivity implemented
	V_{AZ} or V_{REF} too small
	Insufficient power supply bypass capacitor
Offset Drift	Excessive input resistance or C_{AZ} too small (see appendix A)
	Circuit board leakages excessive due to flux or moisture absorption
	A variable offset in grounding system
	Poor quality capacitors for C_{INT} or C_{AZ}
	Sample rate too slow (<1 sec)
	Thermocouple junctions in the 200 mV range
Poor Linearity	Poor quality C_{INT}
	V+ or V– less than 10 V
	Circuit board leakages to C_{INT}
	Noise pickup on U/D or loading of U/D
	V_{REF} modulated by display ground currents
No digit strobes from LD121A	Clock not functioning
	Some terminal of the LD121A more positive than V_{SS}

	AC voltage on V_{IN}, V_{HI-Q} power supplies, or V_{REF}
	AC fields passing through unshielded circuit board
	R_1, R_2, or R_3 being carbon composition type
	Excessively small full-scale sensitivity implemented
	V_{AZ} or V_{REF} too small
	Insufficient power supply bypass capacitor
Offset Drift	Excessive input resistance or C_{AZ} too small (see appendix A)
	Circuit board leakages excessive due to flux or moisture absorption
	A variable offset in grounding system
	Poor quality capacitors for C_{INT} or C_{AZ}
	Sample rate too slow (<1 sec)
	Thermocouple junctions in the 200 mV range
Poor Linearity	Poor quality C_{INT}
	V_+ or V_- less than 10 V
	Circuit board leakages to C_{INT}
	Noise pickup on U/D or loading of U/D
	V_{REF} modulated by display ground currents
No digit strobes from LD1211A	Clock not functioning
	Some terminal of the LD1211A more positive than V_{SS}

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D/A CONVERTERS

Title	Page
DG515/DG516	8-1

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D/A Converter Switches

Siliconix

designed for . . .

- **4, 10 or 14 Bit DACs**
- **Binary or BCD DACs**
- **Multiplying DACs**
- **Successive Approximation ADC**
- **Frequency Synthesizers**
- **Virtual Ground Switches**

BENEFITS

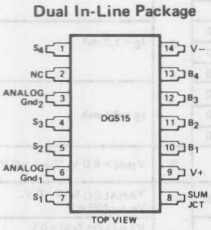
- **Easily Interfaced**
 - Binary Weighting of ON Resistances
- **Minimizes System Power Requirements**
 - 40 μW Operating Power
- **Reduces Systems Costs**
 - Single Supply Operation

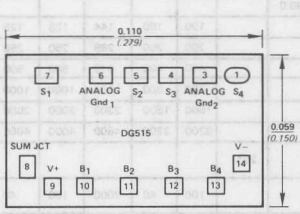
DESCRIPTION

The DG515 and DG516, 4 and 10 bit SPDT switches, combine NMOS analog switches with CMOS switch drivers. These switches feature low channel ON resistance, binary weighting of ON resistance and channel resistance matching to minimize the errors that can lead to non-monotonicity in D/A converters. The binary ON resistance weighting (doubling for each bit) is continued from the DG515 to the DG516 to allow the pair to be used as a 14 bit DAC.

PIN CONFIGURATIONS/BONDING DIAGRAMS

Dual In-Line Package

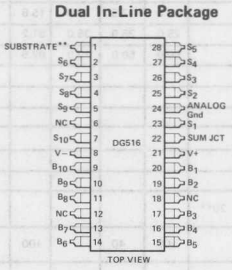


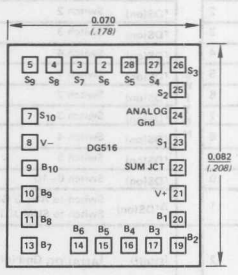


ORDER NUMBERS:
DG515AP
DG515BP
SEE PACKAGE 11
DG515CJ
SEE PACKAGE 7

*** ORDER NUMBERS:**
DG515ADICE
DG515BDICE
DG515CDICE

Dual In-Line Package





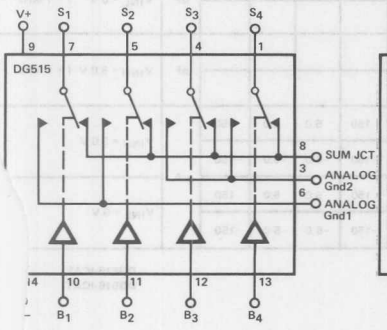
ORDER NUMBERS:
DG516AR
DG516BR
SEE PACKAGE 13
DG516CJ
SEE PACKAGE 14

*** ORDER NUMBERS:**
DG516ADICE
DG516BDICE
DG516CDICE

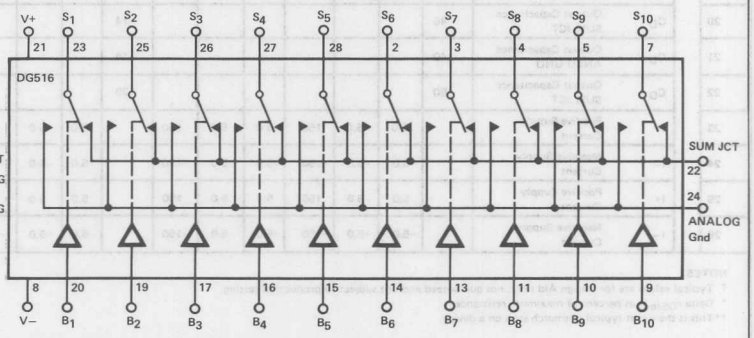
* CONTACT FACTORY FOR TESTING AND INSPECTION CRITERIA
** SHOULD BE LEFT UNCONNECTED OR CAN BE TIED TO V^+

FUNCTIONAL DIAGRAMS

DG515



DG516



SWITCH STATES ARE FOR LOGIC "1" INPUT

I_{SWITCH}	10 mA
Current (Any Terminal Except Switch)	30 mA
Storage Temperature (A & B Suffix)	−65 to 150°C
(C Suffix)	−65 to 125°C
Operating Temperature	
(A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
(C Suffix)	0 to 70°C
Power Dissipation (Package)*	
14 Pin Ceramic DIP**	825 mW
14 Pin Plastic DIP***	470 mW

"Device mounted with all leads welded or soldered to PC board

**Derate 11 mW/°C above 70°C

***Derate 6.3 mW/°C above 25°C

****Derate 10 mW/°C above 25°C

*****Derate 8.3 mW/°C above 25°C

†NOTE: Exceeding these voltage limits can result in a latch-up condition, excessive I+ and possible destruction to the device. Placing a 2K Ω resistor in series with V+ will protect the device and allow recovery (without power supply cycling) after the overvoltage is removed.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters to assure conformance with specifications. DICE are sorted by DC parameter tests and visual inspections.

		Characteristic		DG515	DG515 MAX LIMITS						DG516	DG516 MAX LIMITS						Unit	Test Conditions V+ = 8.0 V, V− = 0 V
					DG515A/B			DG515C				DG516A/B			DG516C				
				Typ† @ 25°C	−55°C To −20°C	25°C	125°C To 85°C	0°C	25°C	70°C	Typ† @ 25°C	−55°C To −20°C	25°C	125°C To 85°C	0°C	25°C	70°C		
1	SWITCH	$r_{DS(on)}$	Switch 1		6.25	6.25	9.0	7.8	7.8	11.2								Ω	I_S = 10 mA
2	SWITCH	$r_{DS(on)}$	Switch 2		12.5	12.5	18.0	15.6	15.6	22.5									
3	SWITCH	$r_{DS(on)}$	Switch 3		25.0	25.0	36.0	31.2	31.2	45.0									
4	SWITCH	$r_{DS(on)}$	Switch 4		50.0	50.0	72.0	62.5	62.5	90.0									
5	SWITCH	$r_{DS(on)}$	Switch 1									100	100	144	125	125	180		I_S = 1.0 mA
6	SWITCH	$r_{DS(on)}$	Switch 2									200	200	288	250	250	360		
7	SWITCH	$r_{DS(on)}$	Switch 3									400	400	576	500	500	720		
8	SWITCH	$r_{DS(on)}$	Switch 4									800	800	1150	1000	1000	1440		I_S = 0.1 mA
9	SWITCH	$r_{DS(on)}$	Switch 5									1600	1600	2300	2000	2000	2880		
10	SWITCH	$r_{DS(on)}$	Switch 6–10									3200	3200	4600	4000	4000	5760		
11	SWITCH	$\Delta r_{DS(on)}$	Switch to ANLG GND Switch to SUM JCT	20**							20**							%	V_{INH} = 8.0 V, V_{INL} = 0 V
12	SWITCH	$I_{D(off)}$	$I_{ANALOG\ Gnd\ (off)}$		100	40		100	40			100	40	2000	100	40	2000	nA	$V_{ANALOG\ Gnd}$ = 0 V, V_S = −100 mV
							2000			2000								nA	$V_{ANALOG\ Gnd}$ = 0 V, V_S = −20 mV
13	SWITCH	$I_{D(off)}$	$I_{SUMMING\ Junction\ (off)}$		100	40		100	40			100	40	2000	100	40	2000		$V_{SUMMING\ Jct}$ = 0 V, V_S = +100 mV
							2000			2000									$V_{SUMMING\ Jct}$ = 0 V, V_S = +20 mV
14	INPUT	V_{IN}	Threshold	4.0							4.0							V	
15	INPUT	I_{INL}	Input Current Input Voltage Low		−1.0	−1.0	−1.0	−1.0	−1.0	−1.0		−1.0	−1.0	−1.0	−1.0	−1.0	−1.0	μA	V_{INL} = 0 V
16	INPUT	I_{INH}	Input Current Input Voltage High		+1.0	+1.0	+1.0	+1.0	+1.0	+1.0		+1.0	+1.0	+1.0	+1.0	+1.0	+1.0		V_{INH} = 8.0 V
17		t_{on}	Turn-ON Time			120			180				120			180		ns	See Switching Time Test Circuit
18		t_{off}	Turn-OFF Time			170			250				170			250			
19		C_D	Output Capacitance ANLG GND	60							20							pF	V_{INL} = 0 V f = 1 MHz
20		C_D	Output Capacitance SUM JCT	40							14								
21		C_D	Output Capacitance ANLG GND	40							14							pF	V_{INH} = 8.0 V f = 1 MHz
22		C_D	Output Capacitance SUM JCT	60							20								
23		I+	Positive Supply Current		5.0	5.0	150	5.0	5.0	150		5.0	5.0	150	5.0	5.0	150	μA	V_{INH} = 8.0 V
24		I−	Negative Supply Current		−5.0	−5.0	−150	−5.0	−5.0	−150		−5.0	−5.0	−150	−5.0	−5.0	−150		
25		I+	Positive Supply Current		5.0	5.0	150	5.0	5.0	150		5.0	5.0	150	5.0	5.0	150		V_{INL} = 0 V
26		I−	Negative Supply Current		−5.0	−5.0	−150	−5.0	−5.0	−150		−5.0	−5.0	−150	−5.0	−5.0	−150		

NOTES:

† Typical values are for Design Aid only, not guaranteed and not subject to production testing.

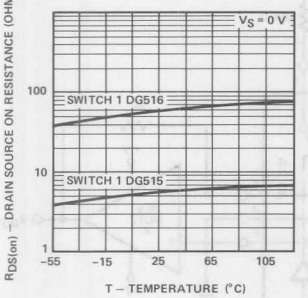
* Delta $r_{DS(on)}$ as percent of maximum resistance.

** This is the worst typical mismatch seen on a device.

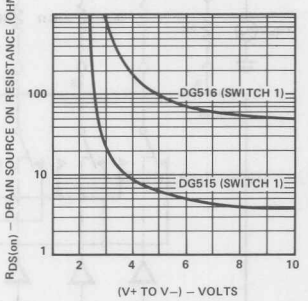
DG515-ICAS
DG516-ICAT

TYPICAL CHARACTERISTICS

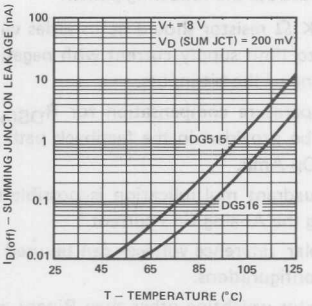
$R_{DS(on)}$ vs Temperature



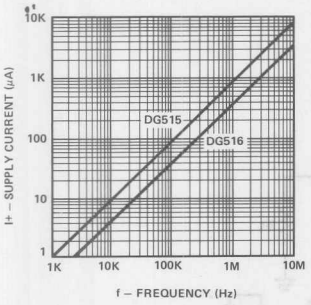
$R_{DS(on)}$ vs Supply Voltage



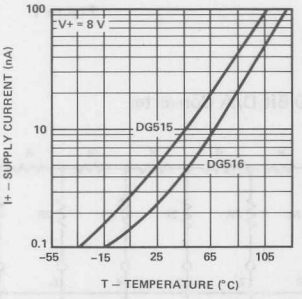
Leakage vs Temperature



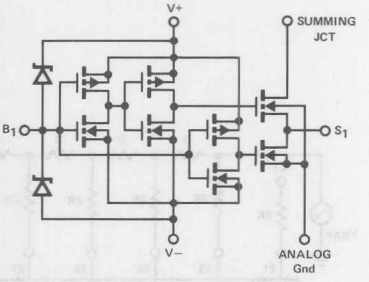
Supply Current vs Toggling Rate



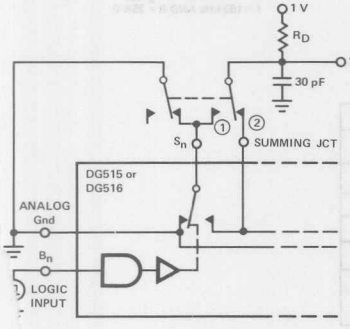
Quiescent Supply Current vs Temperature



Typical Channel (DG515 or DG516)

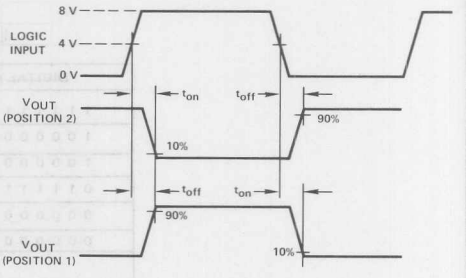


Switching Time Test Circuit



SWITCH	R_D (ohms)	
	DG515	DG516
1	50	300
2	100	300
3	200	300
4	200	510
5		510
6		1000
7		1000
8		1000
9		1000
10		1000

Switching Test Waveforms



APPLICATIONS

The following Application Circuits are intended to illustrate the following points:

1. A 2K Ω resistor should be in series with V+ to limit supply current with negative ringing of the bit inputs.
2. Temperature compensation for $R_{DS(on)}$ can be provided in the feedback path of the Op-Amp.
3. 4 Quadrant multiplication is possible by using the Analog Gnd current.
4. Bipolar reference voltages can be used in all configurations.
5. Resistor weighting other than Binary can be used.

4 Bit Multiplying Current Switch D/A

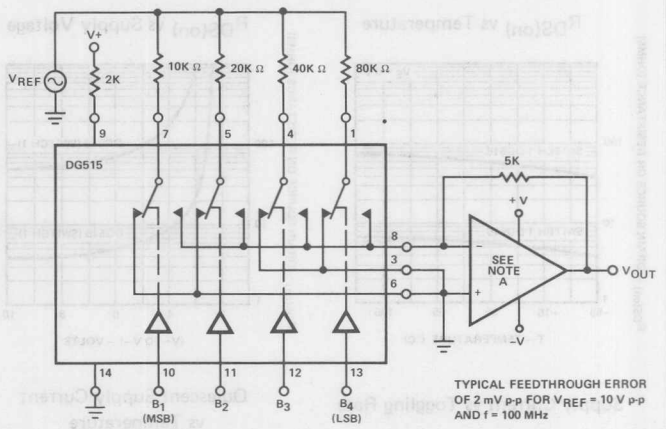


Figure 1

10 Bit D/A Converter

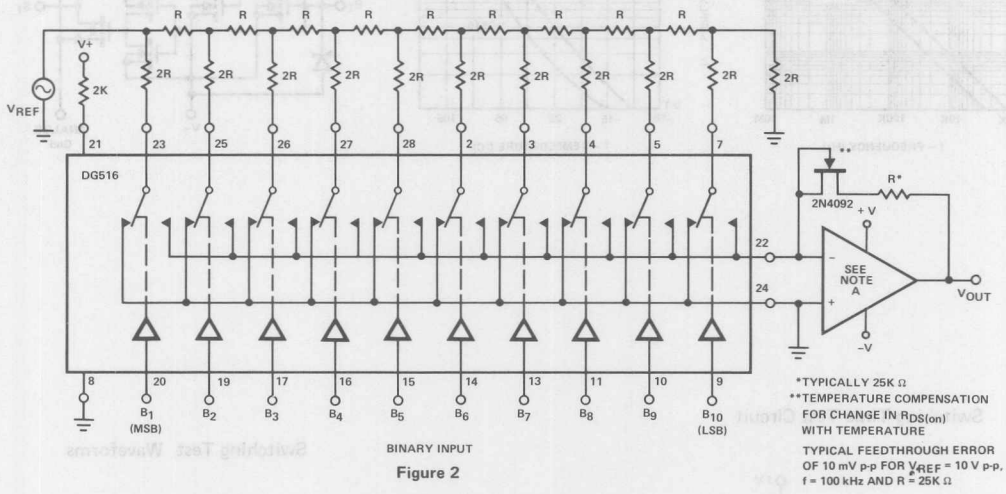


Figure 2

Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\,(1-2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\,(1/2+2^{-10})$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\,(1/2-2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\,(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

Figure 3

NOTE:

Op-Amp characteristics effect D/A accuracy and settling time. The following Op-Amps, listed in order of increasing speed, a suggested:

1. LM101A
2. LF156A
3. LM118

APPLICATIONS (Cont'd)

10 Bit, 4 Quadrant Multiplying DAC
(Offset Binary Coding)

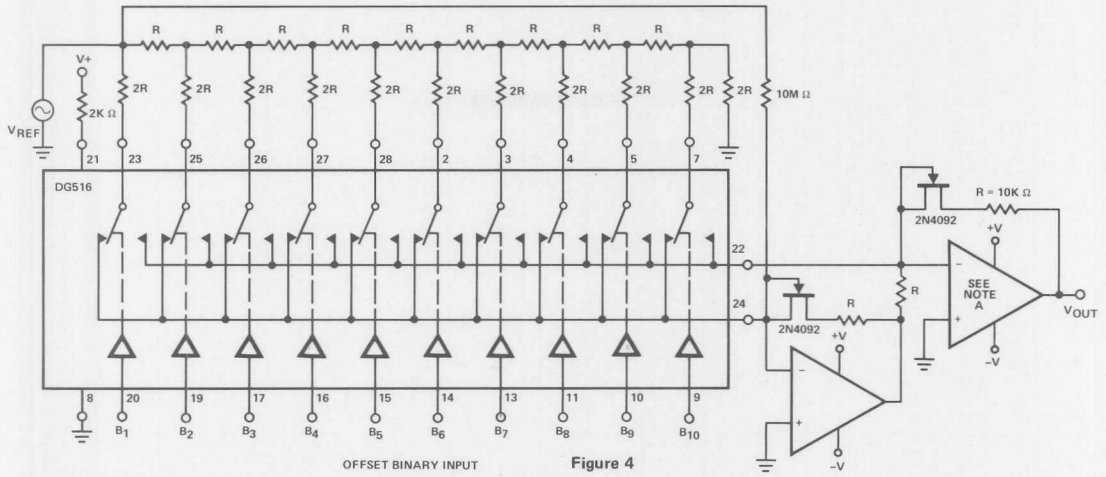


Figure 4

Bipolar (Offset Binary)* Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1-2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = $2^{-9} V_{REF}$

*Complementing B_1 (MSB) will give 2's complement coding.

Figure 5

Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-2^{-14})$
1 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2+2^{-14})$
1 0 0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1/2-2^{-14})$
0 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-14})$
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Figure 6

14 Bit Binary DAC (unipolar)

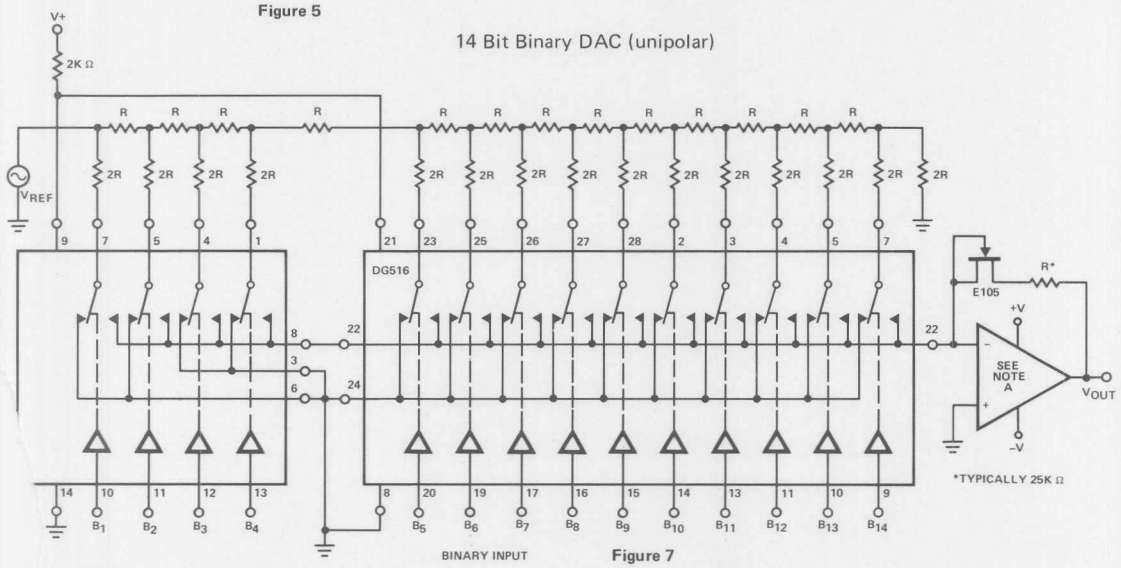


Figure 7

NOTE:

A. Op-Amp characteristics effect D/A accuracy and settling time. The following Op-Amps, listed in order of increasing speed, are suggested:

1. LM101A
2. LF156A
3. LM118

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Die Process Information

Siliconix is a large-volume supplier of die to the hybrid industry. Both military and industrial grades are available. Screening includes 100% DC electrical probe and 100% visual inspection of each die.

PHYSICAL DATA

Physical layout and dimensions are presented in the Die Topography section. Die are supplied to length and width dimensions which have an accuracy of ±0.003 inches. Thickness will be 0.015 inches (±0.001) for integrated circuit die and 0.008 inches (±0.002) for FETs.

Bonding pad location may be identified from the die topography shown. Contact factory for ordering information.

Each die or wafer is passivated with approximately 8,000 angstroms of non-crystalline glass.

FET chips are supplied with gold backing; gold backing is available as an option for integrated circuits.

Die metallization is deposited aluminum approximately 12,000 angstroms thick.

DIE SCREENING CRITERIA

Electrical Probe — All dice are 100% probed in wafer form at 25°C to DC criteria designed to support "A" suffix DC parameters. An optional screen to "C" suffix limits is available.

Visual Criteria — All die receives a visual inspection to MIL-STD-883, Method 2010, Condition B criteria. Siliconix QC Department samples each lot to an LTPD of 10%. Alternate visual criteria, including Method 2010, Condition A, or Siliconix Industrial criteria are available as options.

PACKAGING

Die are supplied in dust-proof, anti-static waffle packs (see illustration).

ASSEMBLY

The customer's interests will best be served if static sensitivity handling procedures are used.

PART NUMBER DESIGNATIONS

See ordering information.

ordered on die and wafers. OEM, wafer qualification should be specified as a separate line item on the purchase order.

Wafer Qualification to Unprobed Parameters

Wafer Qualification to Unprobed Parameters – Sample testing of purchased die to demonstrate capability to perform at data sheet temperature extremes or to switching time test limits by use of LTPD techniques can be provided at additional cost.

Alternate Electrical Probe – A 100% DC electrical probe to support "C" Suffix 25°C electrical specs is available for monolithic parts only. ("IDICE" ordering information.)

Visual inspection to customer generated specifications can be provided.

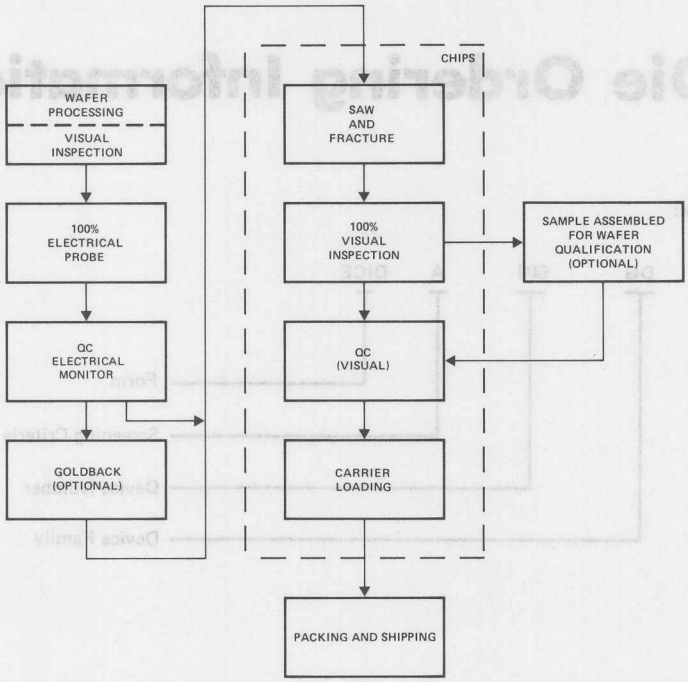
Alternate Electrical Probe – A 100% DC electrical probe to support "C" Suffix 25° electrical specs is available for monolithic parts only ("DICE" ordering information.)

Gold Backing – Die may be purchased with gold alloyed to the backside. This is a special order item. Gold thickness would be as follows:

- FETs (NC, NH, NIP) 750Å min
- IC's (all) 3500Å min

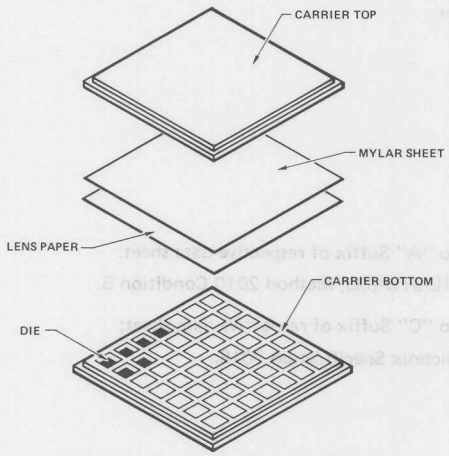
Hot Probe – Siliconix has chip processing distributors with hot probe capability available.

Chip and Wafer Processing



Chip Packaging

Chips are packaged as individual die in the flat waffle carrier illustrated in Figure 1. The carrier has a cavity size adequate to allow ease of loading/unloading and also prevents die from rotating within the cavity.



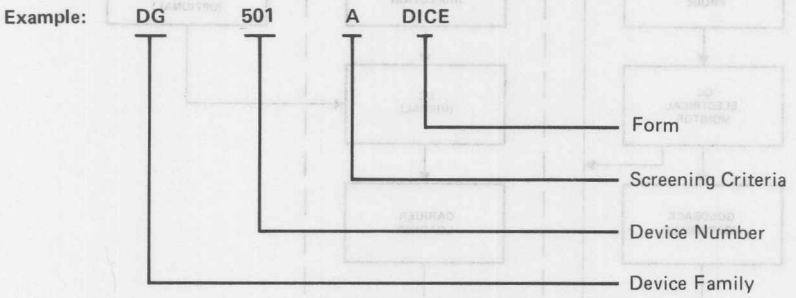
NOTE: CARRIER TOP & BOTTOM SECURED BY CLIPS

Figure 1

Siliconix

Die Ordering Information

1. **Monolithic Chips:**



DEVICE FAMILY
(1, 2 or 3 Letters)

D — Drivers for FET Switches
DG — Analog Switches
DGM — Analog Switches
G — Multi-Channel FETs
Si — Siliconix Second Source Part

DEVICE NUMBER
(3 or 4 Digit Numbers)

SCREENING CRITERIA
(1 Letter)

A — Electrically probed @ 25°C to "A" Suffix of respective data sheet; visual criteria screening to MIL-STD-883, Method 2010 Condition B.

I — Electrically probed @ 25°C to "C" Suffix of respective data sheet; visual criteria screening to Siliconix Specification 5018.

FORM
(4 Letters)

DICE — Chips waffle packed per Figure 4 in Die Process Information

2. Multichip

To order die which form multichip devices the driver chip and corresponding JFETs should be ordered using the geometry designations as shown in Table 1 below.

Example:
For D9190 die, order
CMJB1000
and NC1000

To determine number of JFETs required to go with each driver in a multichip device, see number in parenthesis following geometry codes as shown in table below.

Table 1

Siliconix Part No.	Geometry Code Driver	FET	Technology
DG123	IBAF/MABA	See D123 and G115	PMOS Switch
DG125	IBAF/MABA	See D125 and G115	PMOS Switch
DG126	LODC1000	NC2000(4)	JFET Switch
DG129	LODC1000	NC1000(4)	JFET Switch
DG133	LODC1000	NC1000(2)	JFET Switch
DG134	LODC1000	NC2000(2)	JFET Switch
DG139	LODF1000	NC1000(4)	JFET Switch
DG140	LODC1000	NIP1000(4)	JFET Switch
DG141	LODC1000	NIP1000(2)	JFET Switch
DG142	LODF1000	NC2000(4)	JFET Switch
DG143	LODF1000	NC2000(2)	JFET Switch
DG144	LODF1000	NC1000(2)	JFET Switch
DG145	LODF1000	NIP1000(4)	JFET Switch
DG146	LODF1000	NIP1000(2)	JFET Switch
DG151	LODC1000	NIP1000(2)	JFET Switch
DG152	LODC1000	NC1000(2)	JFET Switch
DG153	LODC1000	NIP1000(4)	JFET Switch
DG154	LODC1000	NC1000(4)	JFET Switch
DG161	LODF1000	NIP1000(2)	JFET Switch
DG162	LODF1000	NC1000(2)	JFET Switch
DG163	LODF1000	NIP1000(4)	JFET Switch
DG164	LODF1000	NC1000(4)	JFET Switch
DG180	CMJB1000	NIP1000(2)	JFET Switch
DG181	CMJB1000	NC1000(2)	JFET Switch
DG182	CMJB1000	NC2000(2)	JFET Switch
DG183	CMJA1000	NIP1000(4)	JFET Switch
DG184	CMJA1000	NC1000(4)	JFET Switch
DG185	CMJA1000	NC2000(4)	JFET Switch
DG186	CMJC1000	NIP1000(2)	JFET Switch
DG187	CMJC1000	NC1000(2)	JFET Switch
DG188	CMJC1000	NC2000(2)	JFET Switch
DG189	CMJB1000	NIP1000(4)	JFET Switch
DG190	CMJB1000	NC1000(4)	JFET Switch
DG191	CMJB1000	NC2000(4)	JFET Switch
DG281	CMJB1000	NH1000(2)	JFET Switch
DG284	CMJA1000	NH1000(4)	JFET Switch
DG287	CMJC1000	NH1000(2)	JFET Switch
DG290	CMJB1000	NH1000(4)	JFET Switch

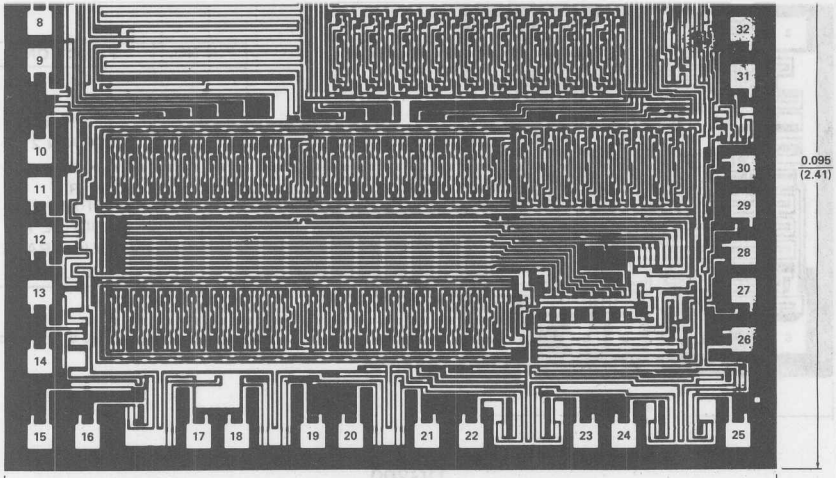
3. Options

The following options are considered "special" and a special part number will be assigned:

1. Die in wafer form
2. Goldbacking on Integrated Circuit die
3. Class A visual
4. Customer visual criteria

Please identify as "similar to _____ with following additional conditions_____."

Die Topography Information
Monolithic

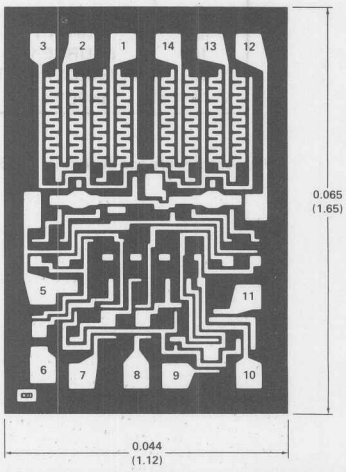


PAD NO.	FUNCTION	PAD NO.	FUNCTION	PAD NO.	FUNCTION
1	V_{DD}	15	c_3	29	B_2
2	e_1	16	d_3	30	B_3
3	g_1	17	e_3	31	D_1
4	f_1	18	g_3	32	D_2
5	BP	19	f_3	33	D_3
6	a_2	20	a_4	34	D_4
7	b_2	21	b_4	35	V_{SS}
8	c_2	22	c_4	36	OSC
9	d_2	23	d_4	37	a_1
10	e_2	24	e_4	38	b_1
11	g_2	25	g_4	39	c_1
12	f_2	26	f_4	40	d_1
13	a_3	27	B_0		
14	b_3	28	B_1		

Substrate = V_{DD}

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

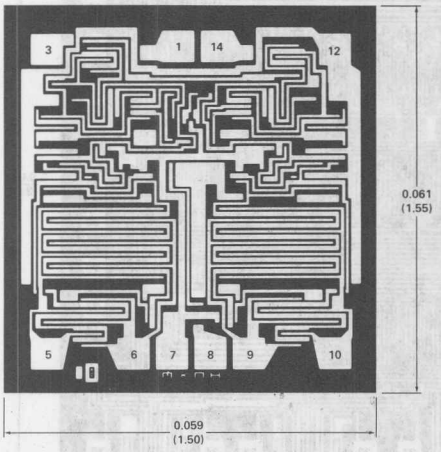
DF412



Pin numbers are for dual in-line packages

PIN NO.	FUNCTION
1	SOURCE 3
2	SOURCE 4
3	DRAIN
5	V– (SUBSTRATE)
6	INPUT 4
7	INPUT 3
8	INPUT 2
9	INPUT 1
10	V_L
11	V_R
12	V+
13	SOURCE 1
14	SOURCE 2

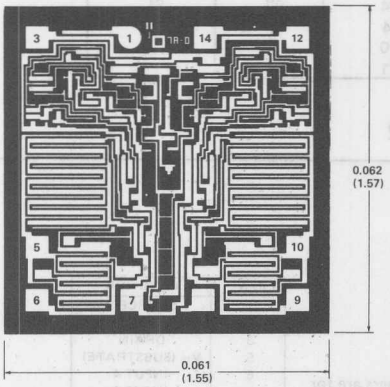
DG172



PIN NO.	FUNCTION
1	INPUT 2
3	GROUND
5	SOURCE 2
6	DRAIN 2
7	V–
8	V_{REF}
9	DRAIN 1
10	SOURCE 1
12	V+ (SUBSTRATE)
14	INPUT 1

Pin numbers are for dual in line packages.

DG200

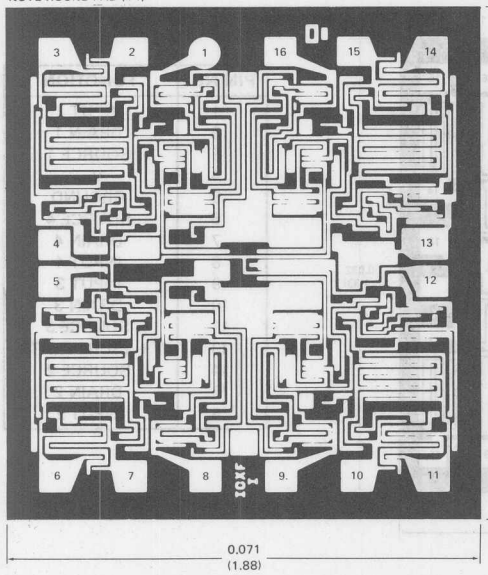


PIN NO.	FUNCTION
1	INPUT 2
3	GROUND
5	SOURCE 2
6	DRAIN 2
7	V–
9	DRAIN 1
10	SOURCE 1
12	V+ (SUBSTRATE)
14	INPUT 1

Pin numbers are for dual in line packages.

DG200A

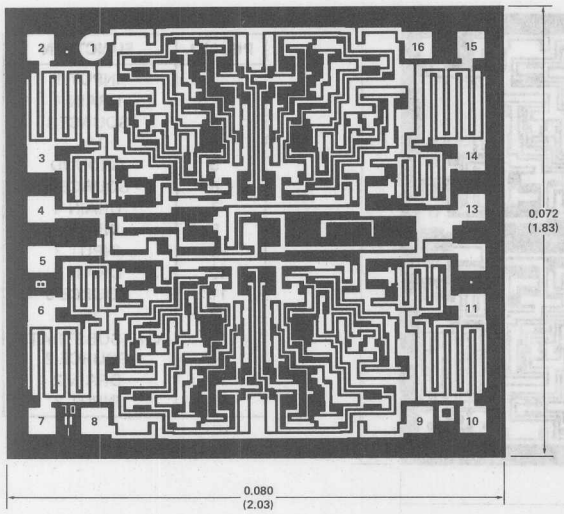
NOTE ROUND PAD (#1)



PIN NO.	FUNCTION
1	INPUT 1
2	DRAIN 1
3	SOURCE 1
4	V–
5	GND
6	SOURCE 4
7	DRAIN 4
8	INPUT 4
9	INPUT 3
10	DRAIN 3
11	SOURCE 3
12	V_{REF}
13	V+ (SUBSTRATE)
14	SOURCE 2
15	DRAIN 2
16	INPUT 2

Pin numbers are for dual in line packages

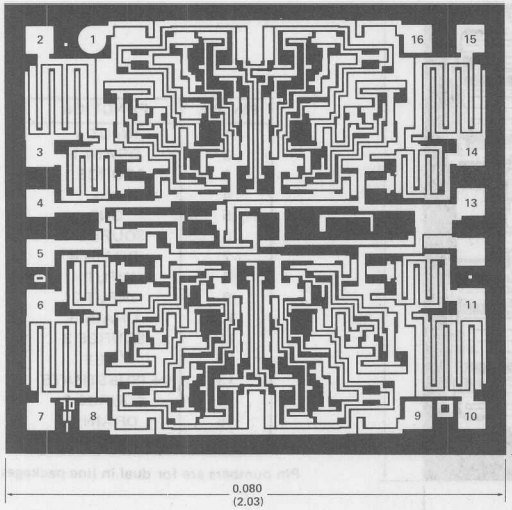
DG201



PIN NO.	FUNCTION
1	INPUT 1
2	DRAIN 1
3	SOURCE 1
4	V–
5	GND
6	SOURCE 4
7	DRAIN 4
8	INPUT 4
9	INPUT 3
10	DRAIN 3
11	SOURCE 3
13	V+ (SUBSTRATE)
14	SOURCE 2
15	DRAIN 2
16	INPUT 2

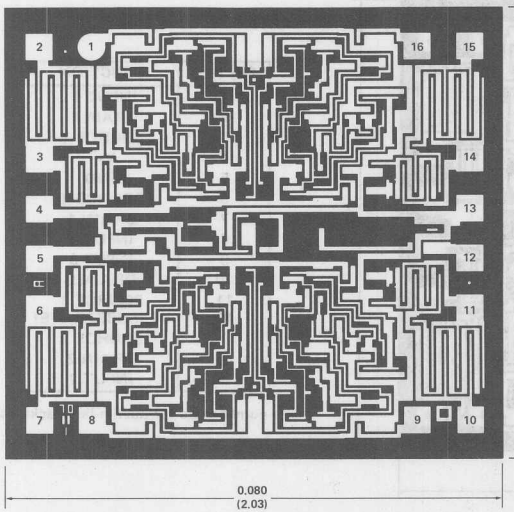
Pin numbers are for dual in-line packages

DG201A



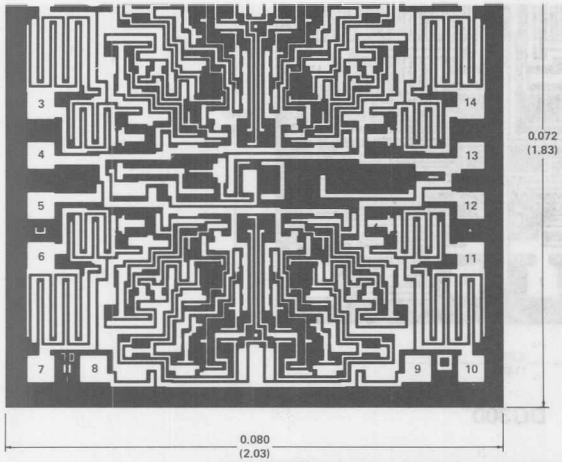
PIN NO.	FUNCTION
1	INPUT 1
2	DRAIN 1
3	SOURCE 1
4	V–
5	GROUND
6	SOURCE 4
7	DRAIN 4
8	INPUT 4
9	INPUT 3
10	DRAIN 3
11	SOURCE 3
13	V+ (SUBSTRATE)
14	SOURCE 2
15	DRAIN 2
16	INPUT 2

DG202



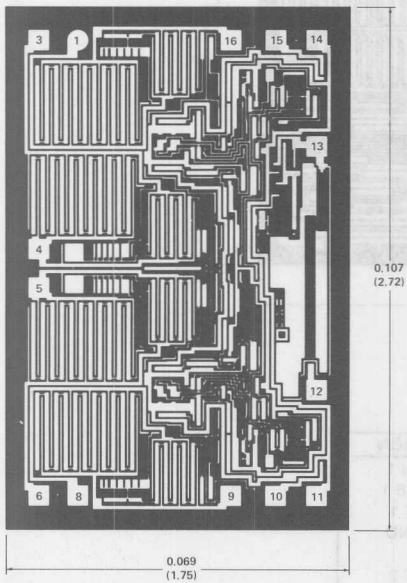
PIN NO.	FUNCTION
1	INPUT 1
2	DRAIN 1
3	SOURCE 1
4	V–
5	GROUND
6	SOURCE 4
7	DRAIN 4
8	INPUT 4
9	INPUT 3
10	DRAIN 3
11	SOURCE 3
12	V_L
13	V+ (SUBSTRATE)
14	SOURCE 2
15	DRAIN 2
16	INPUT 2

DG211



1	INPUT 1
2	DRAIN 1
3	SOURCE 1
4	V–
5	GROUND
6	SOURCE 4
7	DRAIN 4
8	INPUT 4
9	INPUT 3
10	DRAIN 3
11	SOURCE 3
12	V_L
13	V+ (SUBSTRATE)
14	SOURCE 2
15	DRAIN 2
16	INPUT 2

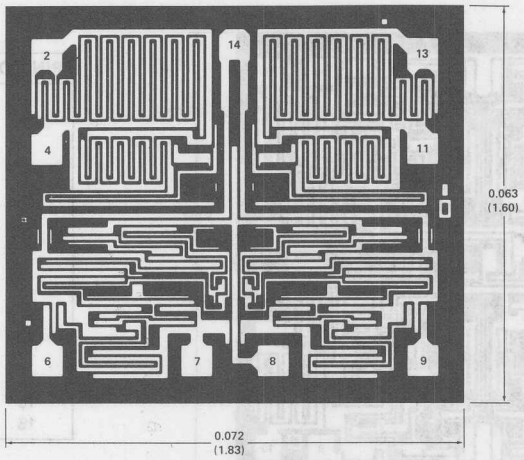
DG212



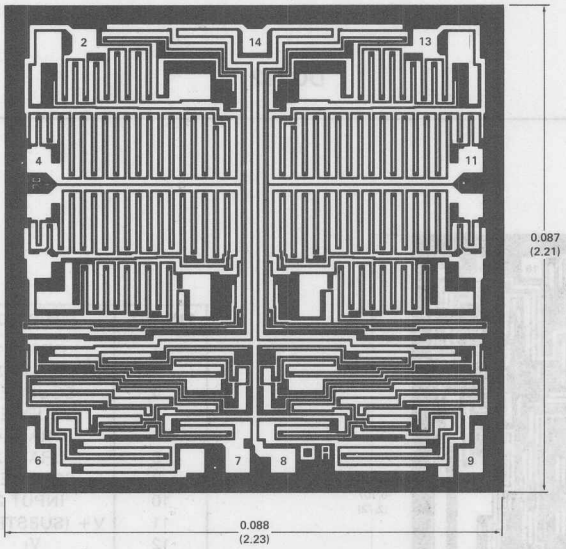
PIN NO.	FUNCTION
1	DRAIN 1
3	DRAIN 3
4	SOURCE 3
5	SOURCE 4
6	DRAIN 4
8	DRAIN 2
9	SOURCE 2
10	INPUT 2
11	V+ (SUBSTRATE)
12	V_L
13	GND
14	V–
15	INPUT 1
16	SOURCE 1

Pin numbers are for dual-in-line packages

DG243



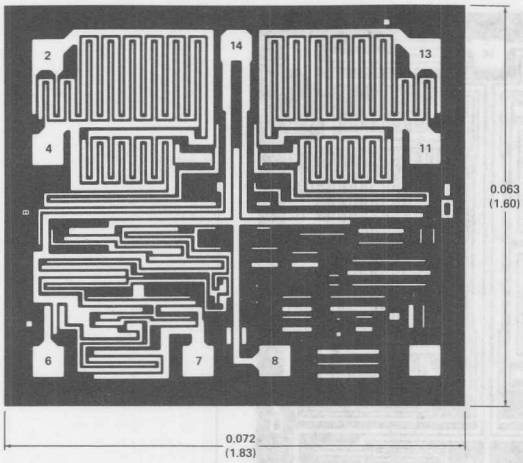
DG300



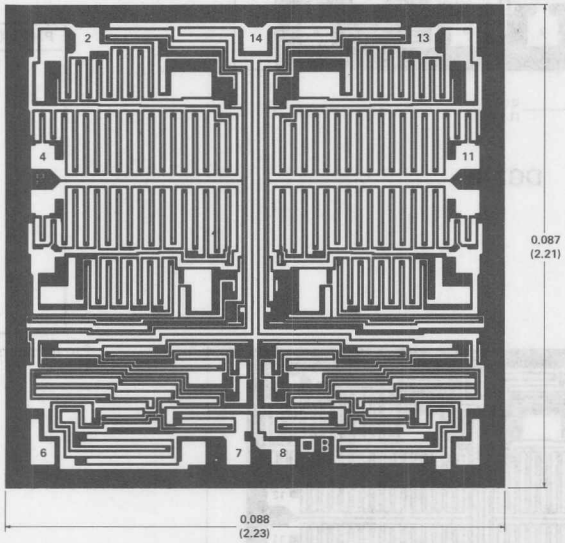
DG300A

PIN NO.	FUNCTION
2	DRAIN 1
4	SOURCE 1
6	INPUT 1
7	GROUND
8	V–
9	INPUT 2
11	SOURCE 2
13	DRAIN 2
14	V+ (SUBSTRATE)

Pin numbers are for dual in-line packages



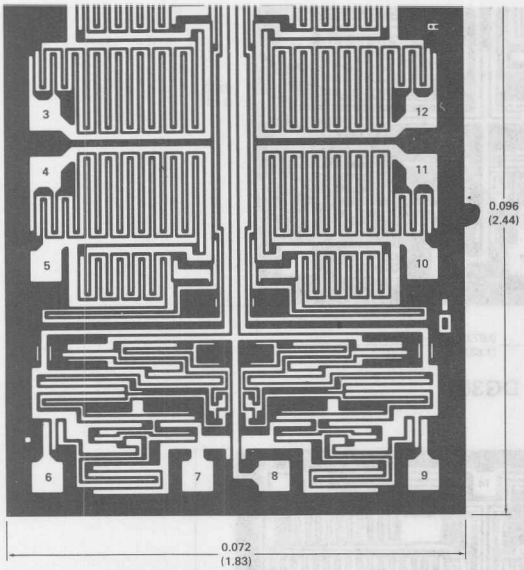
DG301



DG301A

PIN NO.	FUNCTION
2	DRAIN 1
4	SOURCE 1
6	INPUT 1
7	GROUND
8	V–
11	SOURCE 2
13	DRAIN 2
14	V+ (SUBSTRATE)

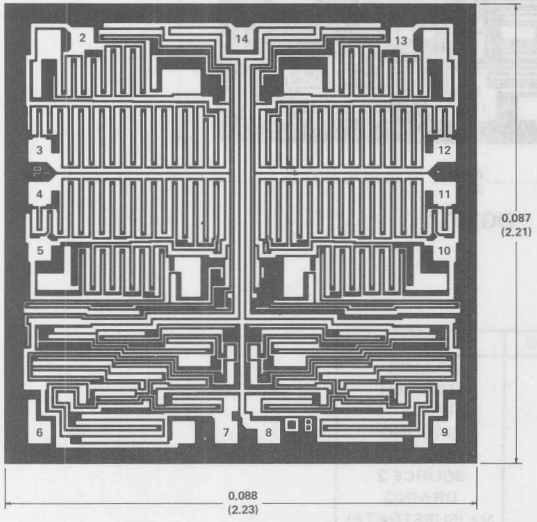
Pin numbers are for dual in-line packages



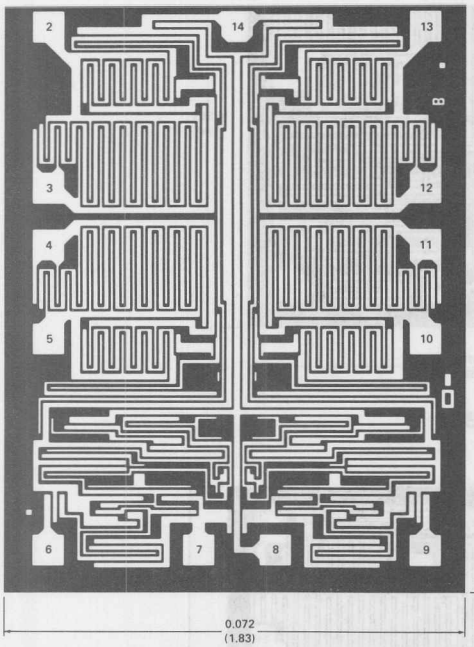
DG302

PIN NO.	FUNCTION
2	SOURCE 3
3	DRAIN 3
4	DRAIN 1
5	SOURCE 1
6	INPUT 1
7	GROUND
8	V–
9	INPUT 2
10	SOURCE 2
11	DRAIN 2
12	DRAIN 4
13	SOURCE 4
14	V+ (SUBSTRATE)

Pin numbers are for dual in-line packages



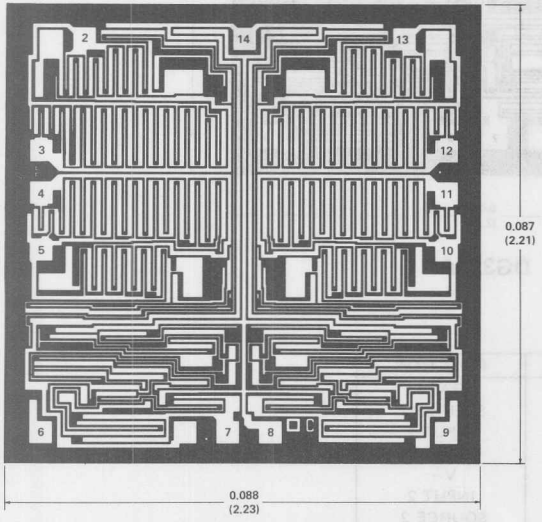
DG302A



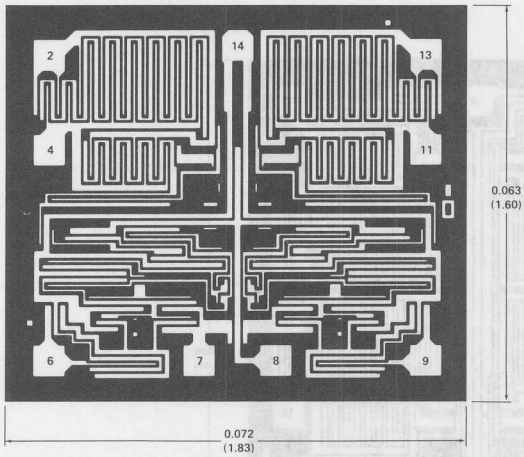
DG303

PIN NO.	FUNCTION
2	SOURCE 3
3	DRAIN 3
4	DRAIN 1
5	SOURCE 1
6	INPUT 1
7	GROUND
8	V–
9	INPUT 2
10	SOURCE 2
11	DRAIN 2
12	DRAIN 4
13	SOURCE 4
14	V+ (SUBSTRATE)

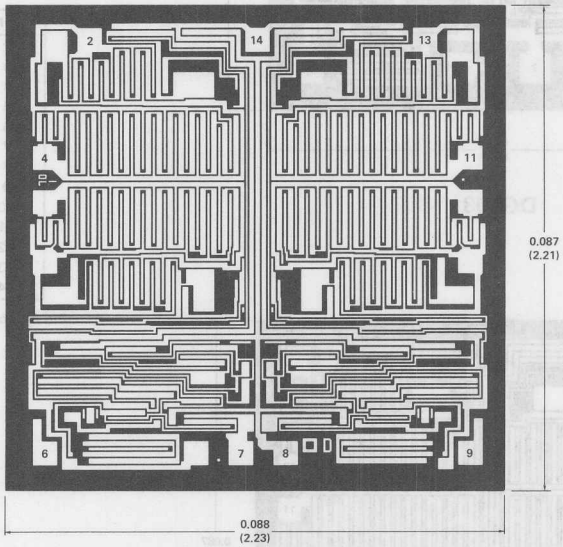
Pin numbers are for dual in-line packages



DG303A



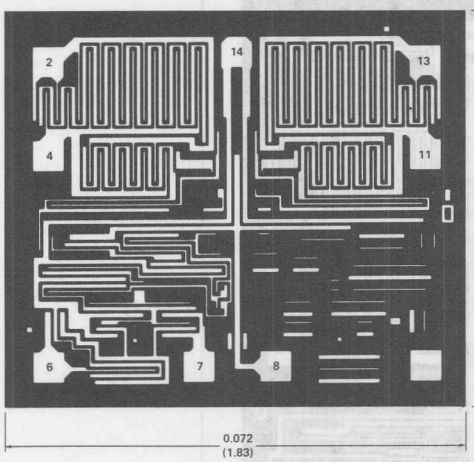
DG304



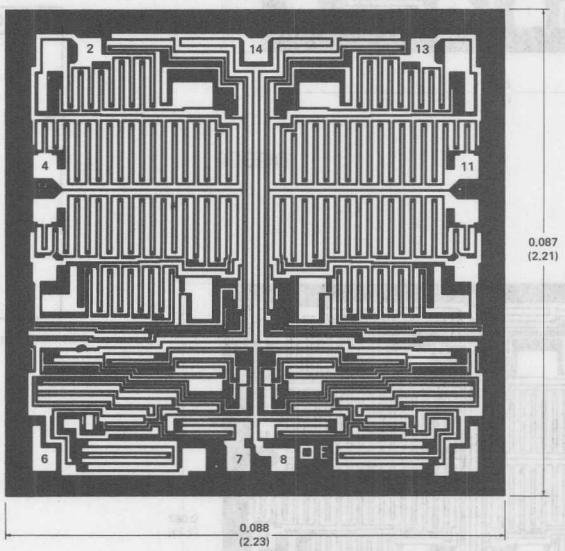
DG304A

PIN NO.	FUNCTION
2	DRAIN 1
4	SOURCE 1
6	INPUT 1
7	GROUND
8	V–
9	INPUT 2
11	SOURCE 2
13	DRAIN 2
14	V+ (SUBSTRATE)

Pin numbers are for dual in-line packages



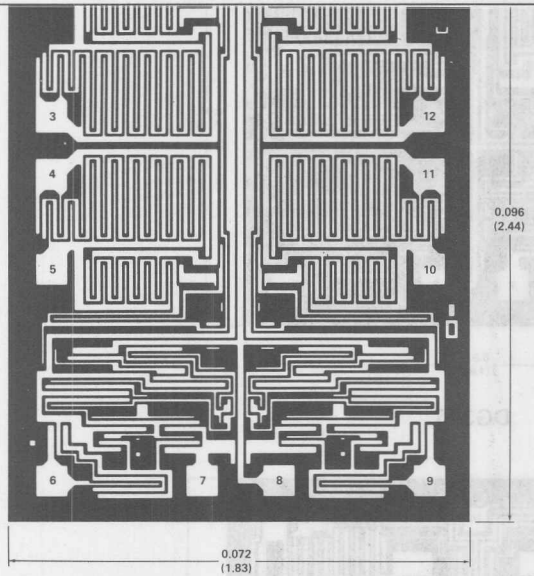
DG305



DG305A

PIN NO.	FUNCTION
2	DRAIN 1
4	SOURCE 1
6	INPUT 1
7	GROUND
8	V–
11	SOURCE 2
13	DRAIN 2
14	V+ (SUBSTRATE)

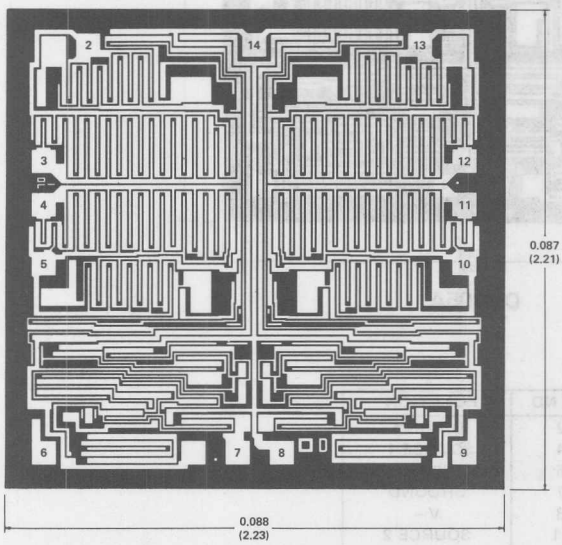
Pin numbers for dual in-line packages



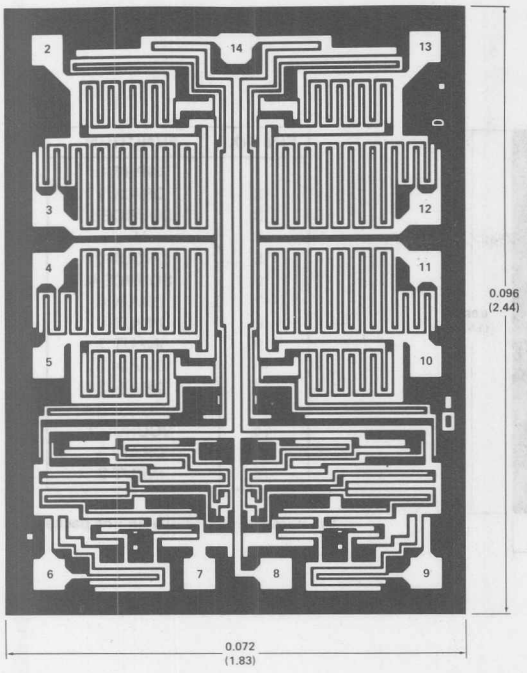
DG306

PIN NO.	FUNCTION
2	SOURCE 3
3	DRAIN 3
4	DRAIN 1
5	SOURCE 1
6	INPUT 1
7	GROUND
8	V–
9	INPUT 2
10	SOURCE 2
11	DRAIN 2
12	DRAIN 4
13	SOURCE 4
14	V+ (SUBSTRATE)

Pin numbers are for dual in-line packages



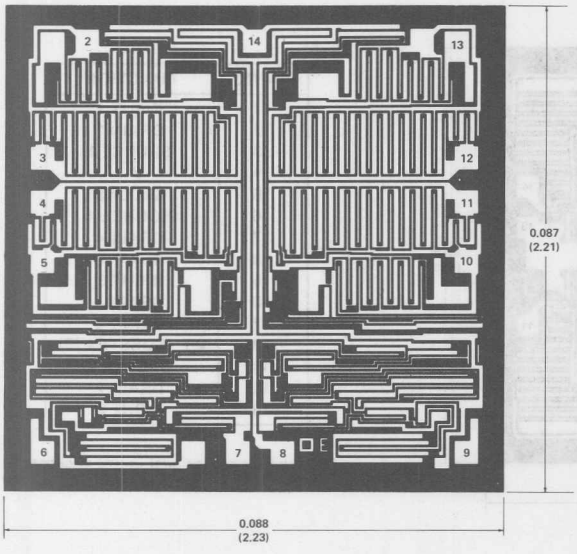
DG306A



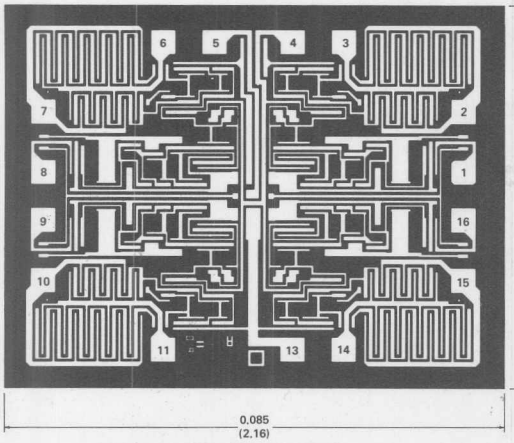
DG307

PIN NO.	FUNCTION
2	SOURCE 3
3	DRAIN 3
4	DRAIN 1
5	SOURCE 1
6	INPUT 1
7	GROUND
8	V–
9	INPUT 2
10	SOURCE 2
11	DRAIN 2
12	DRAIN 4
13	SOURCE 4
14	V+ (SUBSTRATE)

Pin numbers are for dual in-line packages



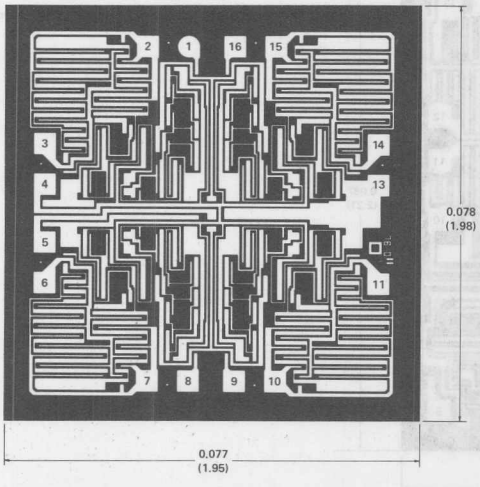
DG307A



PIN NO.	FUNCTION
1	INPUT 1
2	DRAIN 1
3	SOURCE 1
4	V–
5	GROUND
6	SOURCE 4
7	DRAIN 4
8	INPUT 4
9	INPUT 3
10	DRAIN 3
11	DRAIN 3
13	V+ (SUBSTRATE)
14	SOURCE 2
15	DRAIN 2
16	INPUT 2

Pin numbers are for dual in-line packages

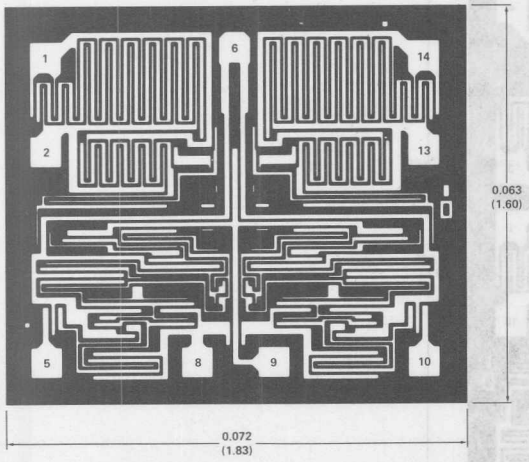
DG308



PIN NO.	FUNCTION
1	INPUT 1
2	DRAIN 1
3	SOURCE 1
4	V–
5	GROUND
6	SOURCE 4
7	DRAIN 4
8	INPUT 4
9	INPUT 3
10	DRAIN 3
11	DRAIN 3
13	V+ (SUBSTRATE)
14	SOURCE 2
15	DRAIN 2
16	INPUT 2

Pin numbers are for dual in-line packages

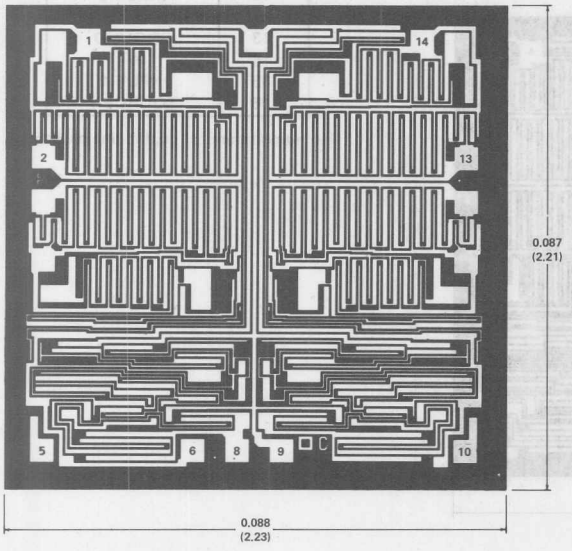
DG309



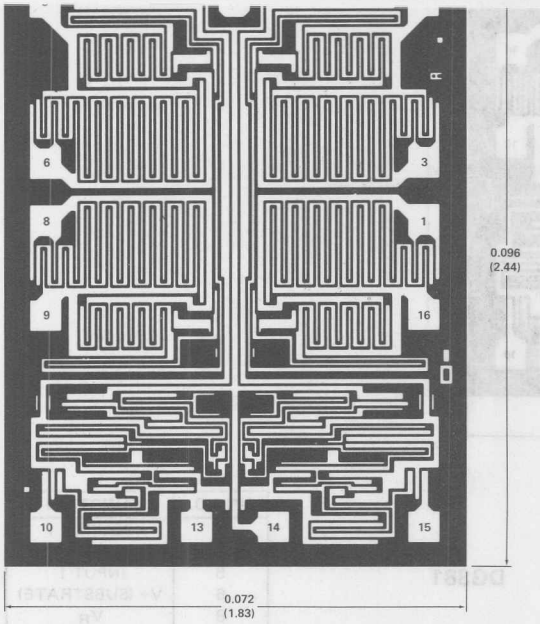
DG381

PIN NO.	FUNCTION
1	SOURCE 1
2	DRAIN 1
5	INPUT 1
6	V+ (SUBSTRATE)
8	V_R
9	V–
10	INPUT 2
13	DRAIN 2
14	SOURCE 2

Pin numbers are for dual in-line packages



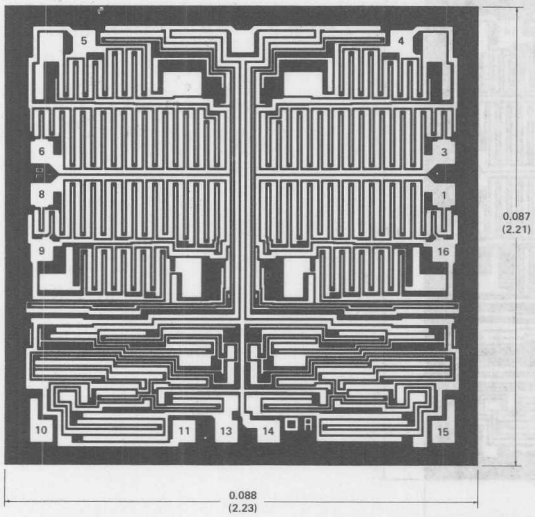
DG381A



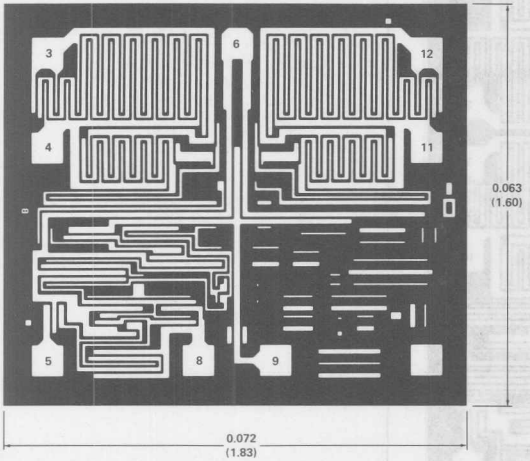
DG384

PIN NO.	FUNCTION
1	DRAIN 1
3	DRAIN 3
4	SOURCE 3
5	SOURCE 4
6	DRAIN 4
8	DRAIN 2
9	SOURCE 2
10	INPUT 2
11	V+ (SUBSTRATE)
13	GROUND
14	V–
15	INPUT 1
16	SOURCE 1

Pin numbers are for dual in-line packages



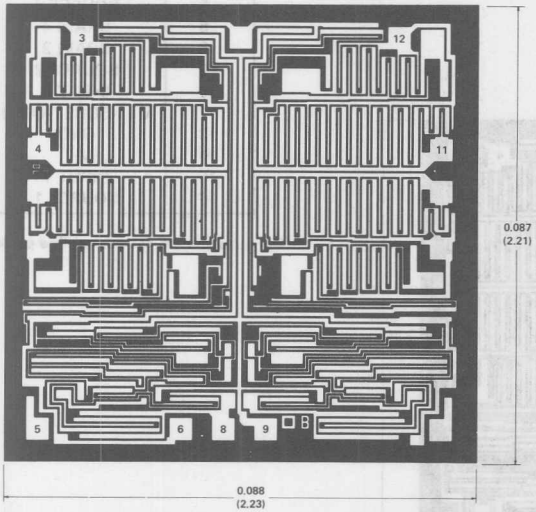
DG384A



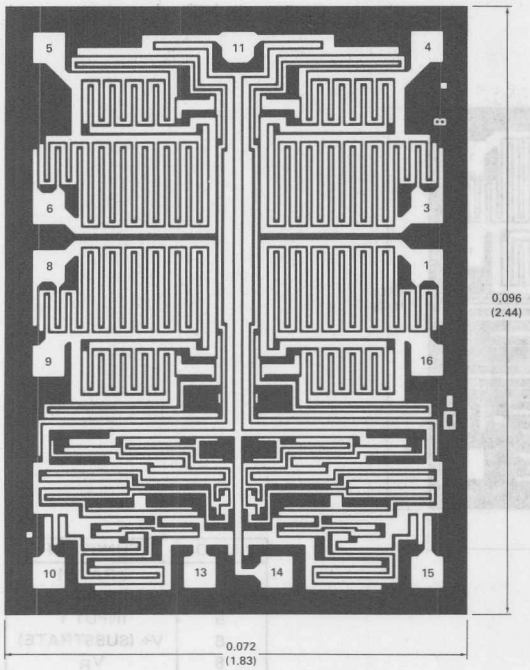
DG387

PIN NO.	FUNCTION
3	DRAIN 1
4	SOURCE 1
5	INPUT 1
6	V+ (SUBSTRATE)
8	V_R
9	V−
11	SOURCE 2
12	DRAIN 2

Pin numbers are for dual in-line packages



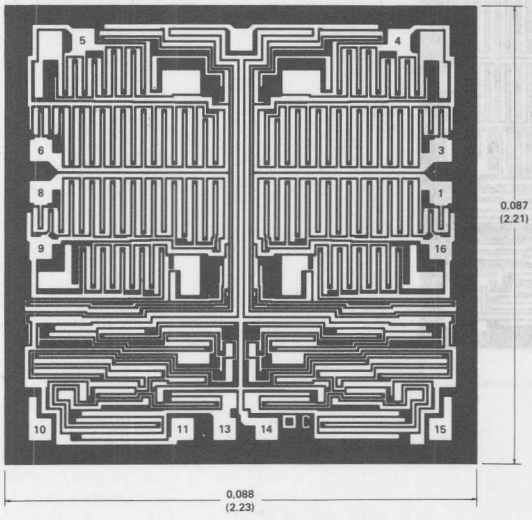
DG387A



DG390

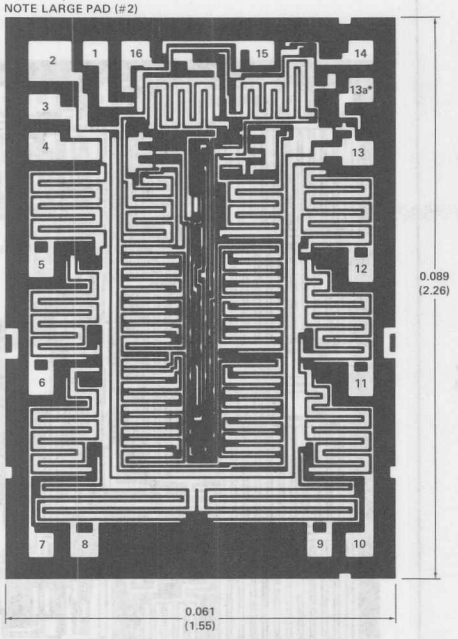
PIN NO.	FUNCTION
1	INPUT 1
3	DRAIN 3
4	SOURCE 3
5	SOURCE 4
6	DRAIN 4
8	DRAIN 2
9	SOURCE 2
10	INPUT 2
11	V+ (SUBSTRATE)
13	GND
14	V−
15	INPUT 1
16	SOURCE 1

Pin numbers are for dual in-line packages



DG390A

NOTE LARGE PAD (#2)



PIN NO.	FUNCTION
1	ENABLE
2†	V+ (SUBSTRATE)
3	DRAIN
4†	V+ (SUBSTRATE)
5	SOURCE 8
6	SOURCE 7
7	SOURCE 6
8	SOURCE 5
9	SOURCE 4
10	SOURCE 3
11	SOURCE 2
12	SOURCE 1
13	V–
14	ADDRESS 0
15	ADDRESS 1
16	ADDRESS 2

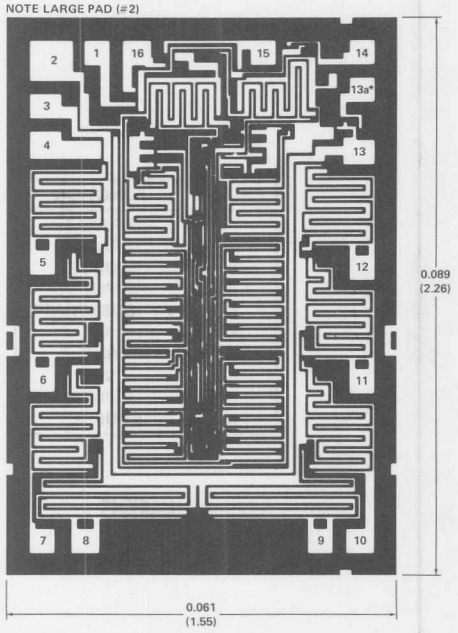
*13a is connected to V–

† Pins 2 and 4 are interconnected, either one may be used

Pin numbers are for dual in-line packages

DG501

NOTE LARGE PAD (#2)

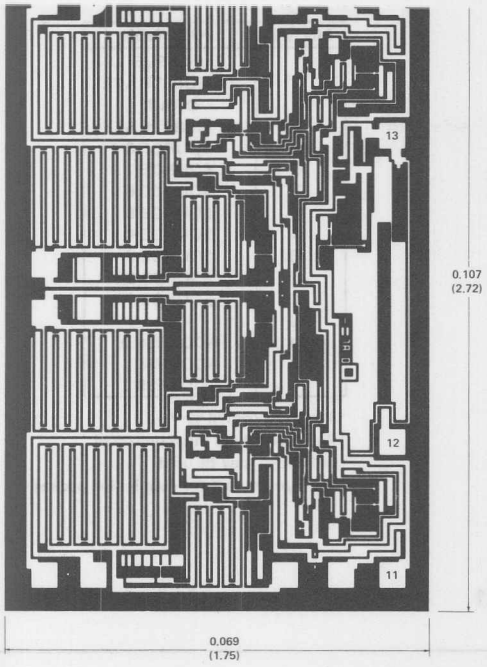


PIN NO.	FUNCTION
1	ENABLE
2*	V+ (SUBSTRATE)
3	DRAIN
4*	V+ (SUBSTRATE)
5	SOURCE 8
6	SOURCE 7
7	SOURCE 6
8	SOURCE 5
9	SOURCE 4
10	SOURCE 3
11	SOURCE 2
12	SOURCE 1
13	V–
14	ADDRESS 0
15	ADDRESS 1
16	ADDRESS 2

*Pins 2 and 4 are interconnected, either one may be used

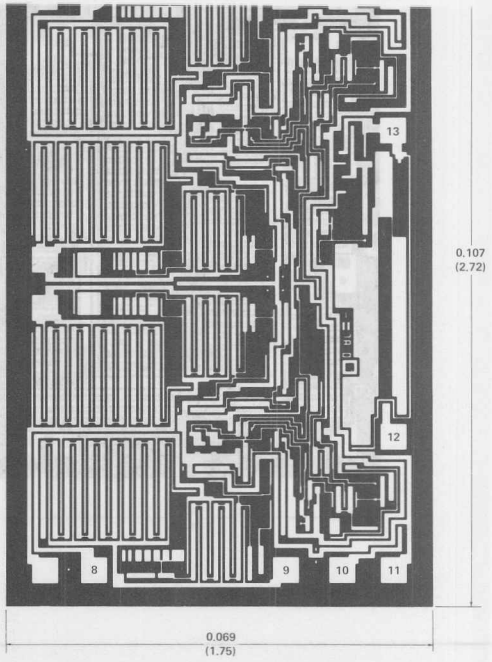
Pin numbers are for dual in-line packages

DG503



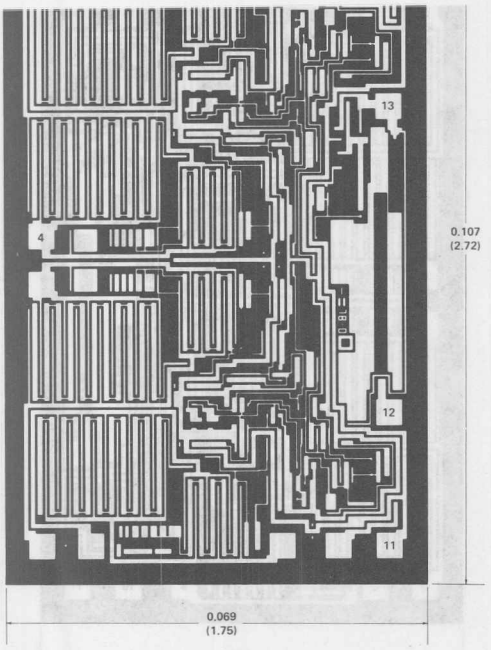
PIN NO.	FUNCTION
1	DRAIN 1
11	V+ (SUBSTRATE)
12	V_L
13	GND
14	V−
15	INPUT 1
16	SOURCE 1

DG5040



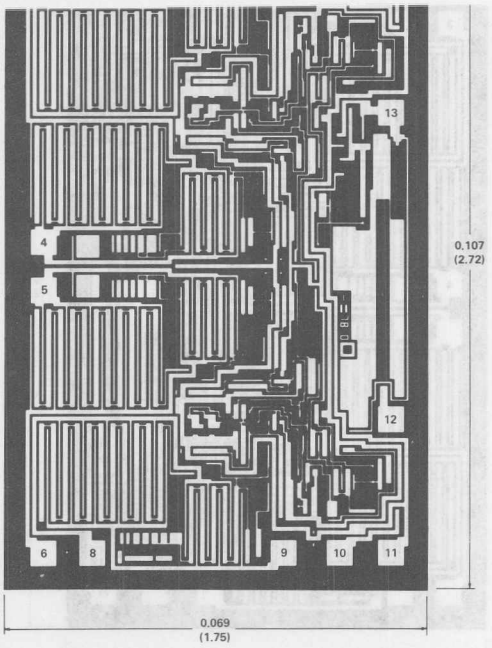
PIN NO.	FUNCTION
1	DRAIN 1
8	DRAIN 2
9	SOURCE 2
10	INPUT 2
11	V+ (SUBSTRATE)
12	V_L
13	GND
14	V−
15	INPUT 1
16	SOURCE 1

DG5041



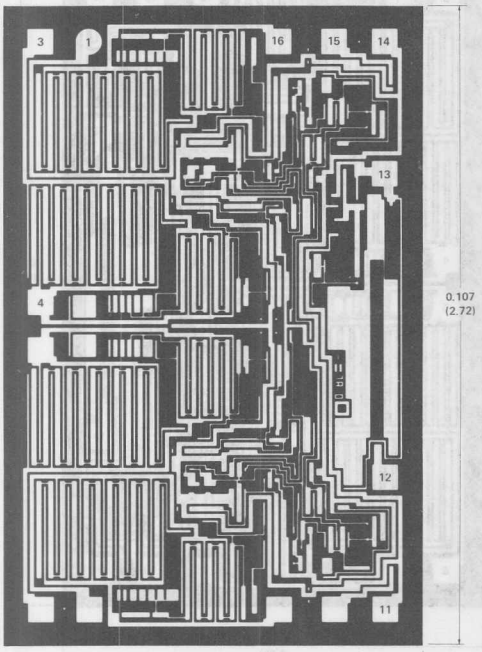
PIN NO.	FUNCTION
1	DRAIN 1
3	DRAIN 2
4	SOURCE 2
11	V+ (SUBSTRATE)
12	V_L
13	GND
14	V−
15	INPUT 1
16	SOURCE 1

DG5042



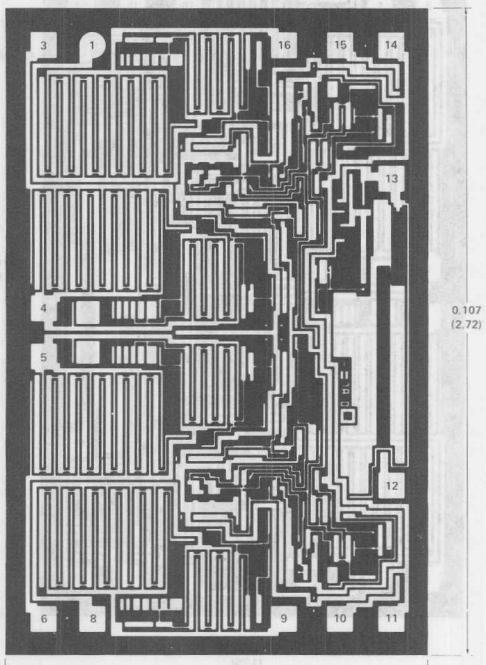
PIN NO.	FUNCTION
1	DRAIN 1
3	DRAIN 3
4	SOURCE 3
5	SOURCE 4
6	DRAIN 4
8	DRAIN 2
9	SOURCE 2
10	INPUT 2
11	V+ (SUBSTRATE)
12	V_L
13	GND
14	V−
15	INPUT 1
16	SOURCE 1

DG5043



PIN NO.	FUNCTION
1	DRAIN 1
3	DRAIN 2
4	SOURCE 2
11	V+ (SUBSTRATE)
12	V_L
13	GND
14	V–
15	INPUT 1
16	SOURCE 1

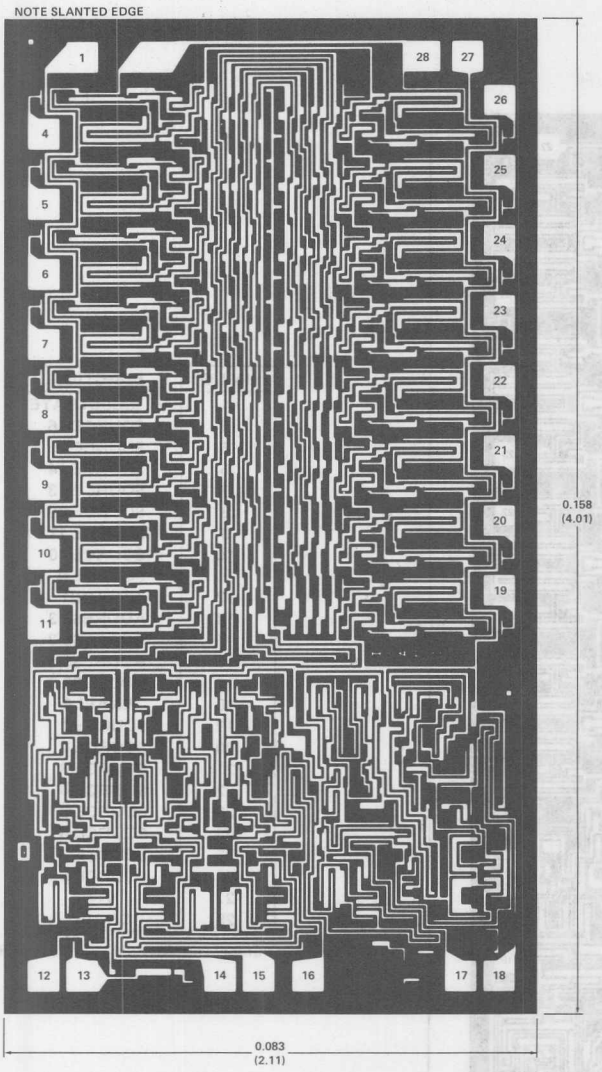
DG5044



PIN NO.	FUNCTION
1	DRAIN 1
3	DRAIN 3
4	SOURCE 3
5	SOURCE 4
6	DRAIN 4
8	DRAIN 2
9	SOURCE 2
10	INPUT 2
11	V+ (SUBSTRATE)
12	V_L
13	GND
14	V–
15	INPUT 1
16	SOURCE 1

Pin numbers are for dual-in-line packages.

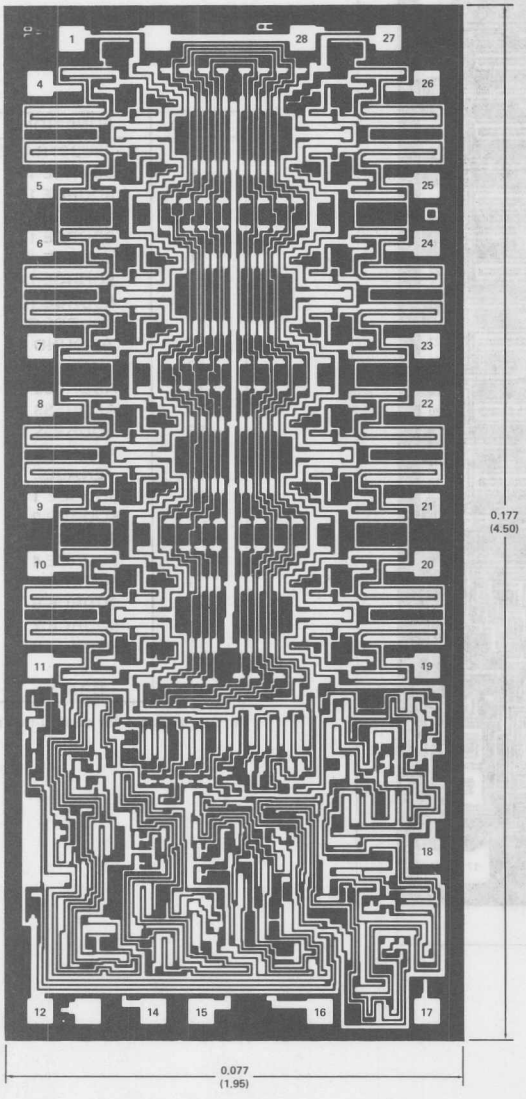
DG5045



PIN NO.	FUNCTION
1	V+ (SUBSTRATE)
4	SOURCE 16
5	SOURCE 15
6	SOURCE 14
7	SOURCE 13
8	SOURCE 12
9	SOURCE 11
10	SOURCE 10
11	SOURCE 9
12	GROUND
13	V_{REF}
14	ADDRESS 3
15	ADDRESS 2
16	ADDRESS 1
17	ADDRESS 0
18	ENABLE
19	SOURCE 1
20	SOURCE 2
21	SOURCE 3
22	SOURCE 4
23	SOURCE 5
24	SOURCE 6
25	SOURCE 7
26	SOURCE 8
27	V–
28	DRAIN

Pin numbers are for dual in-line packages

DG506

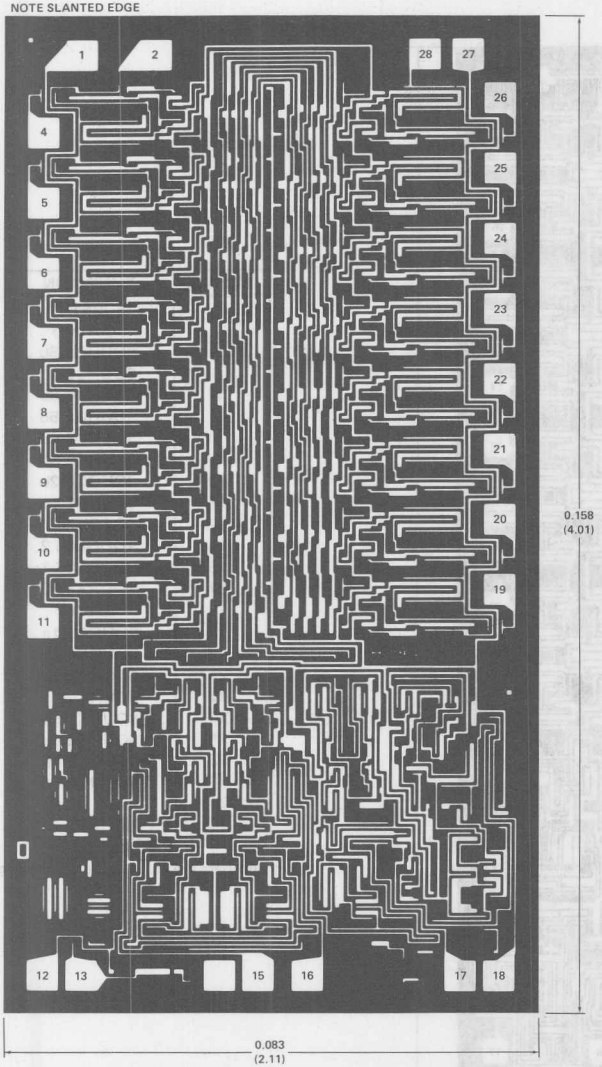


PIN NO.	FUNCTION
1	V+ (SUBSTRATE)
4	SOURCE 16
5	SOURCE 15
6	SOURCE 14
7	SOURCE 13
8	SOURCE 12
9	SOURCE 11
10	SOURCE 10
11	SOURCE 9
12	GROUND
14	ADDRESS 3
15	ADDRESS 2
16	ADDRESS 1
17	ADDRESS 0
18	ENABLE
19	SOURCE 1
20	SOURCE 2
21	SOURCE 3
22	SOURCE 4
23	SOURCE 5
24	SOURCE 6
25	SOURCE 7
26	SOURCE 8
27	V–
28	DRAIN

Pin numbers are for dual in-line packages

DG506A

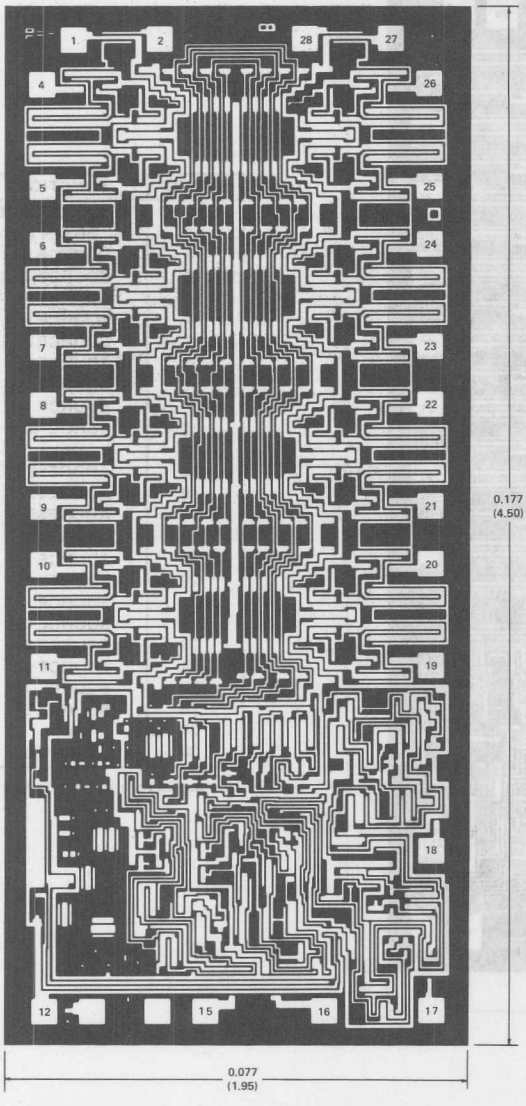
NOTE SLANTED EDGE



PIN NO.	FUNCTION
1	V+ (SUBSTRATE)
2	DRAIN b
4	SOURCE 8b
5	SOURCE 7b
6	SOURCE 6b
7	SOURCE 5b
8	SOURCE 4b
9	SOURCE 3b
10	SOURCE 2b
11	SOURCE 1b
12	GROUND
13	V_{REF}
15	ADDRESS 2
16	ADDRESS 1
17	ADDRESS 0
18	ENABLE
19	SOURCE 1a
20	SOURCE 2a
21	SOURCE 3a
22	SOURCE 4a
23	SOURCE 5a
24	SOURCE 6a
25	SOURCE 7a
26	SOURCE 8a
27	V–
28	DRAIN a

Pin numbers are for dual in-line packages

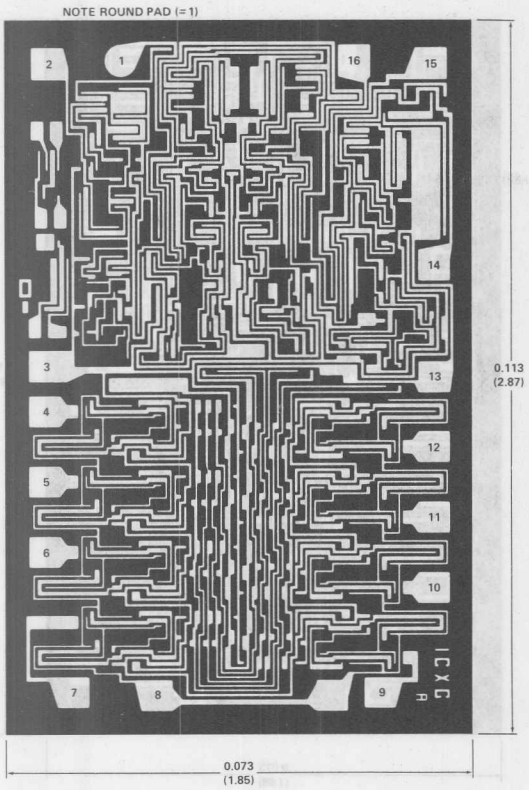
DG507



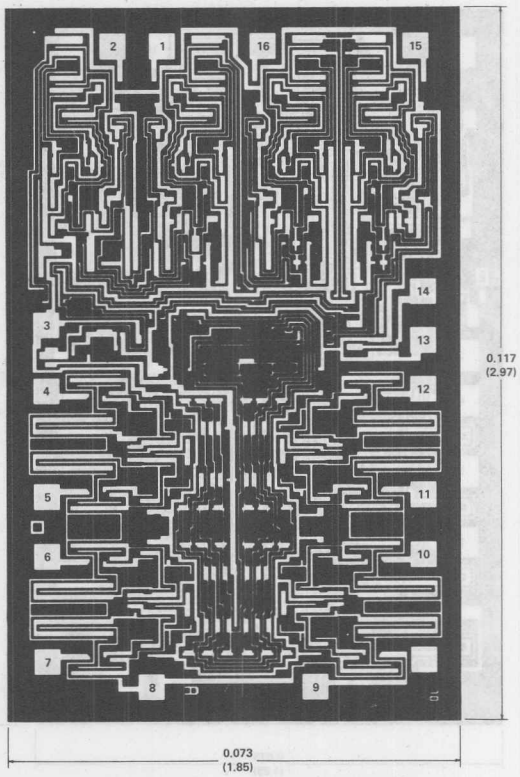
PIN NO.	FUNCTION
1	V+ (SUBSTRATE)
2	DRAIN b
4	SOURCE 8b
5	SOURCE 7b
6	SOURCE 6b
7	SOURCE 5b
8	SOURCE 4b
9	SOURCE 3b
10	SOURCE 2b
11	SOURCE 1b
12	GROUND
15	ADDRESS 2
16	ADDRESS 1
17	ADDRESS 0
18	ENABLE
19	SOURCE 1a
20	SOURCE 2a
21	SOURCE 3a
22	SOURCE 4a
23	SOURCE 5a
24	SOURCE 6a
25	SOURCE 7a
26	SOURCE 8a
27	V–
28	DRAIN a

Pin numbers are for dual in-line packages

DG507A



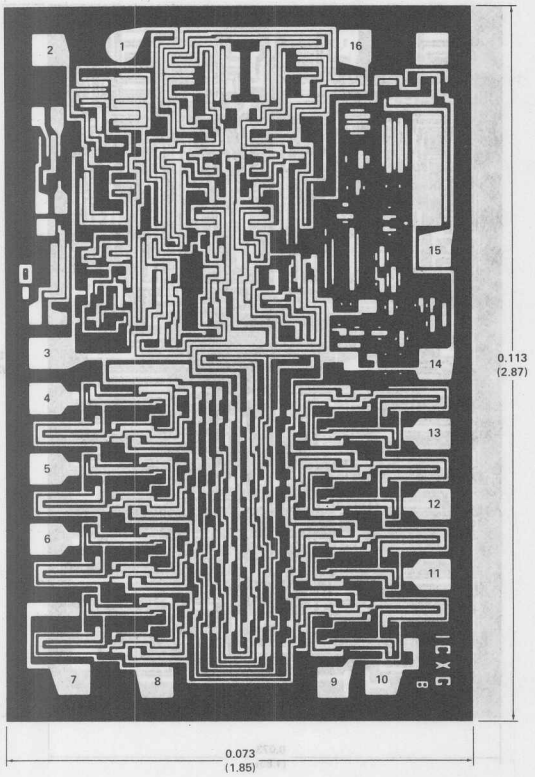
DG508



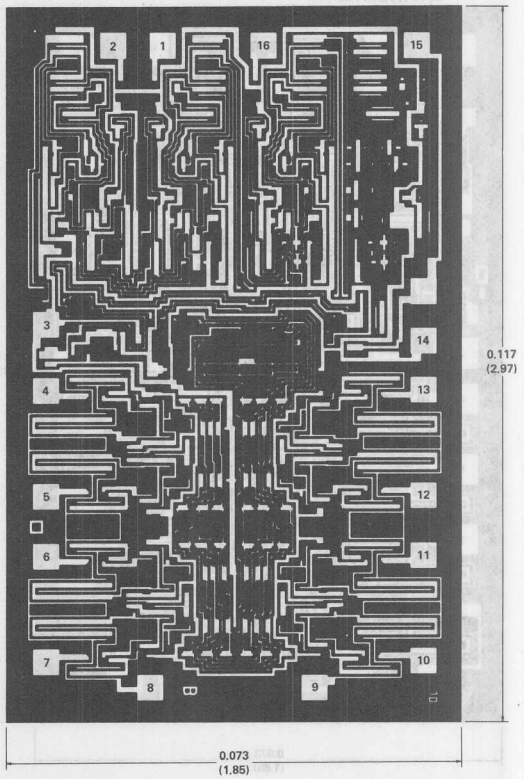
DG508A

PIN NO.	FUNCTION
1	ADDRESS 0
2	ENABLE
3	V–
4	SOURCE 1
5	SOURCE 2
6	SOURCE 3
7	SOURCE 4
8	DRAIN
9	SOURCE 8
10	SOURCE 7
11	SOURCE 6
12	SOURCE 5
13	V+ (SUBSTRATE)
14	GROUND
15	ADDRESS 2
16	ADDRESS 1

Pin number are for dual in-line packages



DG509

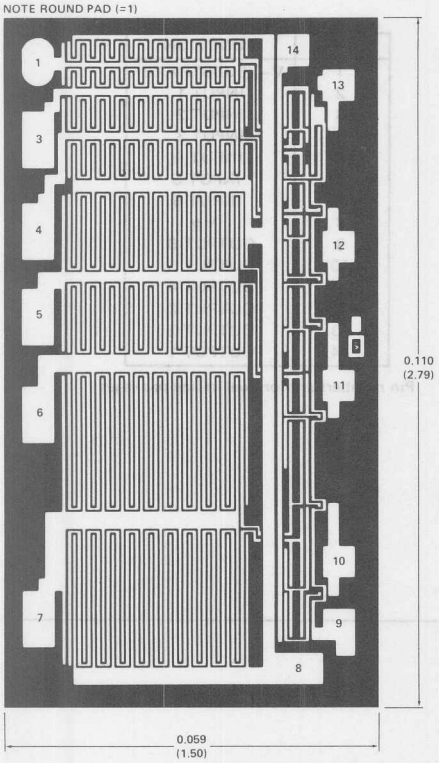


DG509A

PIN NO.	FUNCTION
1	ADDRESS 0
2	ENABLE
3	V–
4	SOURCE 1a
5	SOURCE 2a
6	SOURCE 3a
7	SOURCE 4a
8	DRAIN a
9	DRAIN b
10	SOURCE 4b
11	SOURCE 3b
12	SOURCE 2b
13	SOURCE 1b
14	V+ (SUBSTRATE)
15	GROUND
16	ADDRESS 1

Pin numbers are for dual in-line packages

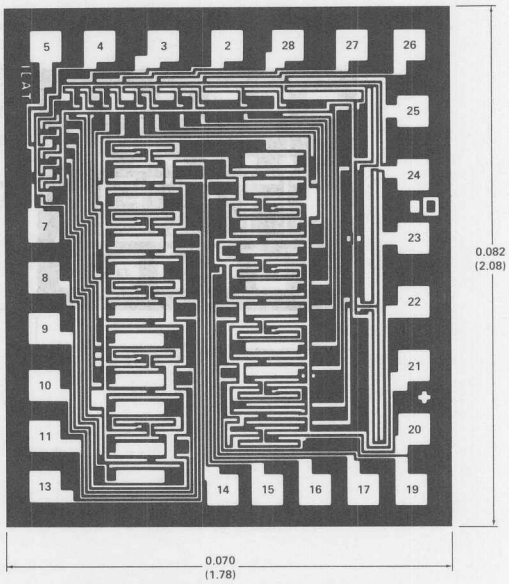
NOTE ROUND PAD (=1)



PIN NO.	FUNCTION
1	SOURCE 4
3	ANALOG GROUND 2
4	SOURCE 3
5	SOURCE 2
6	ANALOG GROUND 1
7	SOURCE 1
8	SUM JCT
9	V+ (SUBSTRATE)
10	B1
11	B2
12	B3
13	B4
14	V–

Pin numbers are for dual in-line packages

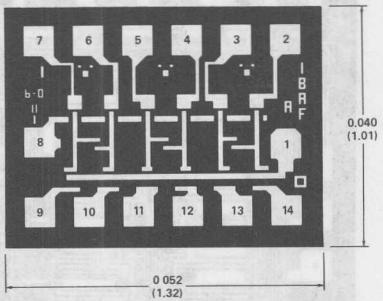
DG515



PIN NO.	FUNCTION
2	SOURCE 6
3	SOURCE 7
4	SOURCE 8
5	SOURCE 9
7	SOURCE 10
8	V–
9	B10
10	B9
11	B8
13	B7
14	B6
15	B5
16	B4
17	B3
19	B2
20	B1
21	V+ (SUBSTRATE)
22	SUM JCT
23	S1
24	ANALOG GROUND
25	S2
26	S3
27	S4
28	S5

Pin numbers are for dual in-line packages

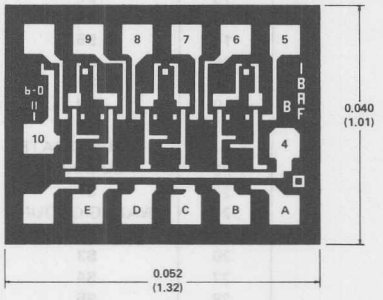
DG516



PIN NO.	FUNCTION
1	V– (SUBSTRATE)
2	INPUT 1
3	INPUT 2
4	INPUT 3
5	INPUT 4
6	INPUT 5
7	INPUT 6
8	V_R
9	OUTPUT 6
10	OUTPUT 5
11	OUTPUT 4
12	OUTPUT 3
13	OUTPUT 2
14	OUTPUT 1

Pin numbers are for dual in-line packages

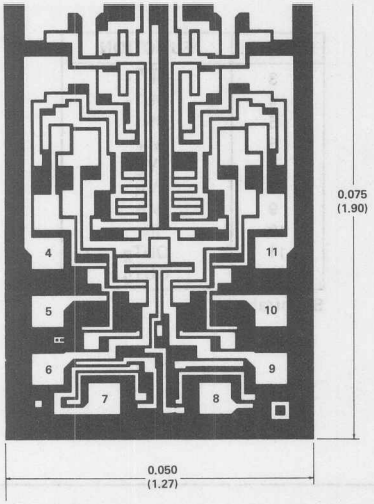
D123



PIN NO.	FUNCTION
1	V– (SUBSTRATE)
2	INPUT 1
3	INPUT 2
4	INPUT 3
5	INPUT 4
6	INPUT 5
7	INPUT 6
8	V_L
9	OUTPUT 6
10	OUTPUT 5
11	OUTPUT 4
12	OUTPUT 3
13	OUTPUT 2
14	OUTPUT 1

Pin numbers are for dual in-line packages

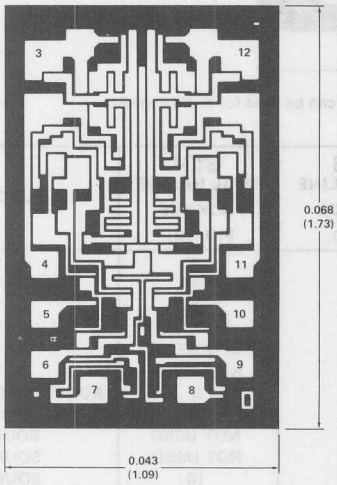
D125



PIN NO.	FUNCTION
1	INPUT 1
2	INPUT 2
3	INPUT 3
4	INPUT 4
5	INPUT 5
6	INPUT 6
7	INPUT 7
8	V_R
9	V– (SUBSTRATE)
10	OUTPUT 4
11	OUTPUT 3
12	OUTPUT 2
13	OUTPUT 1
14	V_L

Pin numbers are for dual in line packages

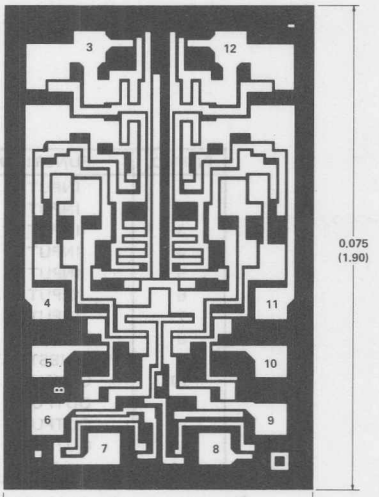
D129



PIN NO.	FUNCTION
3	$\overline{\text{OUT 1}}$
4	OUT 1
5	INPUT 1
6	V+
7	V_L
8	V_R
9	V– (SUBSTRATE)
10	INPUT 2
11	OUT 2
12	$\overline{\text{OUT 2}}$

Pin numbers are for dual in-line packages

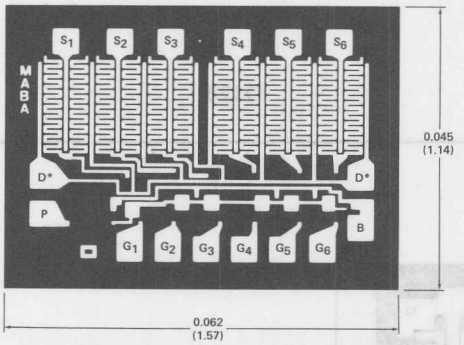
D139



D169

PAD NO.	FUNCTION
3	$\overline{OUT}_1$
4	OUT_1
5	IN_1
6	V+
7	V_L
8	V_R
9	V−
10	IN_2
11	OUT_2
12	$\overline{OUT}_2$

Substrate = V−

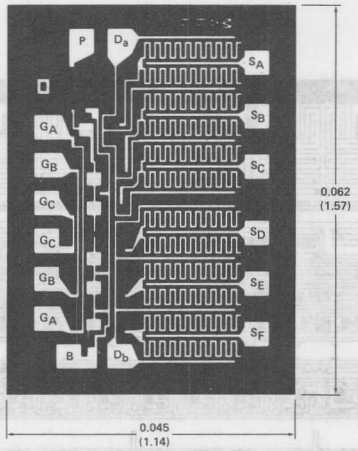


*Both "D" pads are electrically common. Either can be used for drain contact.

PAD	G115 DUAL IN-LINE PACKAGE PIN NO.	G116 DUAL IN-LINE PACKAGE PIN NO.	G117 FLAT PACK PIN NO.	G118 DUAL IN-LINE PACKAGE PIN NO.	G124 DUAL IN-LINE PACKAGE PIN NO.	FUNCTION
†G_1	2	2	3	1	2	GATE 1
†G_2	3	3	4	2	3	GATE 2
†G_3	4	4	5	3	4	GATE 3
†G_4	5	5	6	4	5	GATE 4
†G_5	6	6	7	5	NOT USED	GATE 5
†G_6	7	NOT USED	2	6	NOT USED	GATE 6
B	9	8	8	7	8	BODY (SUBSTRATE) V+
D	16	14	NOT USED	8	14	DRAIN
S_6	10	NOT USED	14**	9	NOT USED	SOURCE 6
S_5	11	9	9	10	NOT USED	SOURCE 5
S_4	12	10	10	11	10	SOURCE 4
S_3	13	11	11	12	11	SOURCE 3
S_2	14	12	12	13	12	SOURCE 2
S_1	15	13	13	14	13	SOURCE 1
P	1	1	1	TIED TO SUBSTRATE	1	PULL UP GATE INPUT

†Any unused gates should be connected to the substrate V+; unused sources can be left open

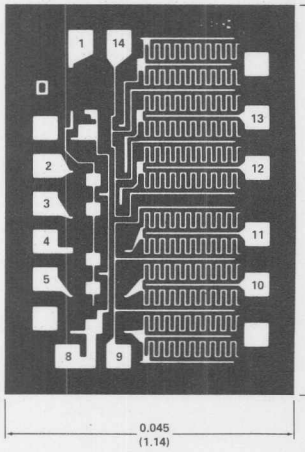
** The G117 uses the S_6 pad as the drain output (pin 14 on package).



PAD	G119		G122	
	FLAT PACK PIN NO.	FUNCTION	FLAT PACK PIN NO.	FUNCTION
G_a	3	GATE 1	3	GATE 2
G_b	4	GATE 3		
G_c	5	GATE 5	†NOT USED	
G_c				
G_b			5	GATE 1
G_a				
B	6	BODY (SUBSTRATE V+)	8	BODY (SUBSTRATE V+)
D_b	7	DRAIN 2	9	DRAIN 1
S_F	9	SOURCE 2	10	SOURCE 1
S_E	10	SOURCE 4	11	SOURCE 2
S_D	11	SOURCE 6	NOT USED	
S_C	12	SOURCE 5	NOT USED	
S_B	13	SOURCE 3	12	SOURCE 3
S_A	14	SOURCE 1	13	SOURCE 4
D_a	1	DRAIN 1	14	DRAIN 2
P	2	PULL UP GATE INPUT	1	PULL UP GATE INPUT

†Any unused gates should be connected to the substrate V+; unused sources can be left open.

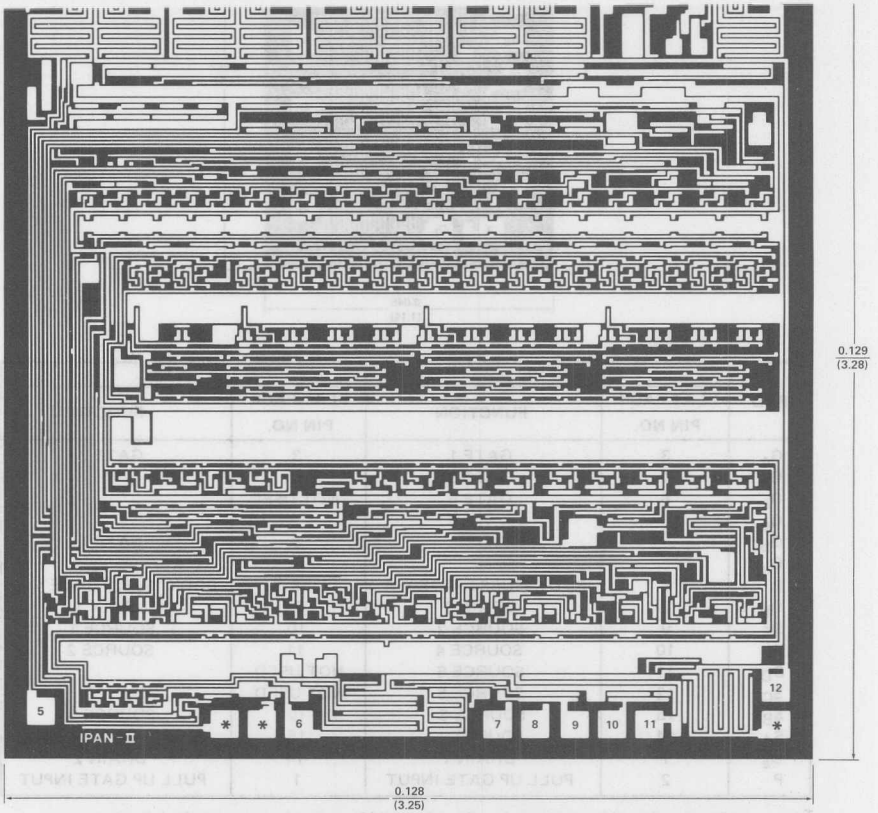
G119
G122



PIN NO.	FUNCTION
1	P (PULL UP GATE INPUT)
2	GATE 1
3	GATE 2
4	GATE 3
5	GATE 4
8	BODY (SUBSTRATE) V+
9	DRAIN 2
10	SOURCE 4
11	SOURCE 3
12	SOURCE 2
13	SOURCE 1
14	DRAIN 1

Pin numbers are for dual in-line packages.

G123



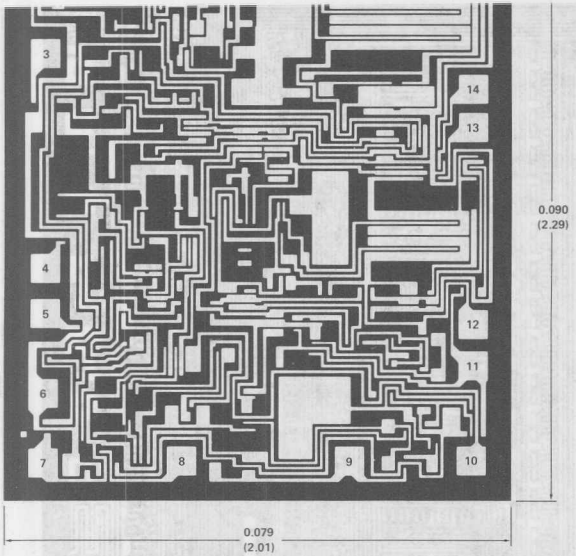
PAD NO.	FUNCTION
1	D_1
2	D_2
3	D_3
4	D_4
5	SIGN
6	V_{SS}
7	CLOCK IN
8	COMP
9	U/D
10	M/Z
11	V_2
12	GND
13	B_4
14	B_3
15	B_2
16	B_1

Substrate = V_{SS}

*Leave unused pads floating

LD110

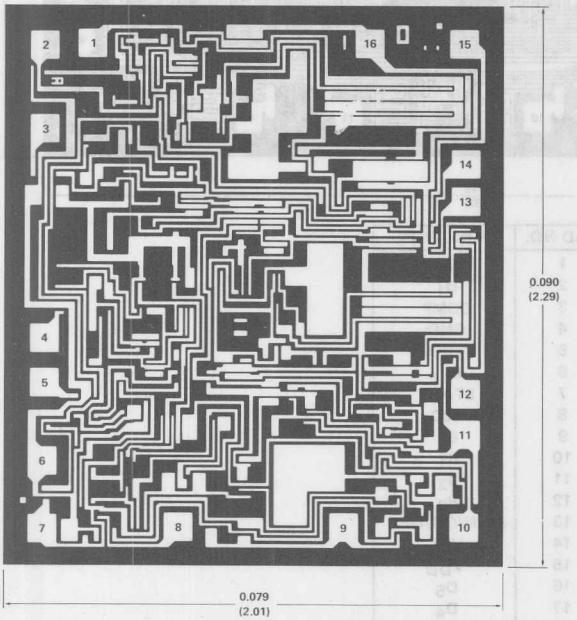
ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



PAD NO.	FUNCTION
1	BUFF OUT
2	HI-Q GND
3	M/Z
4	U/D
5	COMP
6	V_2
7	GND
8	REF OUT
9	INT IN
10	V_{REF}
11	INT OUT
12	AZ OUT
13	AZ FILTER
14	AZ IN
15	V_{IN}
16	V_1

Substrate = V_2

LD111A

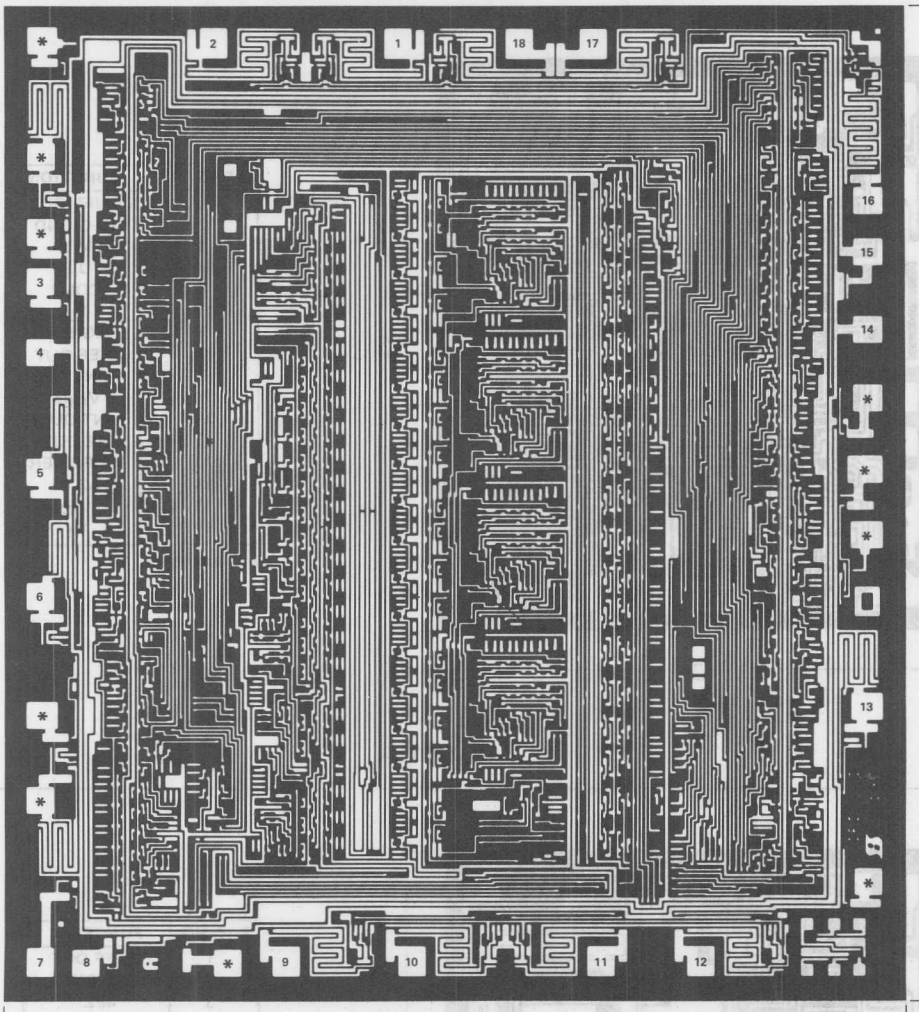


PAD NO.	FUNCTION
1	BUFF OUT
2	HI-Q GND
3	M/Z
4	U/D
5	COMP
6	V^-
7	ANALOG GND
8	REF_{OUT}
9	INT IN
10	V_{REF}
11	INT OUT
12	AZ OUT
13	AZ FILTER
14	AZ IN
15	V_{IN}
16	V^+

Substrate = V^-

LD120

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



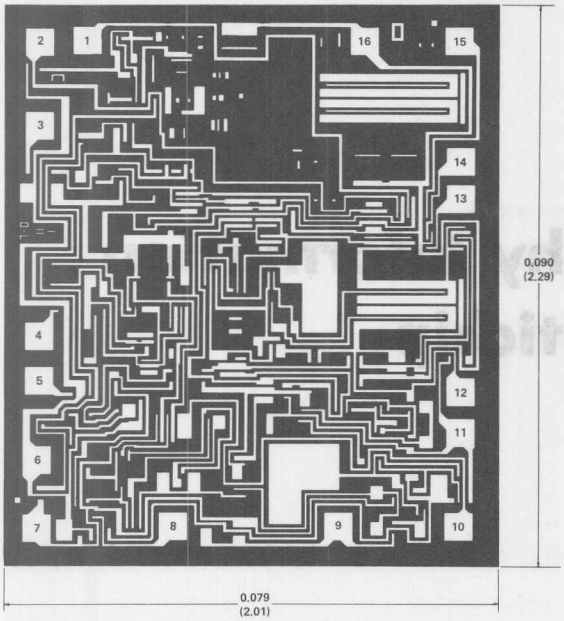
PAD NO.	FUNCTION
1	D_2
2	D_1
3	COMP
4	GND
5	U/D
6	M/Z
7	START
8	OSC
9	B_0
10	B_1
11	B_2
12	B_3
13	SIGN/OR/UR
14	V_{SS}
15	V_{DD}
16	D_5
17	D_4
18	D_3

Substrate = V_{SS}

*Leave unused pads floating

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

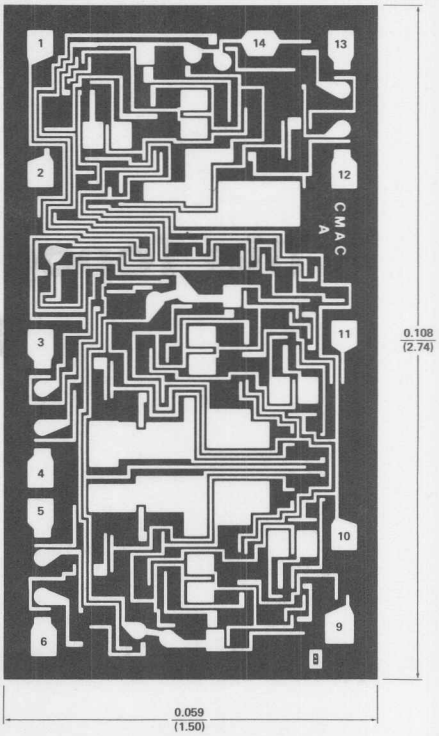
LD121A



PAD NO.	FUNCTION
1	BUFF IN
2	HI-Q GND
3	M/Z
4	U/D
5	COMP
6	V–
7	ANALOG GND
8	REF_{OUT}
9	INT IN
10	V_{REF}
11	INT OUT
12	AZ OUT
13	AZ FILTER
14	AZ IN
15	V_{IN}
16	V+

Substrate = V–

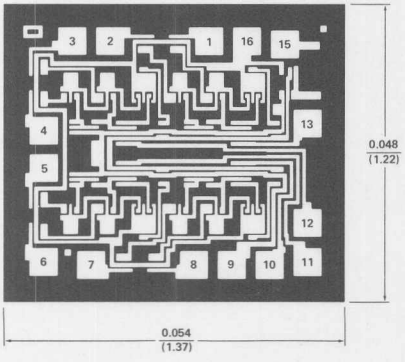
LD122



PAD NO.	FUNCTION
1	SET
2	OUT 1
3	–IN2
4	+IN2
5	+IN3
6	–IN3
9	OUT3
10	$-V_S$
11	OUT2
12	+IN1
13	–IN1
14	$+V_S$

Substrate = $-V_S$

L144



PAD NO.	FUNCTION
1	$+IN_1$
2	$-IN_1$
3	$+IN_2$
4	$-IN_2$
5	$-IN_3$
6	$+IN_3$
7	$-IN_4$
8	$+IN_4$
9	–V
10	OUT_4
11	OUT_3
12	OUT_2
13	OUT_1
15	I_{SET}
16	+V

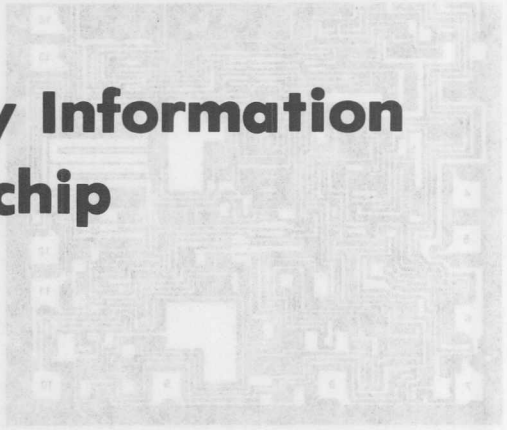
Substrate = –V

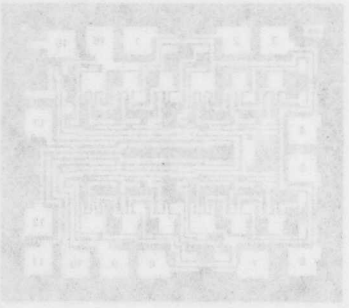
L161

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

Die Topography Information
Multichip







Die Topography Information

Some of Siliconix's analog switches are of multi-chip design with inter-chip connections. The DG123, for example, consists of a separate driver chip (IBAF) and a separate MOS switch chip (MABA). Figure 1 illustrates the bonding arrangement in the DIP package. Note that the two chips are mounted on electrically separate islands. This is due to the different substrate potentials, the MABA substrate is at the positive supply voltage while the EID substrate is at the negative supply voltage.

The JFET switches, for example, are also of multi-chip design. The DG190 consists of a separate driver chip (CMJB) and four separate JFET transistors (NC). Figure 2 illustrates the bonding diagram arrangement in the DIP package. The driver and the JFET switches are mounted so that the substrates are electrically isolated. The substrate of the driver is at the negative supply voltage while the substrate of the JFET switches is the gate connection. A bond wire connects the driver to the JFET gate.

The pin connections for the JFET switch chips can be determined from the chip section and switch pin-out in the data sheet. For example, from the DG190 pin configuration we see that the DG190 has 4 JFETs in one package; D_3 and S_3 are the drain and source of the third JFET.

Die Diagrams/Dimensions

These negative image photos are of the metallization pattern. Scale is ≈32x. Bonding pads are 4 mil (0.10 mm) square, glass-free aluminum metallization. Pad identification numbers correspond to pin numbers for the dual-in-line package on data sheets. The "geometry" is an alpha code used in the factory for identification.

The following pages contain layout, die dimensions and pad identification.

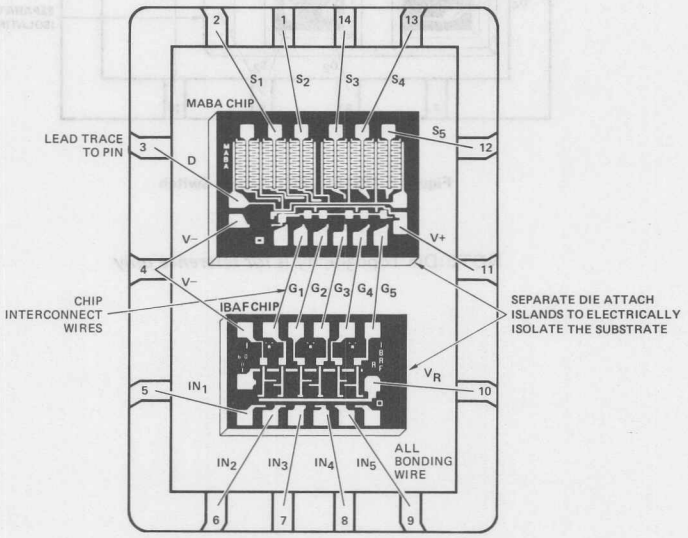


Figure 1. DG123 Analog Switch (Multi-Chip)

Die Topography Information (Continued)

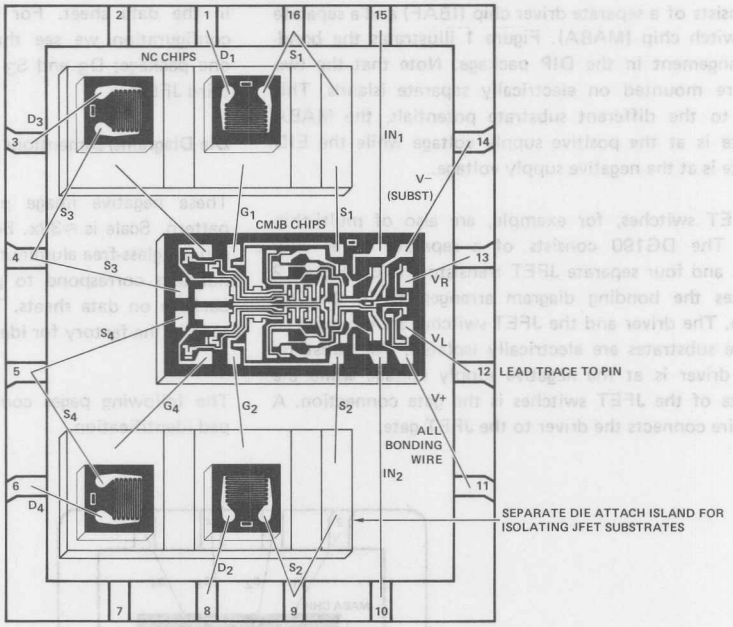


Figure 2. DG190 JFET Analog Switch

NOTE: Die Topography is *for reference only*

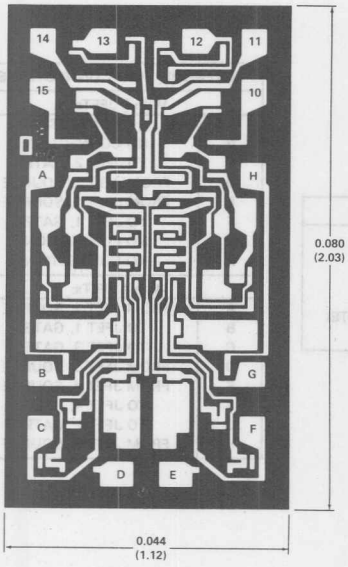
CMJA1000 — DRIVER CHIP CHARACTERISTICS

All parameters are specified under the following conditions: V+ = 15 V, V− = −15 V, V_R = 0 V, V_L = 5 V, T_A = 25°C.

DC PARAMETERS

	Characteristics		Min	Max	Unit	Test Conditions
1	I_{INL}	Input Current Input Voltage Low		-250	μA	V_{IN} = 0 V
2	I_{INH}	Input Current Input Voltage High		20	μA	V_{IN} = 5 V
3	I_L	Logic Supply Current		4.5	mA	V_{IN} = 0 V
4				4.5		V_{IN} = 5 V
5	I_R	Reference Supply Current		-2	mA	V_{IN} = 0 V
6				-2		V_{IN} = 5 V
7	I−	Negative Supply Current		–5.5	mA	V_{IN} = 0 V
8				-4		V_{IN} = 5 V
9	I+	Positive Supply Current		3	mA	V_{IN} = 0 V
10				0.1		V_{IN} = 5 V

V_{IN} = 0.8 V or 2.0 V



PAD NO.	FUNCTION
10	INPUT 2
11	V+
12	V_L
13	V_R
14	V− (SUBSTRATE)
15	INPUT 1

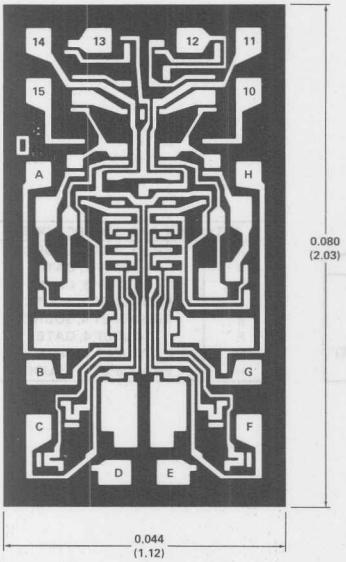
INTERCHIP PAD CONNECTIONS	
A	FROM JFET 1, SOURCE
B	TO JFET 1, GATE
C	TO JFET 3, GATE
D	FROM JFET 3, SOURCE
E	FROM JFET 4, SOURCE
F	TO JFET 4, GATE
G	TO JFET 2, GATE
H	FROM JFET 2, SOURCE

CMJA1000 is used for following devices:

DEVICE	JFET USED	NO. OF JFETs
DG183	NIP1000	4
DG184	NC1000	4
DG185	NC2000	4
DG284	NH1000	4

	Characteristics		Min	Max	Unit	Test Conditions
1	I_{INL}	Input Current Input Voltage Low		-250	μA	$V_{IN} = 0$ V
2	I_{INH}	Input Current Input Voltage High		20	μA	$V_{IN} = 5$ V
3	I_L	Logic Supply Current		4.5	mA	$V_{IN} = 0$ V
4				4.5		$V_{IN} = 5$ V
5	I_R	Reference Supply Current		-2	mA	$V_{IN} = 0$ V
6				-2		$V_{IN} = 5$ V
7	I−	Negative Supply Current		-5	mA	$V_{IN} = 0$ V
8				-5		$V_{IN} = 5$ V
9	I+	Positive Supply Current		1.5	mA	$V_{IN} = 0$ V
10				1.5		$V_{IN} = 5$ V

V_{IN} = 0.8 V or 2.0 V



PAD NO.	FUNCTION
10	INPUT 2
11	V+
12	V_L
13	V_R
14	V− (SUBSTRATE)
15	INPUT 1

INTERCHIP PAD CONNECTIONS	
With 2 JFETs:	
A	NO CONNECTION
B	NO CONNECTION
C	TO JFET 2, GATE
D	FROM JFET 2, SOURCE
E	FROM JFET 1, SOURCE
F	TO JFET 1, GATE
G	NO CONNECTION
H	NO CONNECTION
With 4 JFETs:	
A	FROM JFET 1, SOURCE
B	TO JFET 1, GATE
C	TO JFET 3, GATE
D	FROM JFET 3, SOURCE
E	FROM JFET 4, SOURCE
F	TO JFET 4, GATE
G	TO JFET 2, GATE
H	FROM JFET 2, SOURCE

CMJB1000 is used for following devices:

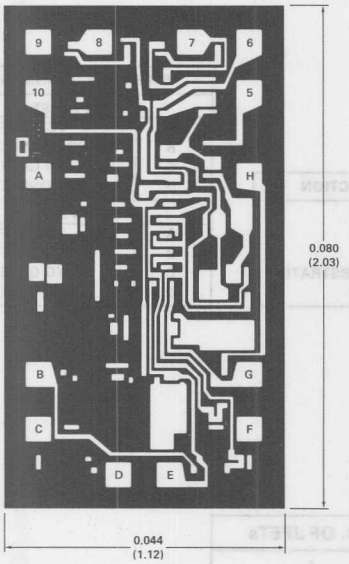
DEVICE	JFET USED	NO. OF JFETs
DG180	NIP1000	2
DG181	NC1000	2
DG182	NC2000	2
DG189	NIP1000	4
DG190	NC1000	4
DG191	NC2000	4
DG281	NH1000	2
DG290	NH1000	4

CMJC1000 — DRIVER CHIP CHARACTERISTICS

All parameters are specified under the following conditions: $V+ = 15$ V, $V- = -15$ V, $V_R = 0$ V, $V_L = 5$ V, $T_A = 25°C$.

DC PARAMETERS

	Characteristics		Min	Max	Unit	Test Conditions
1	I_{INL}	Input Current Input Voltage Low		-250	μA	$V_{IN} = 0$ V
2	I_{INH}	Input Current Input Voltage High		10	μA	$V_{IN} = 5$ V
3	I_L	Logic Supply Current		3.2	mA	$V_{IN} = 0$ V
4				3.2		$V_{IN} = 5$ V
5	I_R	Reference Supply Current		-2	mA	$V_{IN} = 0$ V
6				-2		$V_{IN} = 5$ V
7	I−	Negative Supply Current		-3	mA	$V_{IN} = 0$ V
8				-3		$V_{IN} = 5$ V
9	I+	Positive Supply Current		0.8	mA	$V_{IN} = 0$ V
10				0.8		$V_{IN} = 5$ V



PAD NO.	FUNCTION
5	INPUT 1
6	V+
7	V_L
8	V_R
9	NOT CONNECTED
10	V− (SUBSTRATE)

INTERCHIP PAD CONNECTIONS	
A	NOT CONNECTED
B	FROM JFET 2, SOURCE
C	NOT CONNECTED
D	NOT CONNECTED
E	TO JFET 2, GATE
F	NOT CONNECTED
G	TO JFET 1, GATE
H	FROM JFET 1, SOURCE

CMJC1000 is used for following devices:

DEVICE	JFET USED	NO. OF JFETs
DG186	NIP1000	2
DG187	NC1000	2
DG188	NC2000	2
DG287	NH1000	2

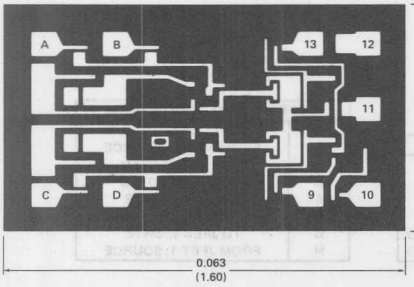
LODC1000 — DRIVER CHIP CHARACTERISTICS

All parameters are specified under the following conditions: V+ = +12 V, V− = −18 V, V_R = 0 V, T_A = 25°C.

DC PARAMETERS

	Characteristics		Min	Max	Unit	Test Conditions
1	I_{INL}	Input Current Input Voltage Low		0.1	μA	V_{IN} = 0.8 V
2	I_{INH}	Input Current Input Voltage High		100	μA	V_{IN} = 2.5 V
3	I+	Positive Supply Current		3.3	μA	V_{IN} = 2.5 V, One Channel On
4	I−	Negative Supply Current		-2.0	μA	
5	I_R	Reference Supply Current		-1.5	μA	
6	I+	Positive Supply Current		25	μA	Both V_{IN} = 0 V, All Channels Off
7	I−	Negative Supply Current		-25	μA	
8	I_R	Reference Supply Current		-25	μA	

NOTES:
1. V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μS.
2. The supply voltage condition of +12 V/ −18 V is standard test condition. Specs will also be met with +15 V/ −15 V supplies, but are not tested.



PAD NO.	FUNCTION
9	INPUT 1
10	V_R
11	V+
12	V− (SUBSTRATE)
13	INPUT 2

INTERCHIP CONNECTIONS	
With 2 JFETs:	
A	TO GATE 2
B	NO CONNECTION
C	TO GATE 1
D	NO CONNECTION
With 4 JFETs:	
A	TO GATE 4
B	TO GATE 2
C	TO GATE 3
D	TO GATE 1

LODC1000 is used for following devices:

DEVICE	JFET USED	NO. OF JFETs
DG126	NC2000	4
DG129	NC1000	4
DG133	NC1000	2
DG134	NC2000	2
DG140	NIP1000	4
DG141	NIP1000	2
DG151	NIP1000	2
DG152	NC1000	2
DG153	NIP1000	4
DG154	NC1000	4

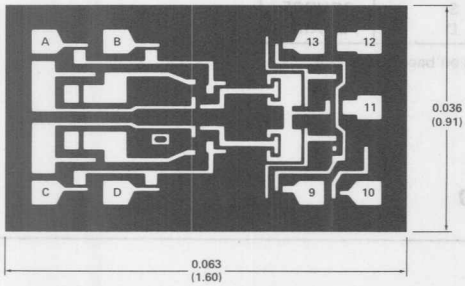
LODF1000 — DRIVER CHIP CHARACTERISTICS

All parameters are specified under the following conditions: V+ = +12 V, V− = −18 V, V_R = 0 V, V_{IN2} = 2.5 V unless otherwise noted, T_A = 25°C.

DC PARAMETERS

	Characteristics		Min	Max	Unit	Test Conditions
1	I_{INL1}	Input Current		0.1	μA	V_{IN1} = 2 V, V_{IN2} = 2.5 V
	I_{INL2}	Input Voltage Low		0.1		V_{IN1} = 2.5 V, V_{IN2} = 2 V
2	I_{INH1}	Input Current		100	μA	V_{IN1} = 3 V, V_{IN2} = 2.5 V
	I_{INH2}	Input Voltage High		100		V_{IN1} = 2.5 V, V_{IN2} = 3 V
3	I+	Positive Supply Current		4.5	μA	V_{IN1} = 2 V or V_{IN1} = 3 V, One Channel On
4	I−	Negative Supply Current		-2.2	μA	
5	I_R	Reference Supply Current		-2.4	μA	
6	I+	Positive Supply Current		25	μA	V_{IN1} = V_{IN2} = 0.8 V, All Channels Off
7	I−	Negative Supply Current		-25	μA	
8	I_R	Reference Supply Current		-25	μA	

NOTES:
1. V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μS.
2. The supply voltage condition of +12 V/ − 18 V is standard test condition. Specs will also be met with +15 V/ − 15 V supplies, but are not tested.



PAD NO.	FUNCTION
9	INPUT 1
10	V_R
11	V+
12	V− (SUBSTRATE)
13	INPUT 2

INTERCHIP CONNECTIONS	
With 2 JFETs:	
A	TO GATE 2
B	NO CONNECTION
C	TO GATE 1
D	NO CONNECTION
With 4 JFETs:	
A	TO GATE 4
B	TO GATE 2
C	TO GATE 3
D	TO GATE 1

LODF1000 is used for following devices:

DEVICE	JFET USED	NO. OF JFETs
DG139	NC1000	4
DG142	NC2000	4
DG143	NC2000	2
DG144	NC1000	2
DG145	NIP1000	4
DG146	NIP1000	2
DG161	NIP1000	2
DG162	NC1000	2
DG163	NIP1000	4
DG164	NC1000	4

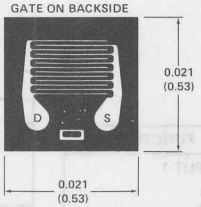
NC1000 JFET SWITCH CHARACTERISTICS

2	$I_{D(off)}$	Drain Cut Off Current		1.0	nA	$V_{DS} = 22$ V, $V_{GS} = -6.2$ V
3	$I_{S(off)}$	Source Cut Off Current		1.0	nA	$V_{DS} = 22$ V, $V_{GS} = -6.2$ V
4	$r_{DS(on)}$	Drain Source-ON Resistance		30	Ω	$V_{GS} = 0$ V, $G_{DS} = 0.2$ V

NC2000 JFET SWITCH CHARACTERISTICS

DC PARAMETERS $T_A = 25°C$

Characteristics			Min	Max	Unit	Test Conditions
1	BV_{GDS}	Gate-Drain Breakdown Voltage	-35		V	$I_G = -1\ \mu A$
2	$I_{D(off)}$	Drain Cut Off Current		1.0	nA	$V_{DS} = 22$ V, $V_{GS} = -3.9$ V
3	$I_{S(off)}$	Source Cut Off Current		1.0	nA	$V_{DS} = 22$ V, $V_{GS} = -3.9$ V
4	$r_{DS(on)}$	Drain Source-ON Resistance		75	Ω	$V_{GS} = 0$ V, $G_{DS} = 0.2$ V



INTERCHIP CONNECTIONS	FUNCTION
S	SOURCE
D	DRAIN

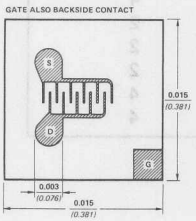
Gate is on backside of chip

NC1000/NC2000

NH1000 JFET SWITCH CHARACTERISTICS

DC PARAMETERS $T_A = 25°C$

Characteristics			Min	Max	Unit	Test Conditions
1	BV_{GDS}	Gate-Drain Breakdown Voltage	-33		V	$I_G = -1\ \mu A$
2	$I_{D(off)}$	Drain Cut Off Current		200	pA	$V_{DS} = 22$ V, $V_{GS} = -6.2$ V
3	$I_{S(off)}$	Source Cut Off Current		200	pA	$V_{DS} = 22$ V, $V_{GS} = -6.2$ V
4	$r_{DS(on)}$	Drain Source-ON Resistance		300	Ω	$V_{GS} = 0$ V, $G_{DS} = 0.2$ V



INTERCHIP PAD CONNECTIONS	FUNCTION
S	SOURCE
D	DRAIN
G	GATE

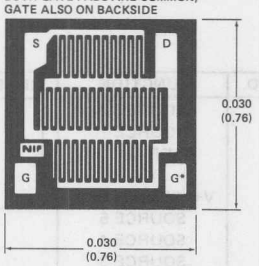
300 Ω
JFET SWITCH CHIP

NIP1000 JFET SWITCH CHARACTERISTICS

DC PARAMETERS $T_A = 25°C$

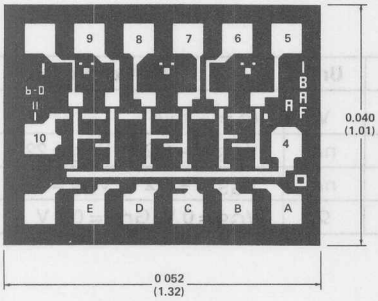
	Characteristics		Min	Max	Unit	Test Conditions
1	BV_{GDS}	Gate-Drain Breakdown Voltage	-33		V	$I_G = -1\ \mu A$
2	$I_{D(off)}$	Drain Cut Off Current		10	nA	$V_{GS} = -6.2$ V, $V_{DS} = 22$ V
3	$I_{S(off)}$	Source Cut Off Current		10	nA	$V_{GS} = -6.2$ V, $V_{DS} = -22$ V
4	$r_{DS(on)}$	Drain Source		10	Ω	$V_{GS} = 0$ V, $G_{DS} = 0.2$ V

BOTH GATE PADS ARE COMMON, GATE ALSO ON BACKSIDE



INTERCHIP PAD CONNECTIONS	FUNCTION
S	SOURCE
D	DRAIN
G	GATE

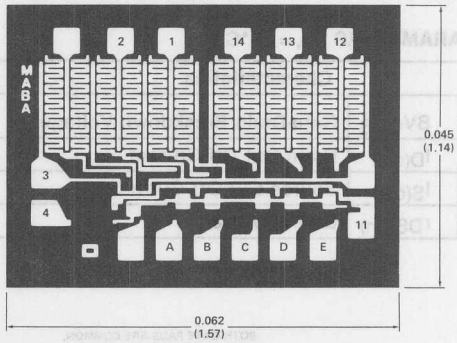
*Either gate pad can be used, backside is also gate



PIN NO.	FUNCTION
4	V– (SUBSTRATE)
5	INPUT 1
6	INPUT 2
7	INPUT 3
8	INPUT 4
9	INPUT 5
10	V_R

INTERCHIP PAD CONNECTIONS	
A	TO GATE 1
B	TO GATE 2
C	TO GATE 3
D	TO GATE 4
E	TO GATE 5

DRIVER CHIP



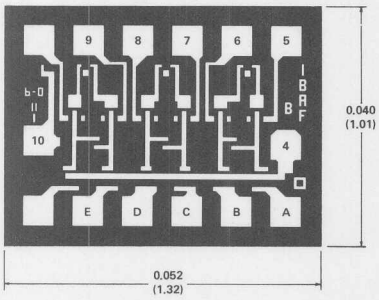
PIN NO.	FUNCTION
1	SOURCE 2
2	SOURCE 1
3	DRAIN
4	V–
11	V+ (SUBSTRATE)
12	SOURCE 5
13	SOURCE 4
14	SOURCE 3

INTERCHIP PAD CONNECTIONS	
A	GATE 1
B	GATE 2
C	GATE 3
D	GATE 4
E	GATE 5

Pin numbers are for dual in-line packages

MOS SWITCH CHIP

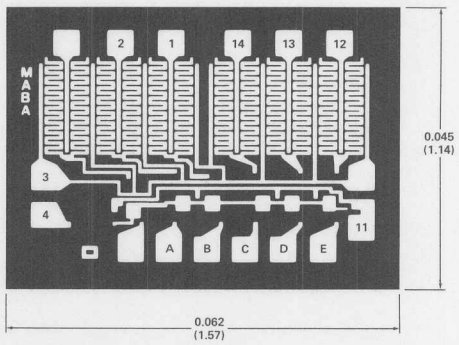
DG123



PIN NO.	FUNCTION
4	V– (SUBSTRATE)
5	INPUT 1
6	INPUT 2
7	INPUT 3
8	INPUT 4
9	INPUT 5
10	V_L

INTERCHIP PAD CONNECTIONS	
A	TO GATE 1
B	TO GATE 2
C	TO GATE 3
D	TO GATE 4
E	TO GATE 5

DRIVER CHIP



PIN NO.	FUNCTION
1	SOURCE 2
2	SOURCE 1
3	DRAIN
4	V–
11	V+ (SUBSTRATE)
12	SOURCE 5
13	SOURCE 4
14	SOURCE 3

INTERCHIP PAD CONNECTIONS	
A	GATE 1
B	GATE 2
C	GATE 3
D	GATE 4
E	GATE 5

Pin numbers are for dual in-line packages

MOS SWITCH CHIP

DG125

Siliconix

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Burn-In Pin Connections

The following table lists the standard Burn-In Pin Connections for most Siliconix Integrated Circuits. Devices are listed in Alpha-Numerical order according to package type. Following the tables are two examples illustrating Burn-In Pin Connections for different switches and packages.

Part Type	Package Type*	Pins																	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
D129	P/L	(7)	(7)	(7)	GND	(7)	(7)	10K→ +5 V	GND	−30 V	(13)	(13)	(13)	10K→ +5 V	+5 V				
D123/ D125	P/L	−30 V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K→ GND				
D139 D169	P/L	—	—	10K→ Pin 4	10K→ Pin 3	+5 V	+10 V	+5 V	GND	−20 V	GND	10K→ Pin 12	10K→ Pin 11	—	—				
DG123	P/L	GND	GND	GND	−20 V	4.7K→ +5 V	4.7K→ +5 V	4.7K→ +5 V	4.7K→ +5 V	4.7K→ +5 V	GND	+5 V	GND	GND	GND				
DG125	P/L	GND	GND	GND	−20 V	GND	GND	GND	GND	GND	+5 V	+5 V	GND	GND	GND				
DG126 DG129 DG133 DG134 DG139 DG140 DG141 DG142 DG143 DG144 DG145 DG146 DG151 DG152 DG153 DG154 DG161 DG162 DG163 DG164	P/L	10K→ GND	+10 V	10K→ GND	—	+10 V	10K→ GND	10K→ GND	+10 V	GND	GND	+10 V	−20 V	GND	+10 V				
DG172	P/L	To Pin 14	GND	GND	—	−20 V	GND	+5 V	+5 V	+5 V	+5 V	GND	+5 V	To Pin 14	7.5K→ −20 V				
DG180 DG181 DG182 DG186 DG187 DG188 DG281	A	+15 V	10K→ GND	GND	+15 V	+5 V	GND	−15 V	GND	10K→ GND	+15 V								
DG180 DG181 DG182 DG281	P/L	+15 V	10K→ GND	—	—	GND	+15 V	+5 V	GND	−15 V	GND	—	—	10K→ GND	+15 V				
DG183 DG184 DG185 DG189 DG190 DG191 DG284 DG290	P	10K→ GND	—	10K→ GND	−15 V	−15 V	10K→ GND	—	10K→ GND	+15 V	GND	+15 V	+5 V	GND	−15 V	GND	+15 V		

Parentheses indicate direct connection to indicated pin i.e., (2) = connect to pin 2; All voltages ±5%.

*Package types: P = All Dual-In-Line Packages, L = All Flat Packages, A = All 10-Lead TO-5s, R = 28 Pin Dual-In-Line Packages.

Burn-In Pin Connections (Continued)

Part Type	Package Type*	Pins 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
DG183 DG184 DG185	L																		
DG186 DG187 DG188	P/L	−15 V	10K→ GND	10K→ GND	+15 V	GND	+15 V	+5 V	GND	−15 V	GND	+15 V	10K→ GND	10K→ GND	−15 V				
DG189 DG190 DG191 DG284 DG290	L																		
DG200	A	+15 V	+15 V	GND	(9)	(9)	−15 V	—	(9)	10K→ GND	+15 V								
DG200A	P/L	+15 V	—	GND	—	(10)	(10)	−15 V	—	(10)	10K→ GND	—	+15 V	—	+15 V				
DG201 DG201A	P/L	+15 V	(15)	(15)	−15 V	GND	(15)	(15)	+15 V	+15 V	(15)	(15)	—	+15 V	(15)	10K→ GND	+15 V		
DG211	P	+15 V	(15)	(15)	−15 V	GND	(15)	(15)	+15 V	+15 V	(15)	(15)	+5 V	+15 V	(15)	10K→ GND	+15V		
DG300 DG300A DG301 DG301A DG304 DG304A DG305 DG305A	A	(9)	(9)	GND	—	GND	−15 V	GND	(9)	10K→ GND	+15 V								
DG300 DG300A DG301 DG301A DG302 DG302A DG303 DG303A DG304 DG304A DG305 DG305A DG306 DG306A DG307 DG307A	P/L	—	(13)	(13)	(13)	(13)	GND	GND	−15 V	GND	(13)	(13)	(13)	10K→ GND	+15 V				
DG308 DG308A	P	+15 V	(15)	(15)	−15 V	GND	(15)	(15)	+15 V	+15 V	(15)	(15)	—	+15 V	(15)	10K→ GND	+15 V		
DG381 DG381A	A/P	See DG181																	
DG384 DG384A	A/P	See DG184																	
DG387 DG387A	A/P	See DG187																	
DG390 DG390A	A/P	See DG190																	
DG501 DG503 SI3705	P/L	(16)	(4)	(4)	+10 V	(12)	(12)	(12)	(12)	(12)	(12)	(12)	−10 V	−15 V	(16)	(16)	GND		
DG506 DG506A DG507	R	1 +15 V 15	2 (28) 16	3 — 17	4 (28) 18	5 (28) 19	6 (28) 20	7 (28) 21	8 (28) 22	9 (28) 23	10 (28) 24	11 (28) 25	12 GND 26	13 — 27	14 GND 28	—	28 Pins		
DG507A		GND	GND	GND	GND	(28)	(28)	(28)	(28)	(28)	(28)	(28)	(28)	−15 V	10K→ GND				
DG508 DG508A	P/L	GND	GND	−15 V	(12)	(12)	(12)	(12)	(12)	(12)	(12)	(12)	10K→ GND	+15 V	GND	GND	GND		
DG509 DG509A	P/L	GND	GND	−15 V	(13)	(13)	(13)	(13)	(13)	(13)	(13)	(13)	(13)	10K→ GND	+15 V	GND	GND		

Parentheses indicate direct connection to indicated pin i.e., (2) = connect to pin 2; All voltages ±5%.

*Package types: P = All Dual-In-Line Packages, L = All Flat Packages, A = All 10-Lead TO-5s, R = 28 Pin Dual-In-Line Packages.

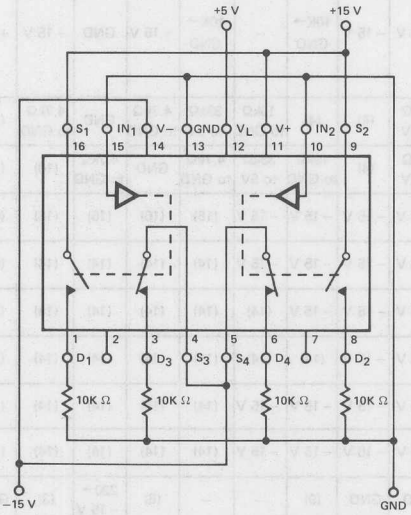
Burn-In Pin Connections (Continued)

Part Type	Package Type*	Pins 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
DG528	P	GND	GND	GND	−15 V	(13)	(13)	(13)	(13)	(13)	(13)	(13)	(13)	10K→ GND	+15 V	GND	GND	GND	GND
DG529	P	GND	GND	GND	−15 V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K→ GND	+15 V	GND	GND	GND
DG5040 DG5041 DG5042 DG5043 DG5044 DG5045	P	10K→ GND	—	10K→ GND	−15 V	−15 V	10K→ GND	—	10K→ GND	+15 V	GND	+15 V	+5 V	GND	−15 V	GND	+15 V		
DF320	P/J	33Ω to 5V	4.7kΩ to 5V	4.7kΩ to 5V	10kΩ to 5V	(4)	(4)	10kΩ to GND	33kΩ to 5V	4.7kΩ to GND	GND	4.7kΩ to GND	(11)	(11)	(11)	(11)	(11)	(11)	(11)
DF328	P/J	33Ω to 5V	4.7kΩ to 5V	4.7kΩ to 5V	10kΩ to 5V	(4)	10kΩ to GND	33kΩ to 5V	4.7kΩ to GND	GND	4.7kΩ to GND	(10)	(10)	(10)	(10)	(10)	(10)		
G115	P/L	(16)	−15 V	−15 V	−15 V	−15 V	−15 V	−15 V	(16)	(16)	(16)	(16)	(16)	(16)	(16)	(16)	10k→ +10 V		
G116	P/L	(14)	−15 V	−15 V	−15 V	−15 V	−15 V	−15 V	(14)	(14)	(14)	(14)	(14)	(14)	10K→ +10 V				
G118	P/L	−15 V	−15 V	−15 V	−15 V	−15 V	−15 V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K→ +10 V				
G119	P/L	(14)	(14)	−15 V	−15 V	−15 V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K→ +10 V				
G122	P/L	(14)	−15 V	−15 V	−15 V	−15 V	−15 V	−15 V	(14)	(14)	(14)	(14)	(14)	(14)	10K→ +10 V				
G123	P/L	(14)	−15 V	−15 V	−15 V	−15 V	−15 V	−15 V	(14)	(14)	(14)	(14)	(14)	(14)	10K→ +10 V				
L144	P/L	3MΩ→ +15 V	(13)	(11)	GND	GND	(9)	—	—	(6)	220→ −15 V	(3)	GND	(2)	→ +15 V				
L161	P	−15 V	+15 V	−15 V	+15 V	−15 V	+15 V	−15 V	+15 V	−15 V	—	—	—	—	—	3MΩ→ +15 V	+15 V		

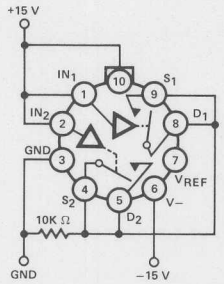
Parentheses indicate direct connection to indicated pin i.e., (2) = connect to pin 2; All voltages ±5%.
*Package types: P = All Dual-In-Line Packages, L = All Flat Packages, A = All 10-Lead TO-5s, R = 28 Pin Dual-In-Line Packages.

Burn-In Pin Connections (Continued)

Examples of Burn-In Circuit Configurations



DG190/DG191 (PACKAGE TYPE P)



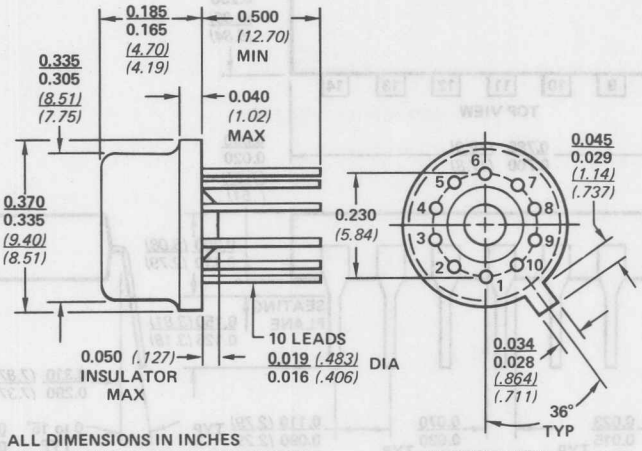
DG200 (PACKAGE TYPE A)

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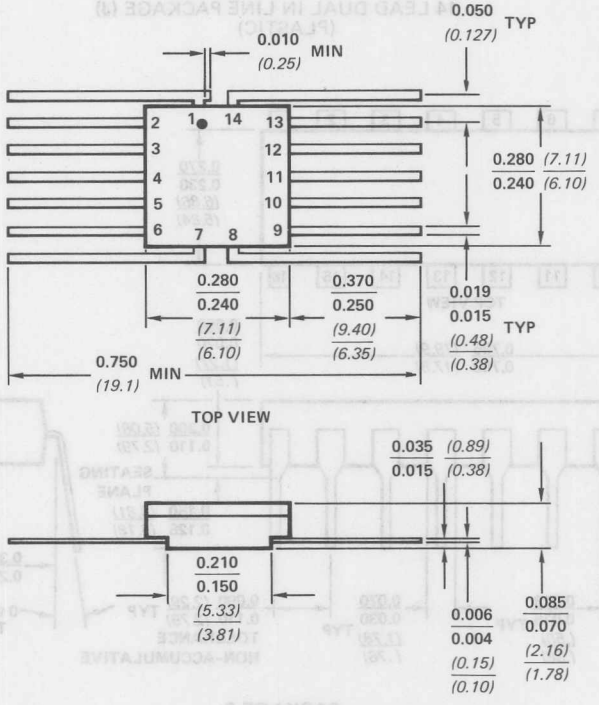
Index

PACKAGE DATA

Package	Letter Code	Package Type	Page
2	A	10 Lead Metal Can	11-1
5	L	14 Lead Bottom-Braze Flatpack	11-1
7	J	14 Pin Plastic Dual-In-Line	11-2
8	J	16 Pin Plastic Dual-In-Line	11-2
9	K	14 Pin Cerdip Dual-In-Line	11-3
10	K	16 Pin Cerdip Dual-In-Line	11-3
11	P	14 Pin Side-Braze Dual-In-Line	11-4
12	P	16 Pin Side-Braze Dual-In-Line	11-4
13	R	28 Pin Side-Braze Dual-In-Line	11-5
14	J	28 Pin Plastic Dual-In-Line	11-5
16	L	14 Lead Bottom-Brace Flatpack	11-6
17	L	16 Lead Bottom-Braze Flatpack	11-6
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19	J	18 Pin Plastic Dual-In-Line	11-8
20	P	18 Pin Side-Braze Dual-In-Line	11-8
22	J	40 Pin Plastic Dual-In-Line	11-9
23	K	18 Pin Cerdip Dual-In-Line	11-9



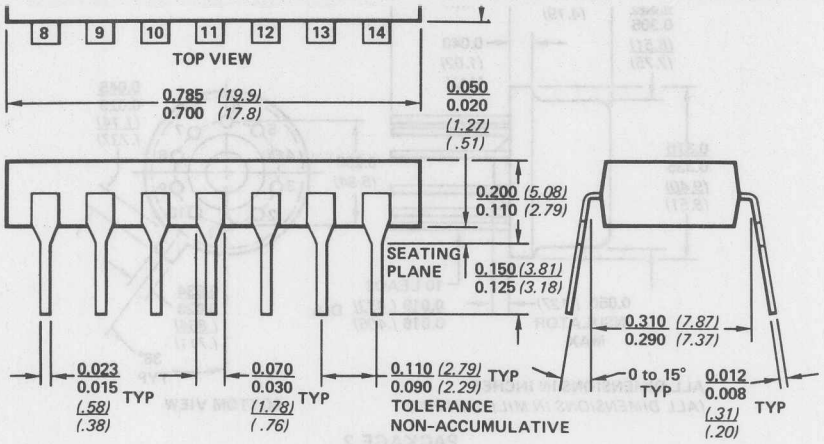
PACKAGE 2
10 LEAD TO-100 TYPE METAL CAN (A)



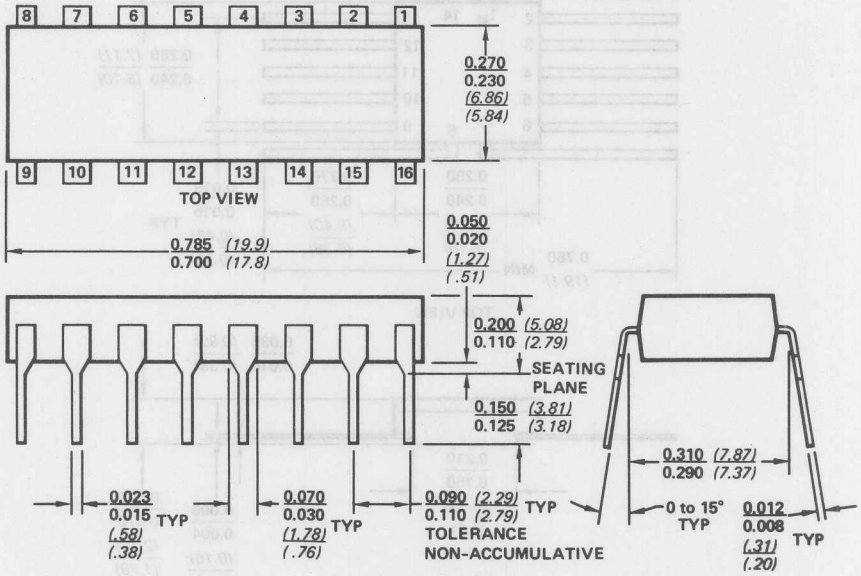
PACKAGE 5
14 LEAD FLATPAC (L)
(BOTTOM BRAZE)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



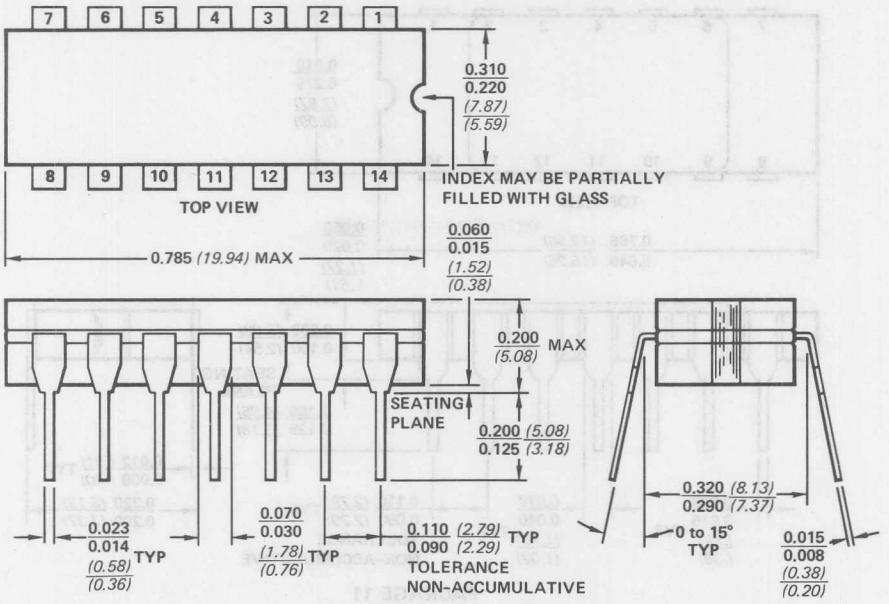
PACKAGE 7
14 LEAD DUAL IN LINE PACKAGE (J)
(PLASTIC)



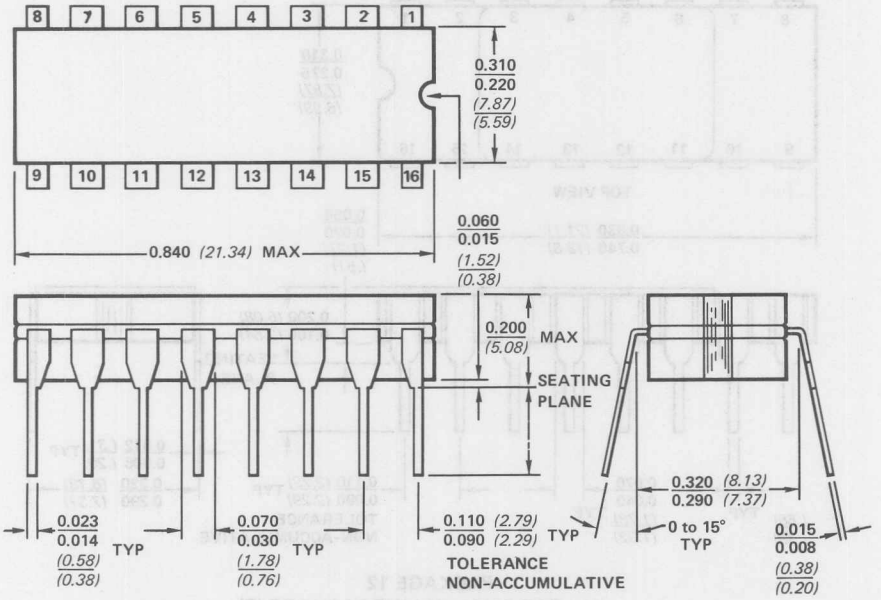
PACKAGE 8
16 LEAD DUAL IN LINE PACKAGE(J)
(PLASTIC)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



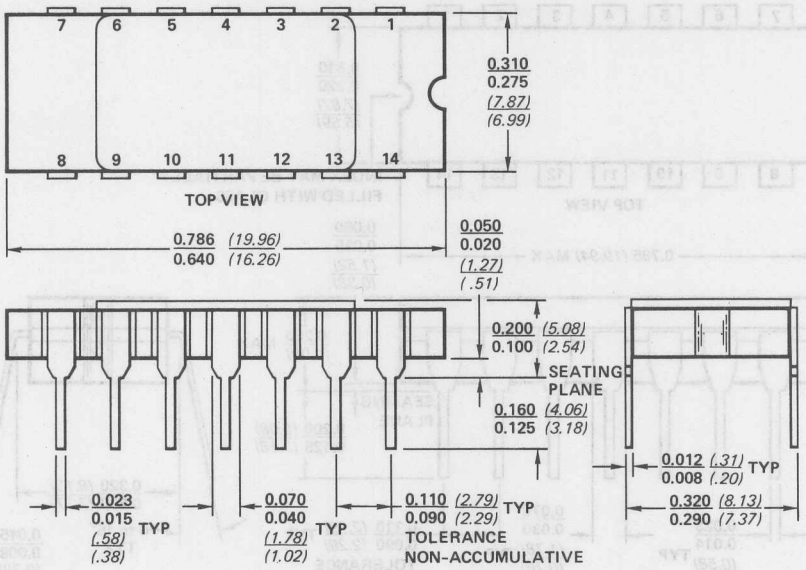
PACKAGE 9
14 LEAD DUAL IN LINE PACKAGE (K)
(CERDIP)



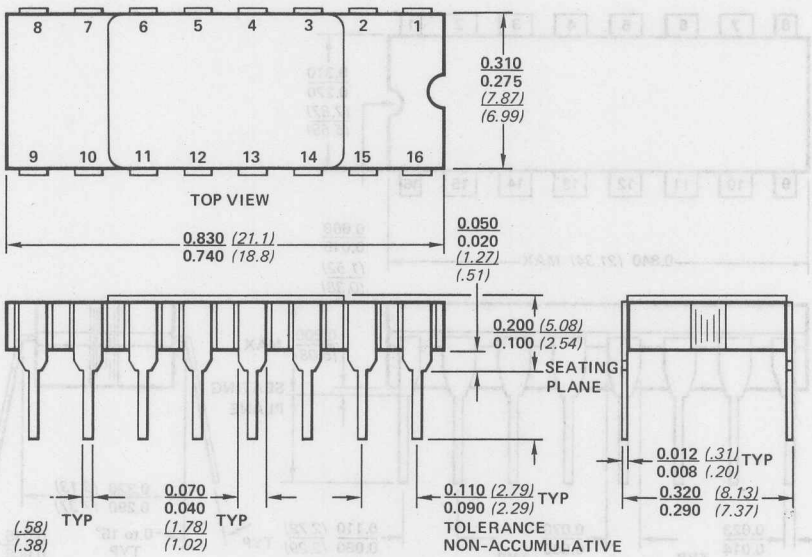
PACKAGE 10
16 LEAD DUAL IN LINE PACKAGE (K)
(CERDIP)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



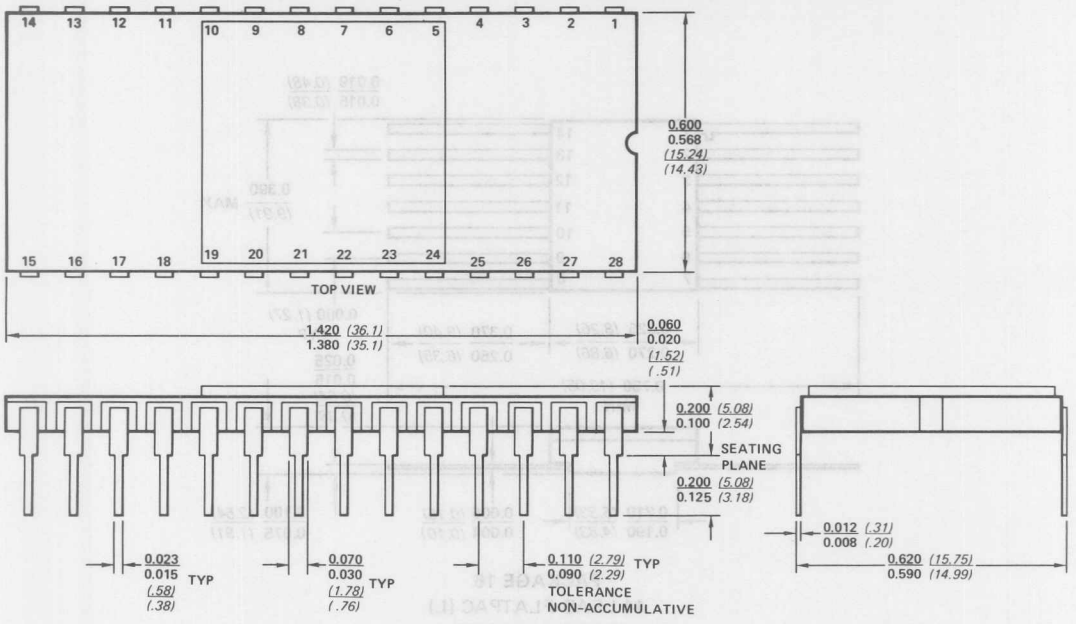
PACKAGE 11
14 LEAD DUAL IN LINE PACKAGE (P)
(SIDE BRAZE)



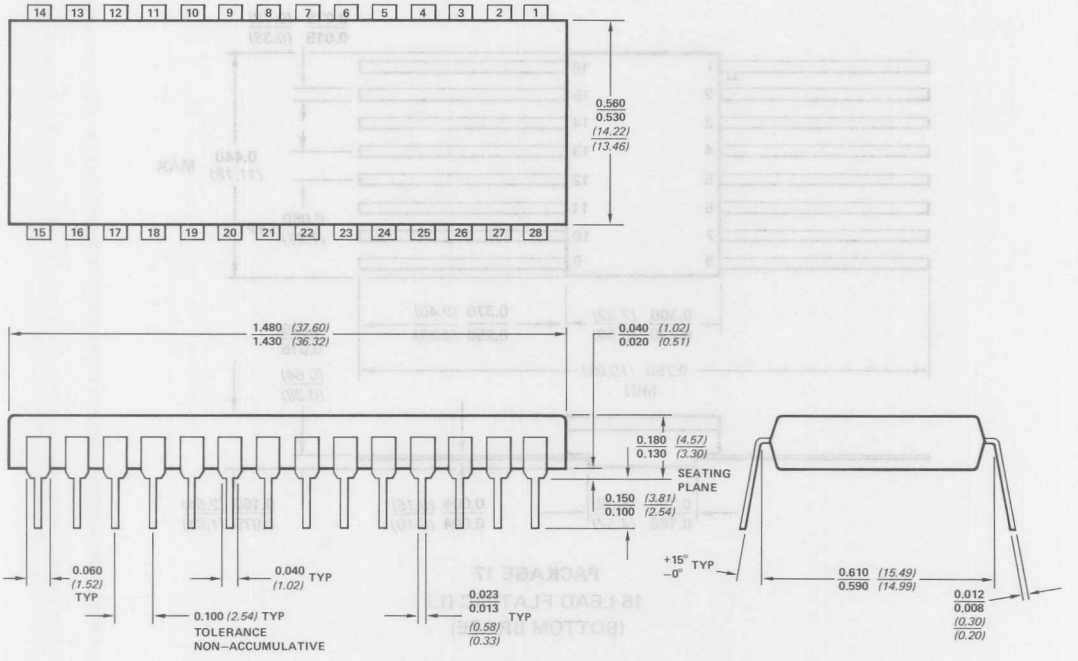
PACKAGE 12
16 LEAD DUAL IN LINE PACKAGE (P)
(SIDE BRAZE)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



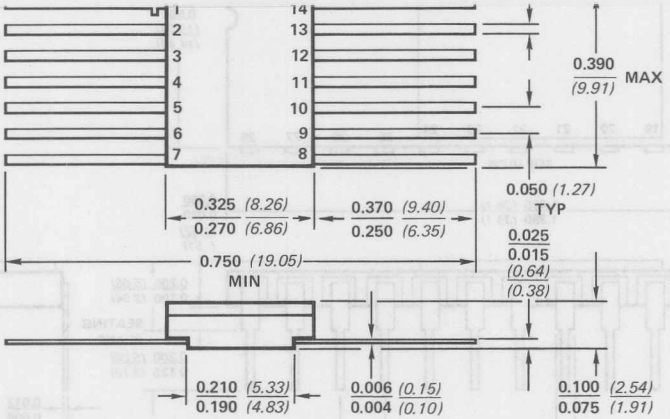
PACKAGE 13
28 LEAD DUAL IN LINE PACKAGE (R)
(SIDE BRAZE)



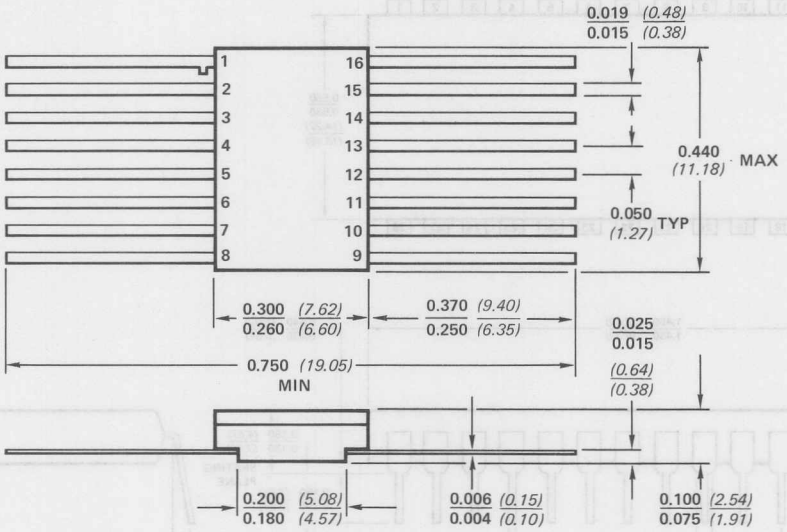
PACKAGE 14
28 LEAD DUAL IN-LINE PACKAGE (J)
(PLASTIC)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM



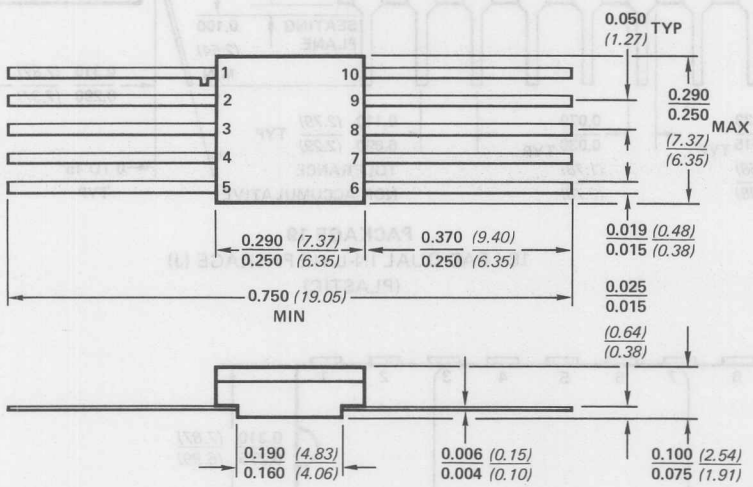
PACKAGE 16
14 LEAD FLATPAC **(L)**
(BOTTOM BRAZE)



PACKAGE 17
16 LEAD FLATPAC **(L)**
(BOTTOM BRAZE)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

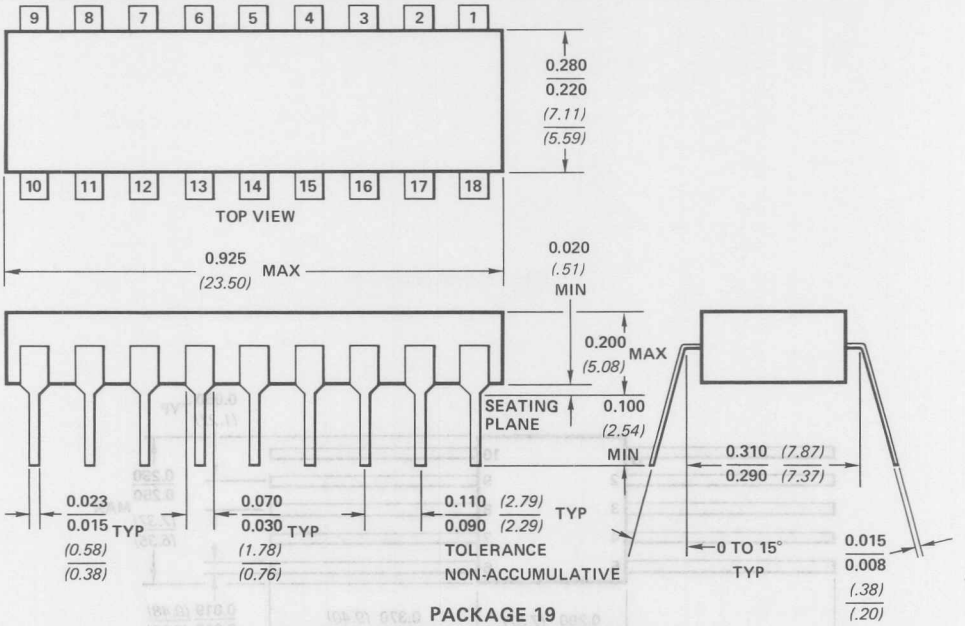


PACKAGE 18
10 LEAD FLATPAC **(L)**
(BOTTOM BRAZE)

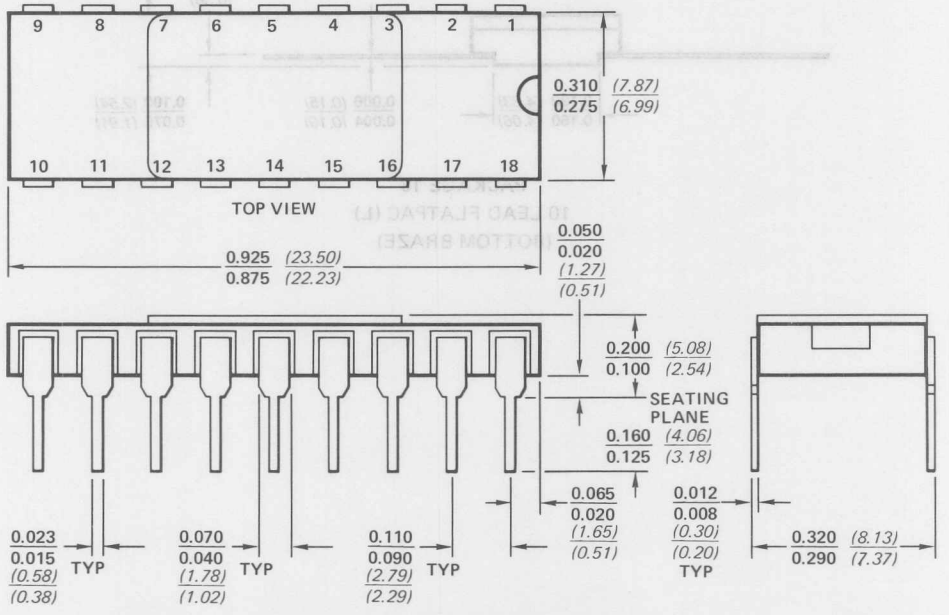
PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



PACKAGE 19
18 LEAD DUAL IN-LINE PACKAGE (J)
(PLASTIC)

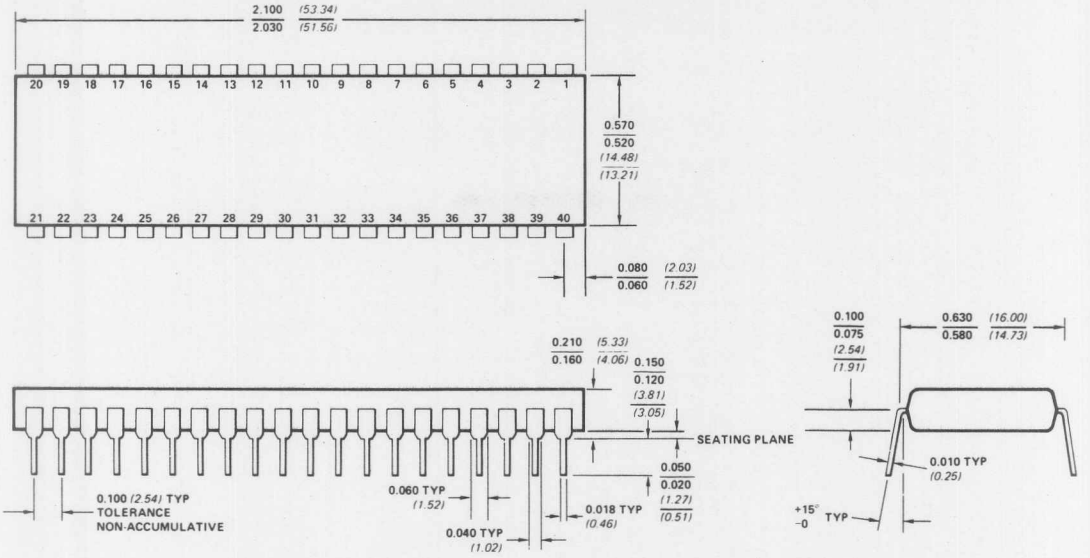


PACKAGE 20
18 LEAD DUAL IN-LINE PACKAGE (P)
(SIZE BRAZE)

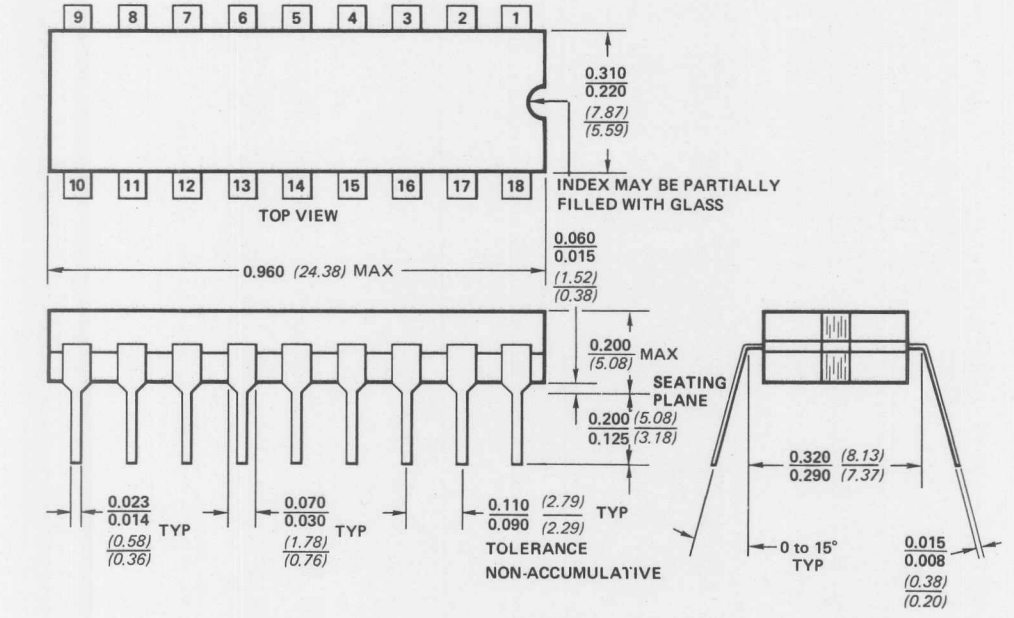
PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



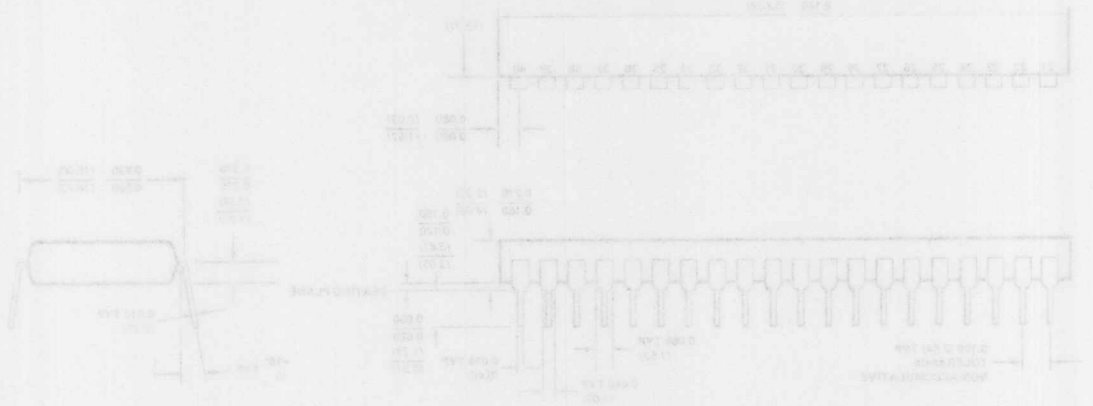
PACKAGE 22
40 LEAD DUAL IN-LINE PACKAGE (J)
(PLASTIC)

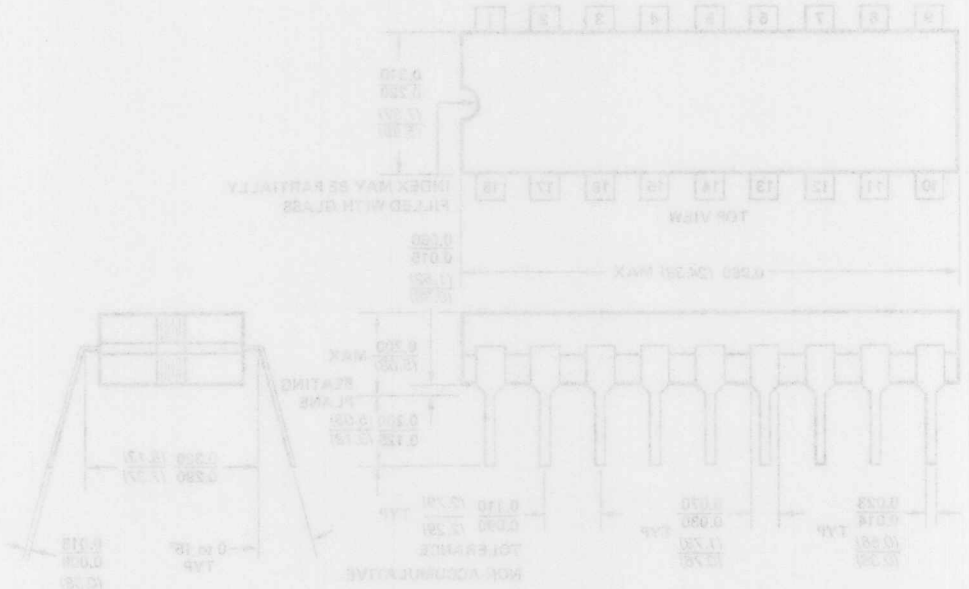


PACKAGE 23
18 LEAD DUAL IN-LINE PACKAGE (K)
(CERDIP)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)





Siliconix

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APPENDICES

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Publications Index

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F	AN70-2	FETs for Video Amplifiers
	AN71-1	A High Resolution CMRR Test Method
F	AN72-1	FETs in Balanced Mixers
A	AN72-2	FETs as Analog Switches
F	AN73-1	FETs as Voltage-Controlled Resistors
A	AN73-2	IC Multiplexer Increases Analog Switching Speeds
A	AN73-3	Switching High-Frequency Signals With FET Integrated Circuits
	AN73-4	Junction FETs in Active Double-Balanced Mixers
A	* AN73-5	Driver Circuits for the JFET Analog Switch
AIC	AN73-6	Function/Application of the L144 Programmable Micro-Power Triple Op Amp
F, A	* AN73-7	An Introduction to FETs
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A	AN74-2	Analog Switches in Sample and Hold Circuits
	AN74-3	Designing Junction FET Input Op Amps
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	AN76-1	Measuring High Frequency S-Parameters on the Dual Gate MOSFET
VA	* AN76-3	VMOS—A Breakthrough in Power MOSFET Technology
A	* AN76-6	DG300 Series Analog Switch Applications
AIC	* AN76-7	Function/Application of the L161 Micropower Comparator
AIC	* AN77-1	Function/Application of the LD120/ LD121 4½ Digit A/D Converter Set in Measurement Systems
VA	* AN77-2	Don't Trade Off Analog Switch Specs. VMOS—A Solution to High Speed, High Current, Low Resistance Analog Switches
VA	* AN79-1	A 500 KHz Switching Inverter for 12 V Systems
VA	* AN79-3	Dynamic Input Characteristics of a VMOS Power Switch
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	TA76-2	A New Technology: Application of VMOS Power FETs for High Frequency Communications
VA	* TA78-2	Designing a VMOS 250 Watt Off-Line Inverter

Catalogs

Analog Switch & IC Product Data Book

Analog Switches and Their Applications ($7.95 charge)

FET Design Catalog

VMOS Power FETs Design Catalog

VMOS Power FETs Applications Handbook

OEM Pricing with Cross Reference

RF Power FET Short Form Catalog

Siliconix Short Form Selector Guide

Key

Catalogs

AIC = Analog Switch & IC Product Data Book

A = Analog Switches and Their Applications

F = FET Design Catalog

VA = VMOS Applications Handbook

*Available in bound catalog only.

Title

Reprints & Reports

- Siliconix, Inc. Annual Report.
- Designing a VMOS 250 Watt Off-Line Inverter. David C. Hoffman, *Powercon* 3/78
- Designing with CODECs: Know Your A's and μ's. Thomas J. Mroz, *EDN* 5/76
- Log Data under μ Control. Gary Grandbois, *Electronic Design* 5/76
- Higher Power Ratings Extend VMOS FETs' Dominion. Arthur D. Evans, David C. Hoffman, Edwin S. Oxner, Walter Heinzer and Lee Shaeffer. *Electronics* 6/78
- CODEC has On-Chip Signaling for Phone Applications, Walter Heinzer and Steve Bolger, *Electronics* 6/7/79
- A Microprocessor Controlled VMOS Power Supply, David C. Hoffman
- Control Analog Signals with Voltage, Stephen Moore, *Electronic Design,* 1978
- Exploit VMOS FETs' Advantages to Drive Bipolar Power Transistors, F. Michael Barlage, *Powercon* 5/78
- Rely on IC Analog Switches for Fast Small-Signal Control, *EDN,* August 5, 20, Sept. 5, 1980
- Composite Op Amp Outperforms FET-input ICs, *EDN*, May 27, 1981.

Book

Designing with Field-Effect Transistors, Edited by Arthur D. Evans. Available at your technical bookstore or write to Suite 26-1; McGraw Hill Book Co.; 1221 Avenue of the Americas; New York, NY 10020.

Glossary of Terms and Abbreviations

A_V — DC Closed Loop Voltage Gain
A_{VOL} — DC Open Loop Voltage Gain
AZ IN — Auto-Zero Amplifier Input
AZ OUT — Auto-Zero Amplifier Output
BCD — Binary Coded Decimal
B_n — BCD Data Bit Outputs
C_{AZ} — Auto-Zero Storage Capacitance
C_{INT} — Integrator Capacitance
C_L — Load Capacitance
CMR — Common Mode Range
CMRR — Common Mode Rejection Ratio
COMP — Analog Comparator Output
C_{OSC} — Oscillator Capacitance
C_{STRG} — Auto-Zero Storage Capacitance
D_n — Digit Strobe Outputs
EOC — End of Conversion Signal
f_{CLK} — Clock Frequency
f_{IN} — Clock Input Frequency
f_L — Line Frequency
f_o — Resonant Frequency
FS — Full Scale
H_o — Gain at the Resonant Frequency
I_{BIAS} — Input Bias Current
I_{CL} — Clock Input Current, Clock Voltage Low
I_{DD} — Drain Supply Current
I_{IN} — Input Current
I_{INH} — Logic Input Current, Input Voltage High
I_{INL} — Logic Input Current, Input Voltage Low
INT IN — Integrator Summing Node (Input)
INT OUT — Integrator Amplifier Output
I_o — Output Current
I_{OH} — Output Current, Output Voltage High
I_{OL} — Output Current, Output Voltage Low
I_{OS} — Input Offset Current
I_R — Reference Supply Current
I_{RH} — Reference Supply Current, Input Voltage High
I_{RL} — Reference Supply Current, Input Voltage Low
I_S — Supply Current or FET Source Current
I_{SC} — Output Short Circuit Current
$I_{S(off)}$ — Source OFF Leakage Current
I_{SS} — Source Supply Current
I_1 — Positive Supply Current
I_2 — Negative Supply Current
$I+$ — Positive Supply Current
$I-$ — Negative Supply Current
LSB — Least Significant Bit
MSB — Most Significant Bit
M/Z — Measure-Zero Logic Output
NC — No Connection
NMR — Normal Mode Rejection at Input
OC — Open Collector Logic
OF — Overflow Logic Output Pulse
OR — Overrange Logic Output Pulse
P — Pull-Up Gate
P_D — Power Dissipation
P-P — Peak to Peak
PSRR — Power Supply Rejection Rate
Q — Quality Factory
$r_{DS(on)}$ — ON Resistance of FET Switch
— Drain-Source ON Resistance (D.C. measurement)
REF_{out} — Reference Output Voltage
R_{in} — Input Resistance

Glossary of Terms and Abbreviations (Cont'd)

R_L — Load Resistance
R_S — Input Source Resistance
R_{SET} — Set Current Resistance
S — Source
SCAN — Sequential/Interlace Digit Scan Logic Input
S_R — Slew Rate
T_A — Ambient Temeprature
TC — Temperature Coefficient
t_{off} — Turn-Off Time
$t_{off(En)}$ — Enable Turn-Off Time
t_{on} — Turn-On Time
$t_{on(En)}$ — Enable Turn-On Time
t_{open} — Break-Before-Make Interval
t_r — Response Time
$t_{transition}$ — Switching Time of Multiplexer
U/D — Up/Down Logic Output
UR — Underrange Logic Output Pulse
V_A — Address Input Voltage
V_{AH} — Address Input Voltage, High
V_{AL} — Address Input Voltage, Low
V_{AZ} — Auto-Zero Amplifier Output Voltage
$V_{AZ(in)}$ — Auto-Zero Switch Input Voltage
V_B — Body Voltage
$V_{CLOCK\ IN}$ — Clock Logic Input Voltage
V_D — Drain Voltage
V_{DB} — Drain-Body Voltage
V_{DD} — Drain Supply Voltage; Negative for PMOS, Positive for NMOS and CMOS
V_{En} — Enable Input Voltage
V_G — Gate Voltage
V_{GB} — Gate-Body Voltage
V_{GD} — Gate-Drain Voltage
V_{GS} — Gate-Source Voltage
$V_{GS(off)}$ — Gate-Source Pinchoff Voltage
$V_{GS(th)}$ — Gate-Source Threshold Voltage
V_{HI-Q} — High Quality Ground Input Voltage
V_{IN} — Input Voltage
V_{INH} — Logic Input Voltage, High
V_{INL} — Logic Input Voltage, Low
V_L — Logic Supply Voltage
V_O — Output Voltage
V_{OH} — Output Voltage, High
V_{OL} — Output Voltage, Low
V_{OS} — Input Offset Voltage
V_{OUT} — Output Voltage Swing
V_P — Pull-Up Gate Voltage
V_{PB} — Pull-Up Gate to Body Voltage
V_R — Reference Voltage
V_{REF} — Threshold Reference Voltage — Positive Reference Voltage
V_S — Source Supply Voltage
V_{SB} — Source-Body Voltage
V_{SS} — Source Supply Voltage; Positive for PMOS, Negative for NMOS and CMOS
V_{STRG} — Auto-Zero Loop Storage Voltage
V_1 — Positive Supply Voltage
V_2 — Negative Supply voltage
V+ — Positive Supply Voltage
V− — Negative Supply Voltage
Z_{IN} — Input Impedance
$\Delta r_{DS(on)}$ — Fractional Change in Drain-Source ON Resistance (D.C. measurement)